AD7683 HDL Driver

Revision history

Date	Rev	Description
01.07.2013	0.1	Document creation

Contents

1. Introduction

This document describes the HDL driver for the AD7683 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture
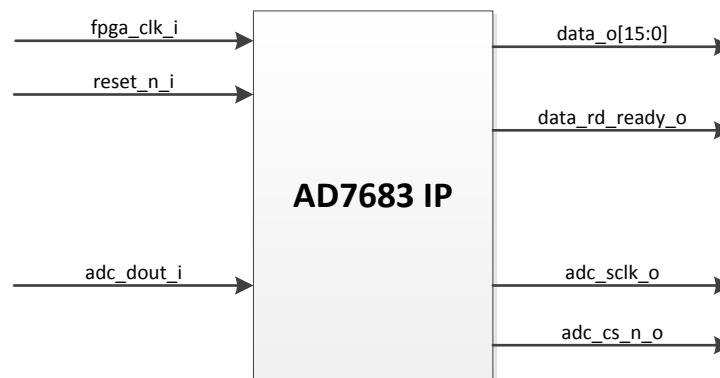
Fig. 1 presents the block diagram of the AD7683 IP.

Fig. 1 AD7683 IP

Table 1 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7683. The IP continuously reads the conversion results from the AD7683 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
Ad7683 control and data ports			
ADC_DOUT_I	IN	1	ADC Serial Data signal. The conversion result is output on this pin. It is synchronized to SCLK.
ADC_SCLK_O	OUT	1	ADC Serial Data Clock signal. When the part is selected, the conversion result is shifted out by this clock.
ADC_CS_N_O	OUT	1	ADC CS signal. On the falling edge, the ADC initiates the conversions. The part returns to shutdown mode as soon as the conversion is completed.

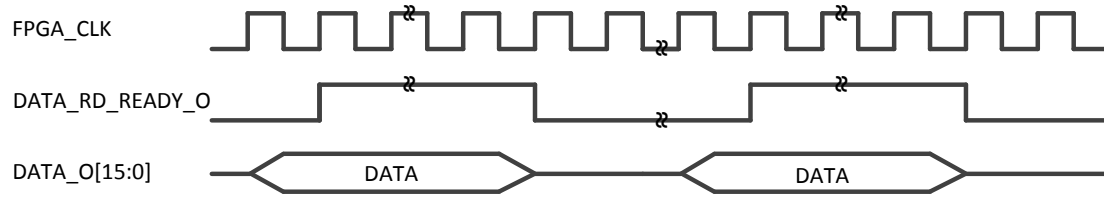Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

Fig. 2. Read operations timing diagram