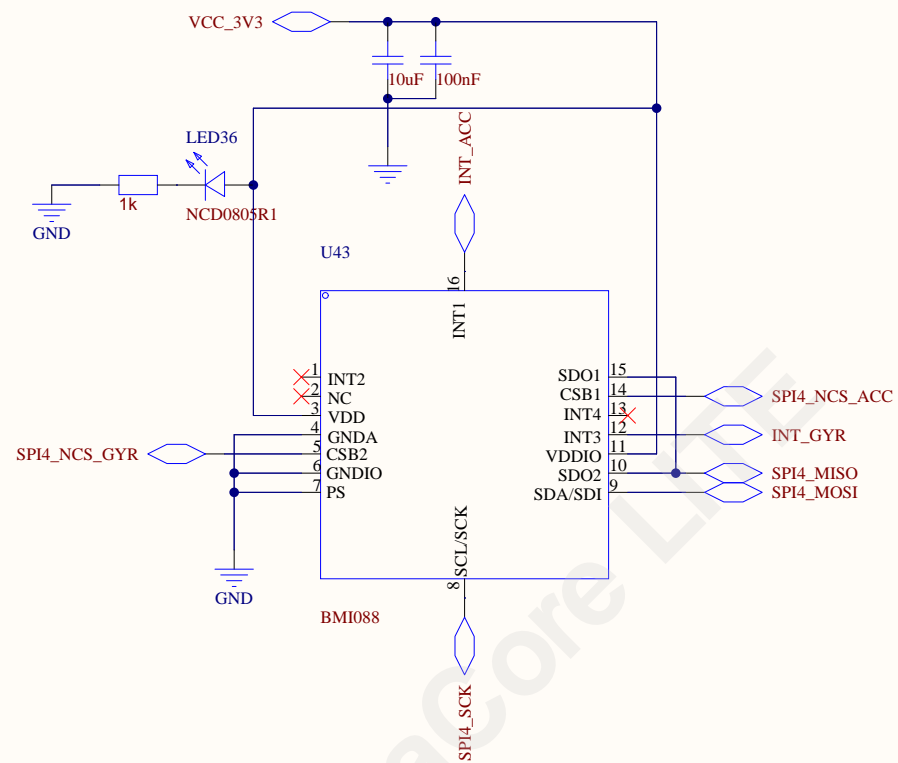

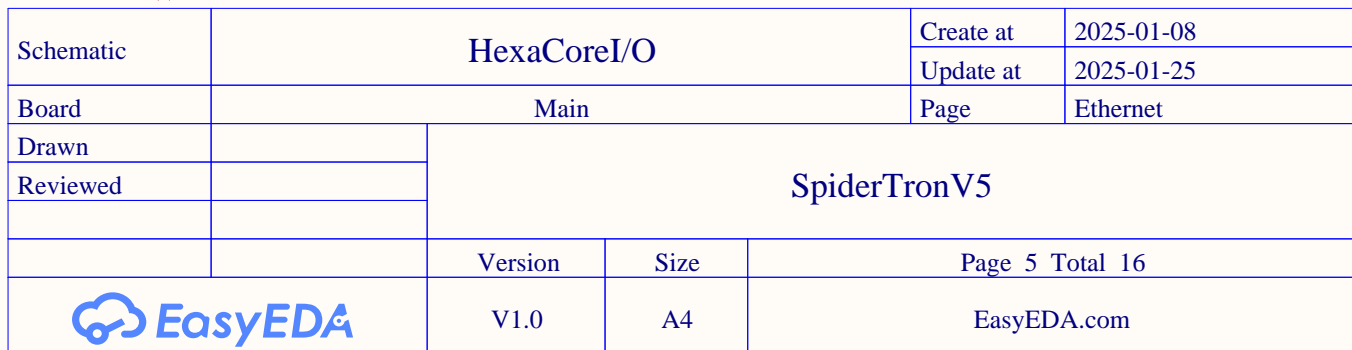
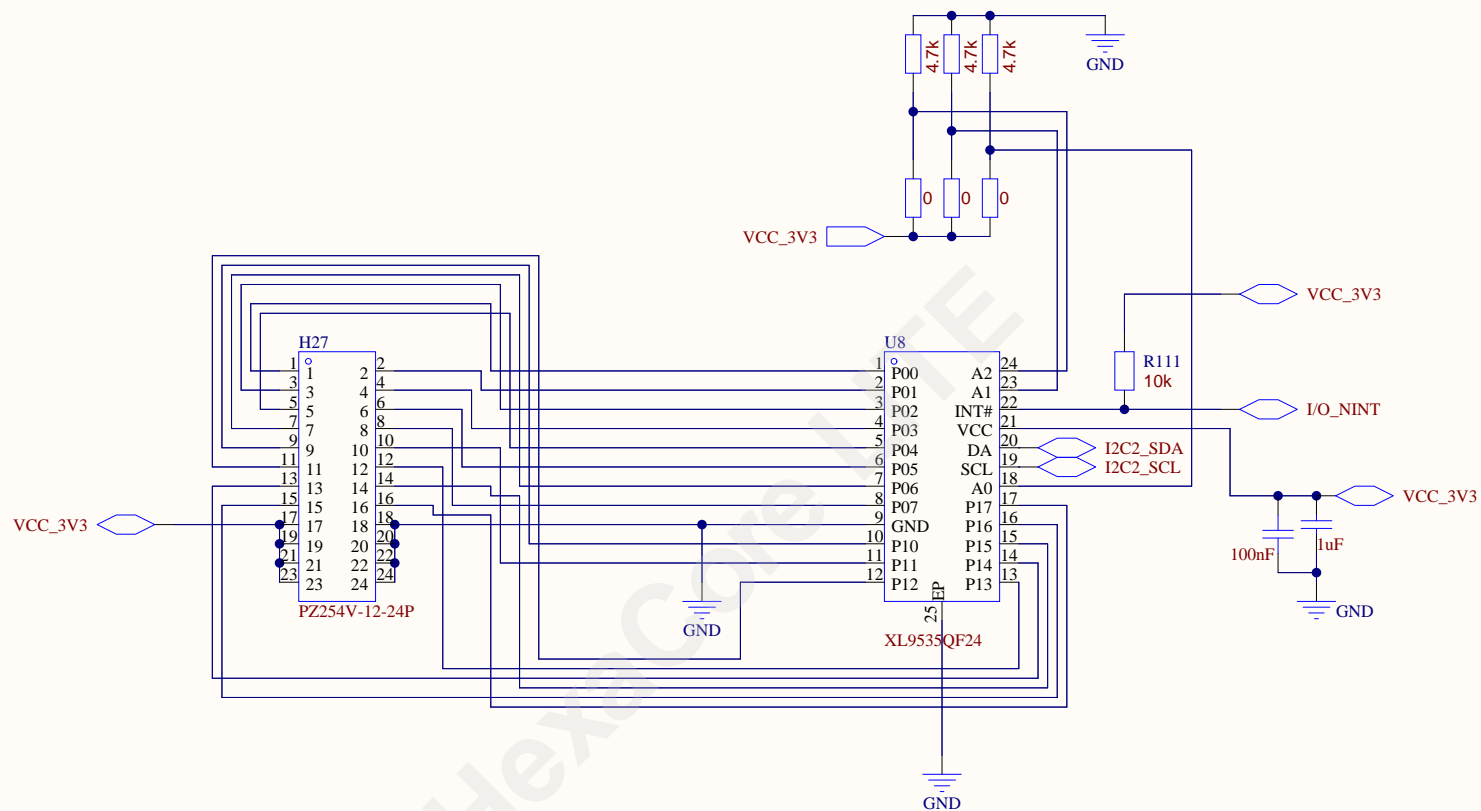



Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-12
Board	Main			Page	Debugger
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 2 Total 16	
EasyEDA		V1.0	A4	EasyEDA.com	

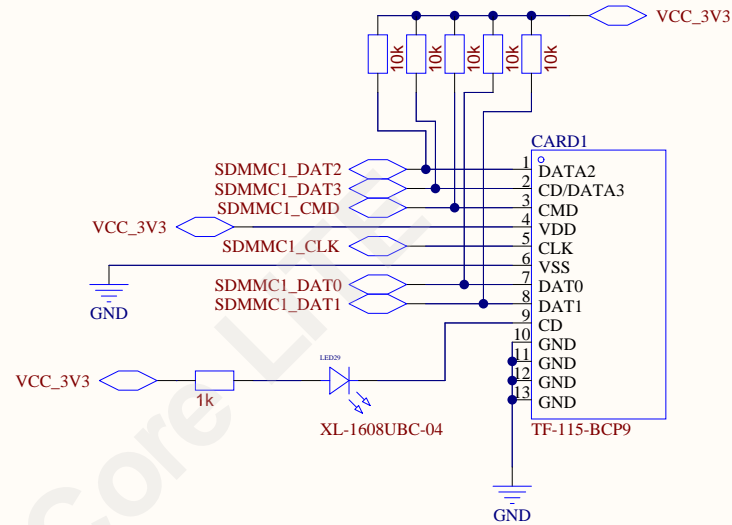


Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-15
Board	Main			Page	IMU
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 3 Total 16	
		V1.0	A4	EasyEDA.com	

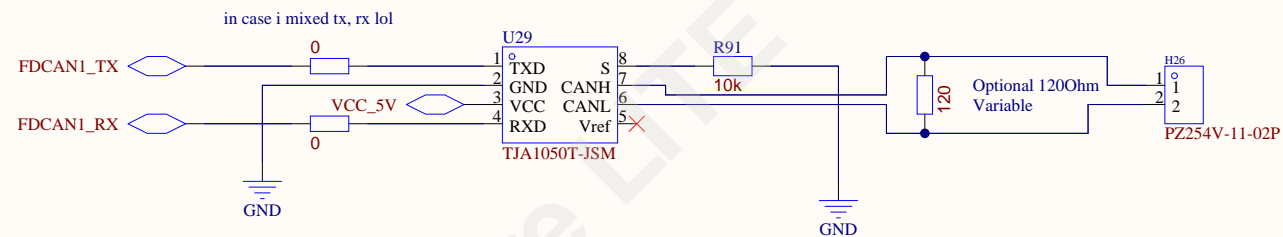




Schematic	HexaCoreI/O			Create at	2025-01-08
Board	Main			Update at	2025-01-13
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 6 Total 16	
		V1.0	A4	EasyEDA.com	



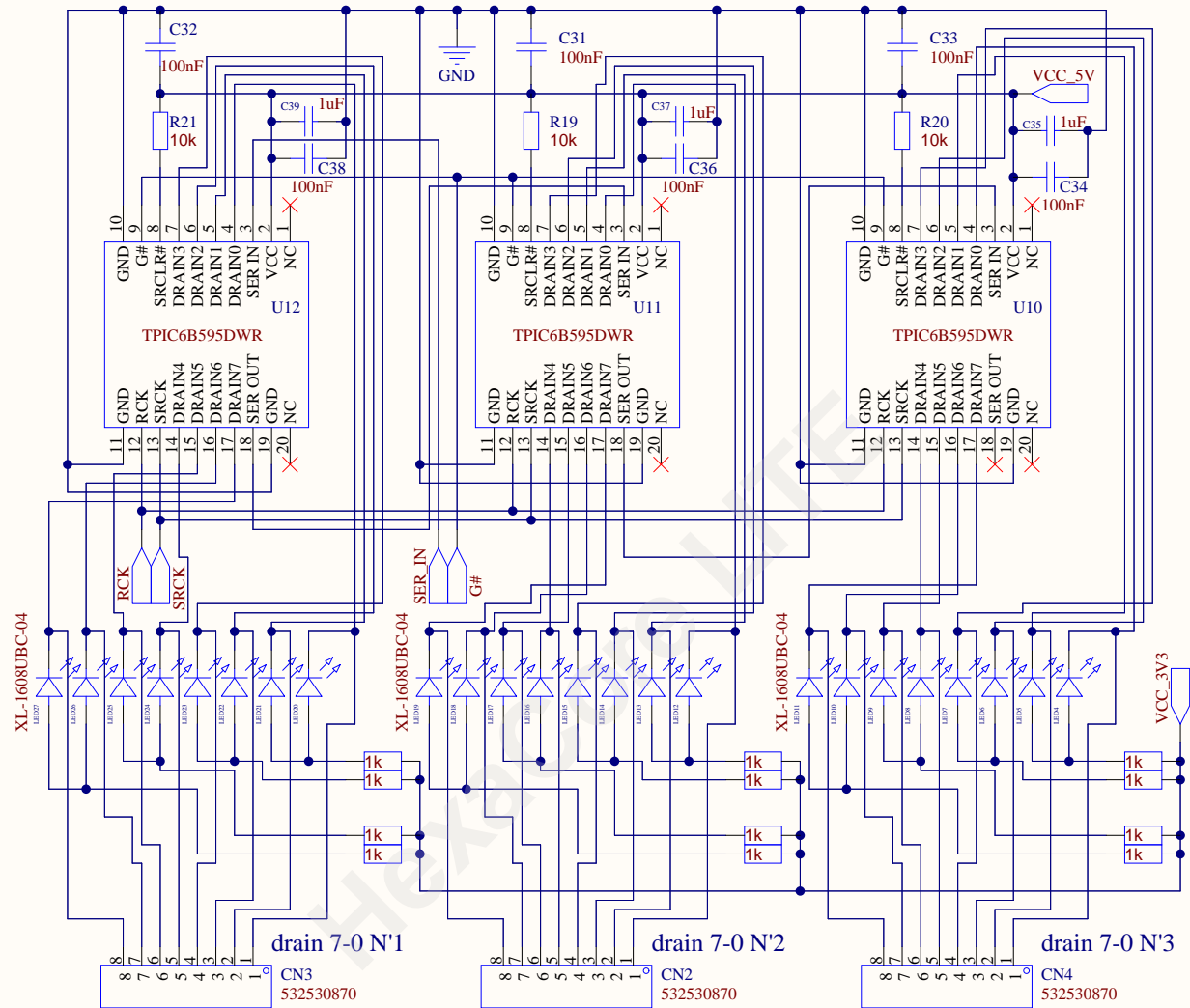
Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-25
Board	Main			Page	Micro SD
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 7 Total 16	
EasyEDA		V1.0	A4	EasyEDA.com	



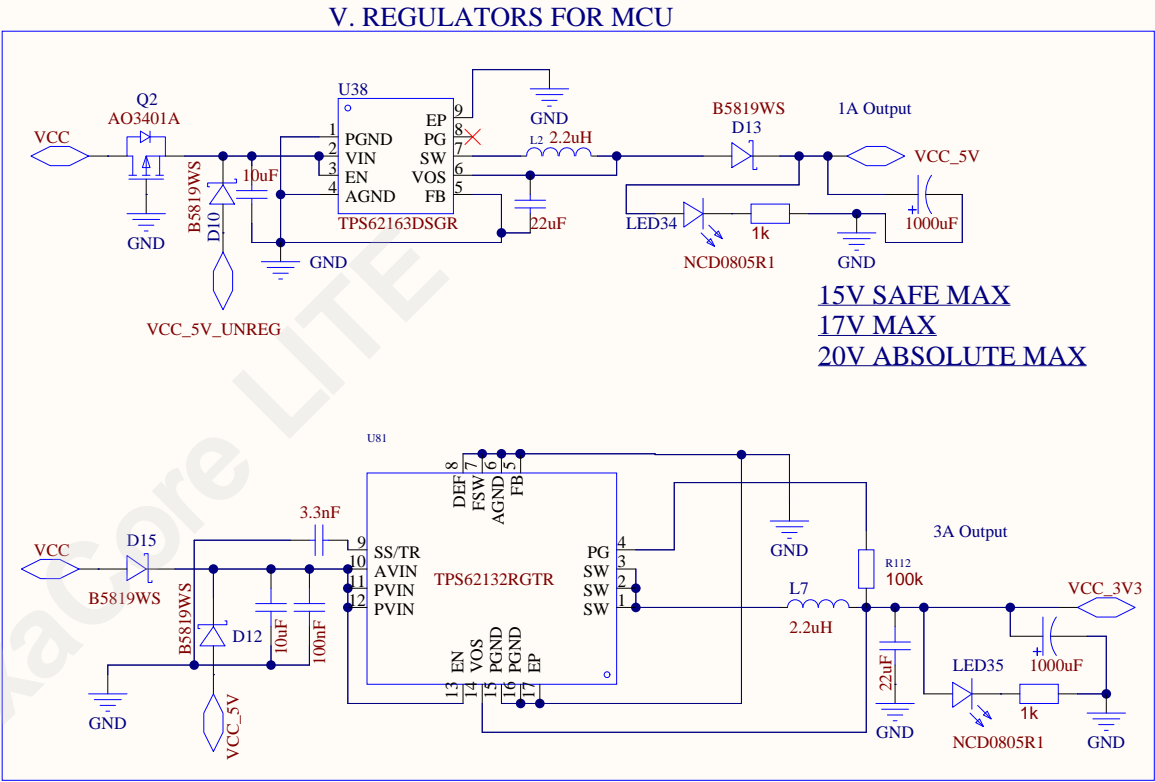
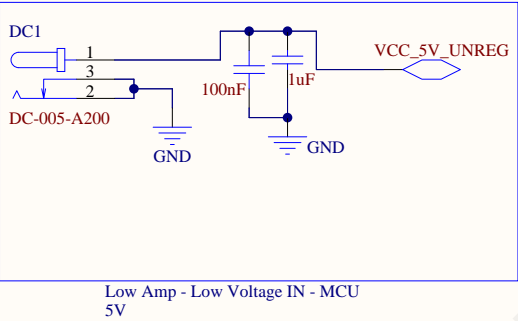
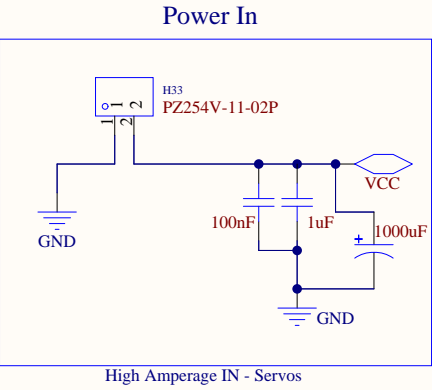
Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-02-07
Board	Main			Page	CAN
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 8 Total 16	
EasyEDA		V1.0	A4	EasyEDA.com	



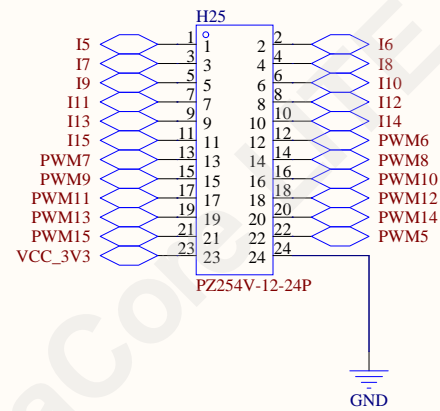
21x Servo GND-VCC-SIG
EACH 5 AMP FUSE



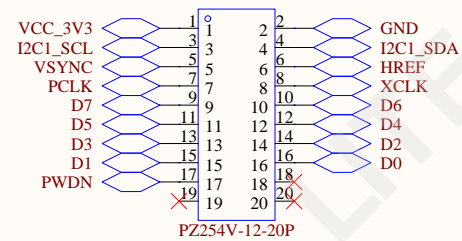
Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-25
Board	Main			Page	Shift Registers
Drawn	SpiderTronV5				
Reviewed					
		Version	Size	Page 10 Total 16	
		V1.0	A4	EasyEDA.com	



Schematic	HexaCoreI/O			Create at	2025-01-08
Board	Main			Update at	2025-02-06
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 12 Total 16	
EasyEDA		V1.0	A4	EasyEDA.com	



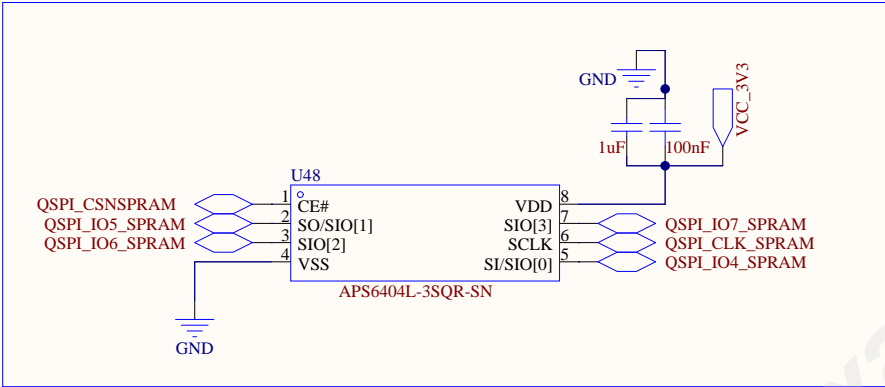
Schematic	HexaCoreI/O			Create at	2025-01-10
				Update at	2025-01-12
Board	Main			Page	ExtraPins
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 14 Total 16	
		V1.0	A4	EasyEDA.com	



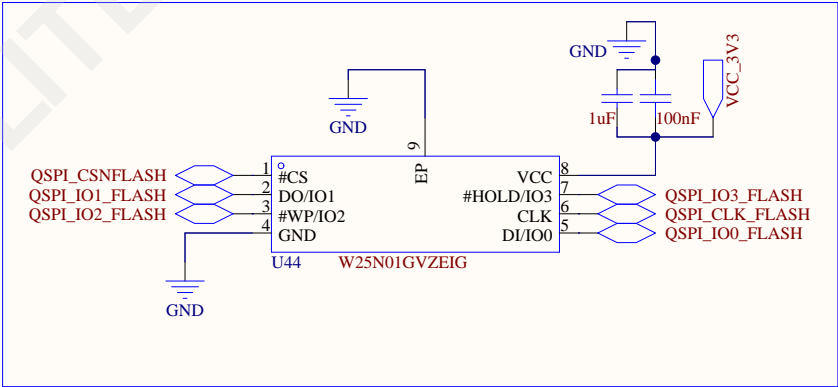
Schematic	HexaCoreI/O			Create at	2025-01-21
				Update at	2025-01-22
Board	Main			Page	DCMI Camera Pins
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 15 Total 16	
EasyEDA		V1.0	A4	EasyEDA.com	

QUAD SPI, CONNECTED TO STM32 OCTOSPI IN0-7

SPRAM 64Mbit 8~mByte



FLASH 1Gbit, 128~Mbytes



Schematic	HexaCoreI/O			Create at	2025-01-09
				Update at	2025-02-02
Board	Main			Page	Flash & RAM
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 16 Total 16	
		V1.0	A4	EasyEDA.com	