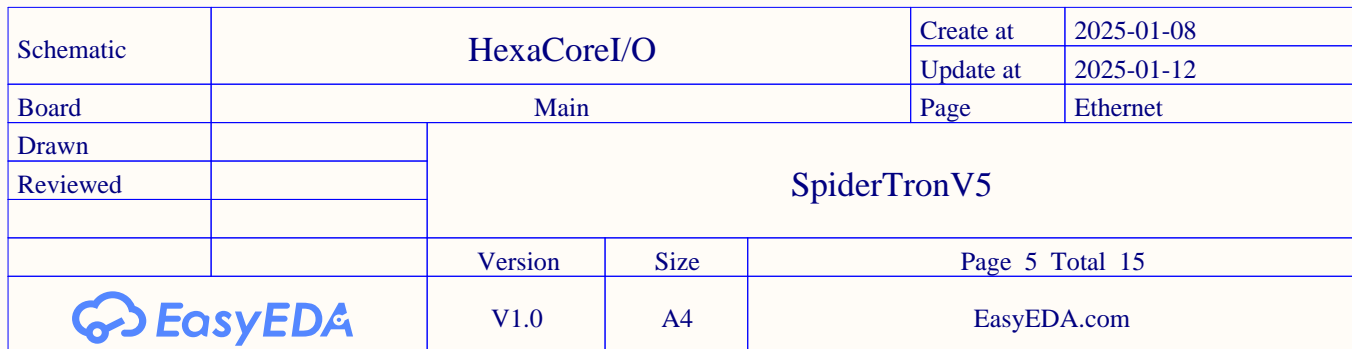
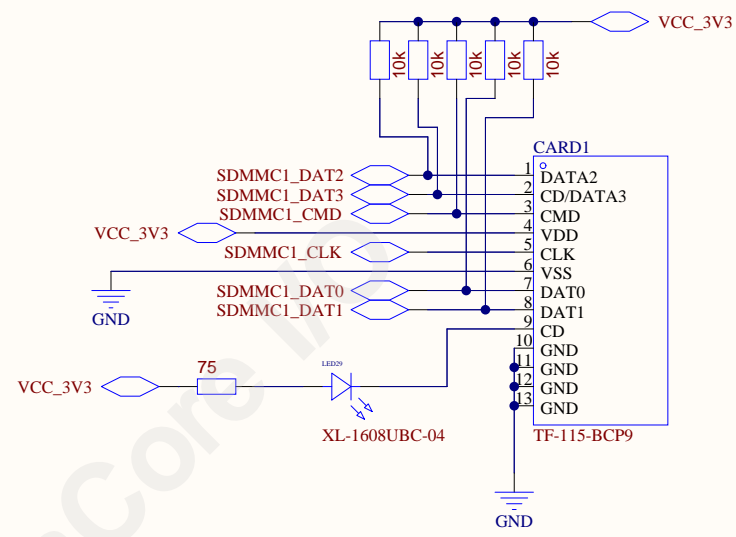
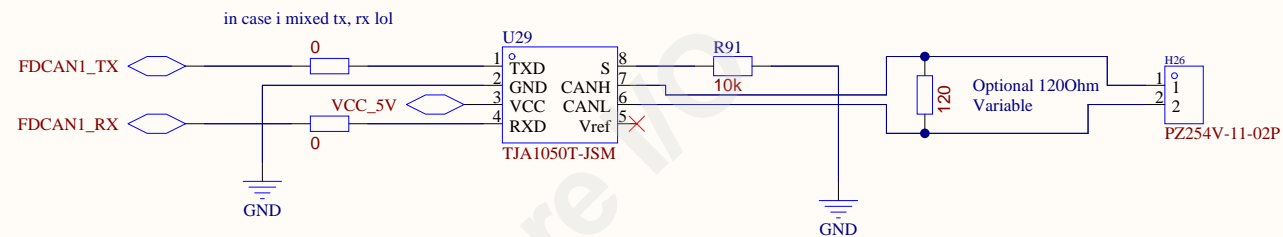


Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-12
Board	Main			Page	Debugger
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 2 Total 15	
EasyEDA		V1.0	A4	EasyEDA.com	

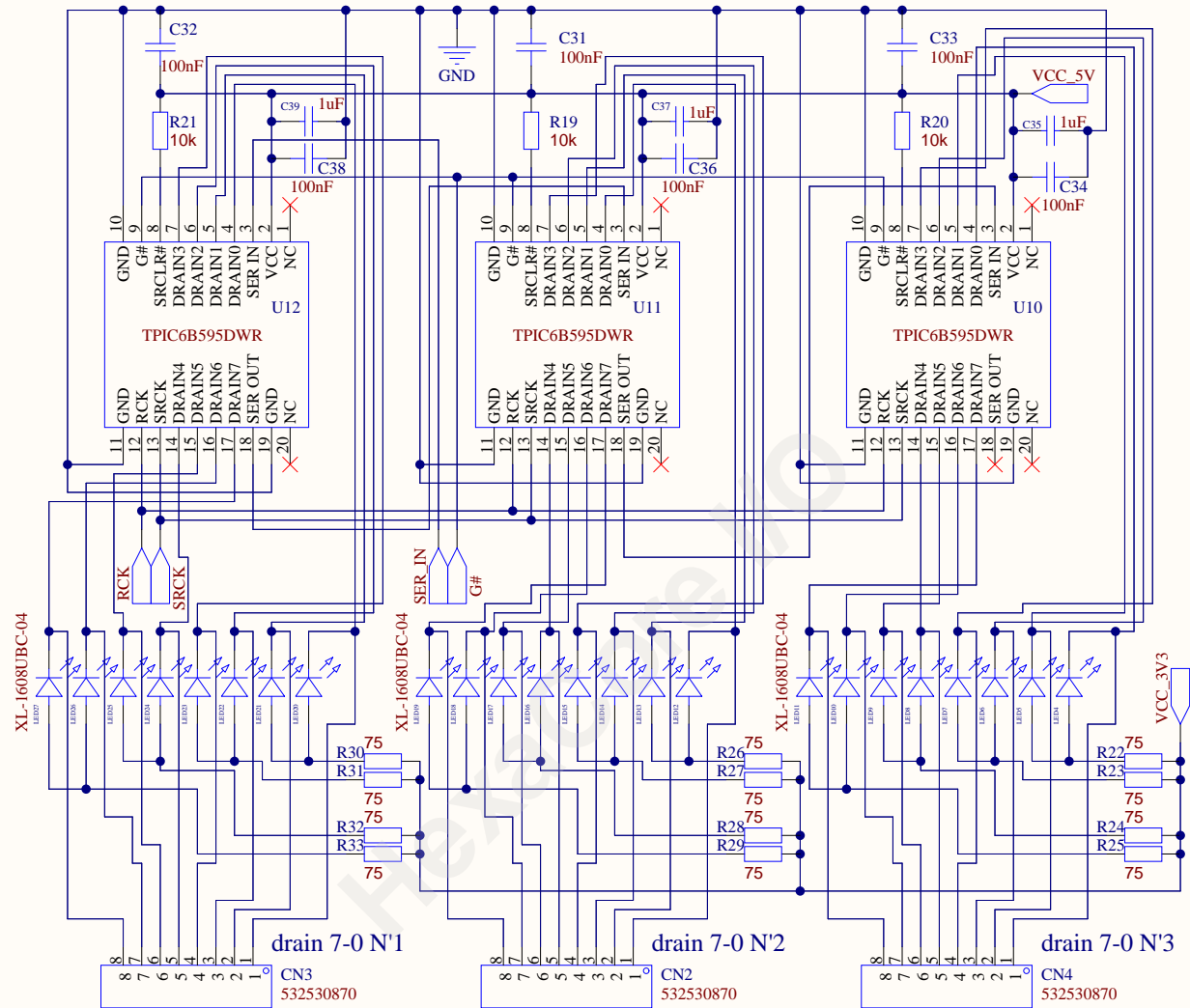




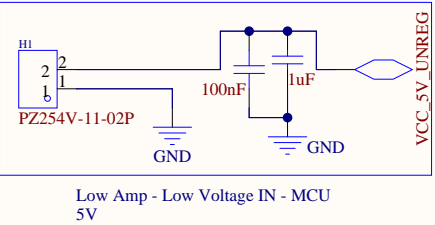
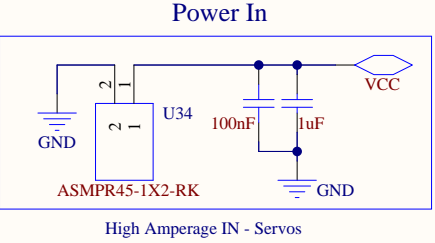
Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-12
Board	Main			Page	Micro SD
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 7 Total 15	
EasyEDA		V1.0	A4	EasyEDA.com	



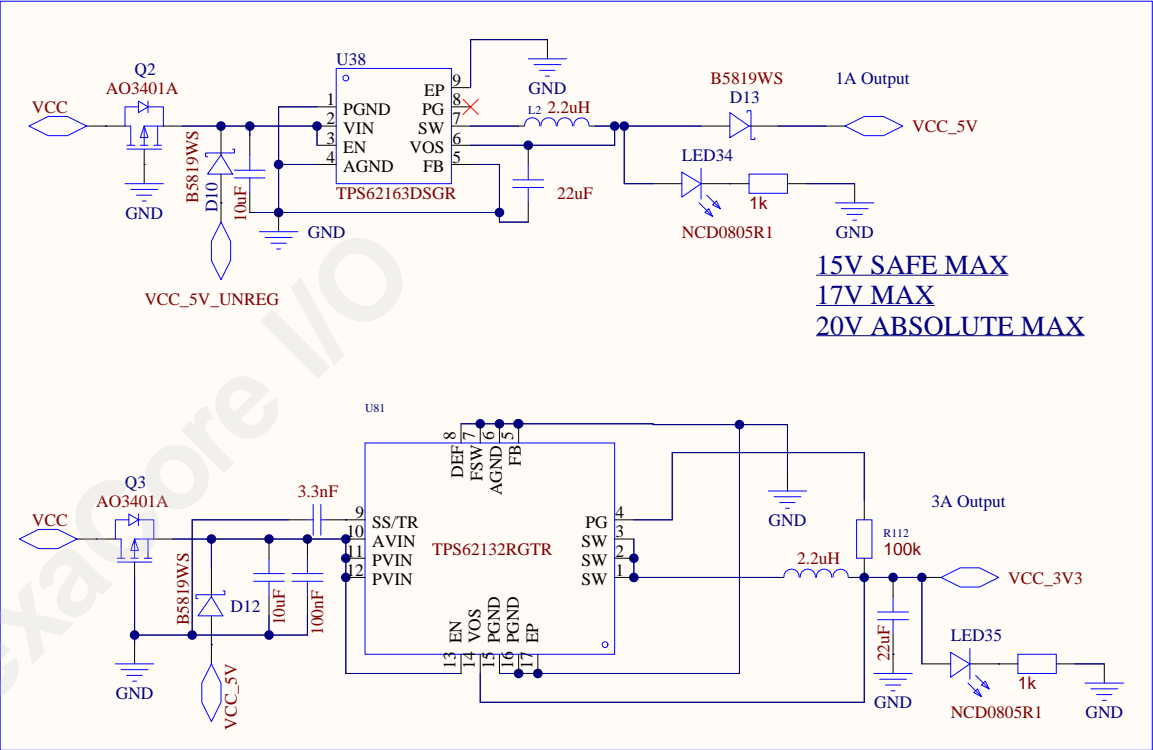
Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-12
Board	Main			Page	CAN
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 8 Total 15	
EasyEDA		V1.0	A4	EasyEDA.com	



Schematic	HexaCoreI/O			Create at	2025-01-08
				Update at	2025-01-10
Board	Main			Page	Shift Registers
Drawn	SpiderTronV5				
Reviewed					
		Version	Size	Page 10 Total 15	
		V1.0	A4	EasyEDA.com	



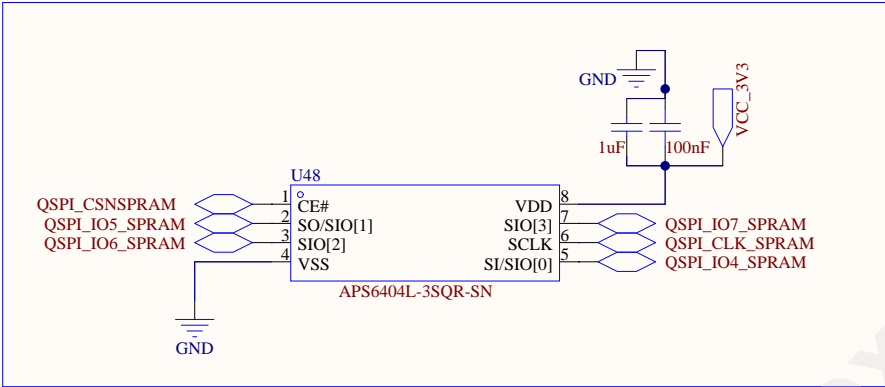
V. REGULATORS FOR MCU



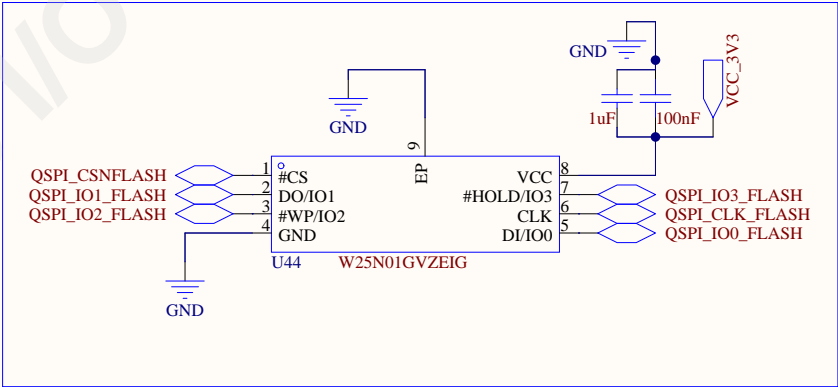
Schematic	HexaCoreI/O			Create at	2025-01-08
Board	Main			Update at	2025-01-12
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 12 Total 15	
EasyEDA		V1.0	A4	EasyEDA.com	

QUAD SPI, CONNECTED TO STM32 OCTOSPI IN0-7

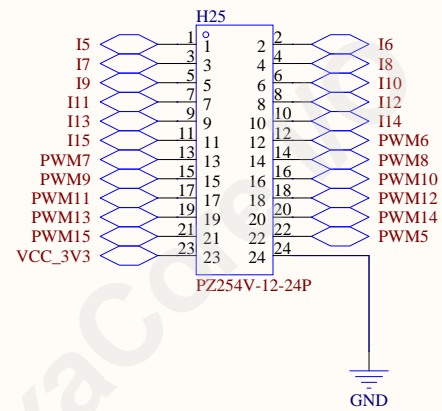
SPRAM 64Mbit 125~kByte



FLASH 1Gbit, 125~Mbytes



Schematic	HexaCoreI/O			Create at	2025-01-09
				Update at	2025-01-12
Board	Main			Page	Flash & RAM
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 13 Total 15	
EasyEDA		V1.0	A4	EasyEDA.com	



Schematic	HexaCoreI/O			Create at	2025-01-10
				Update at	2025-01-12
Board	Main			Page	ExtraPins
Drawn		SpiderTronV5			
Reviewed					
		Version	Size	Page 15 Total 15	
EasyEDA		V1.0	A4	EasyEDA.com	