



CSE 112

SOPHOMORE CESS

SUMMER 2023

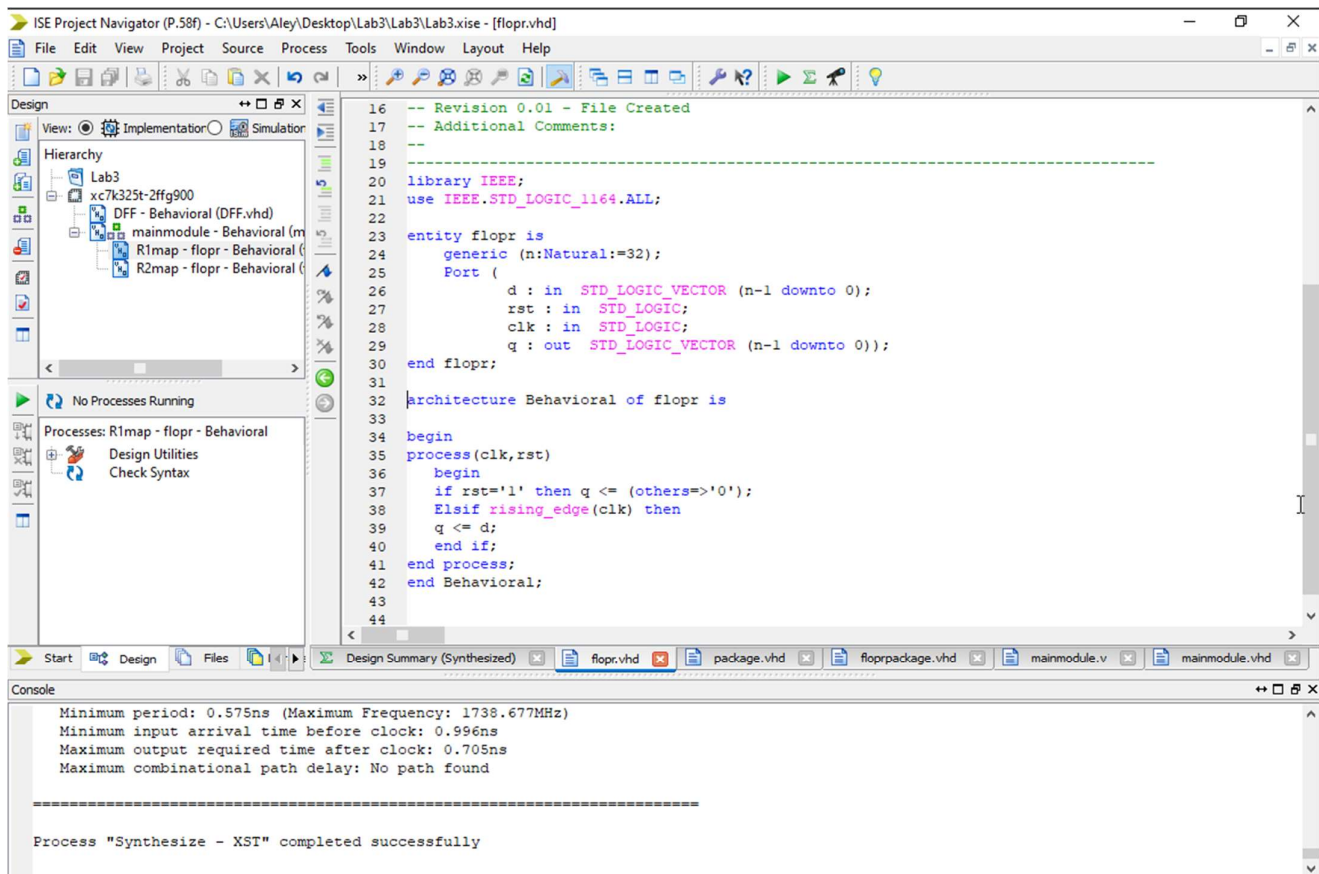
Lab (5):

Experiment Name: Flopr module

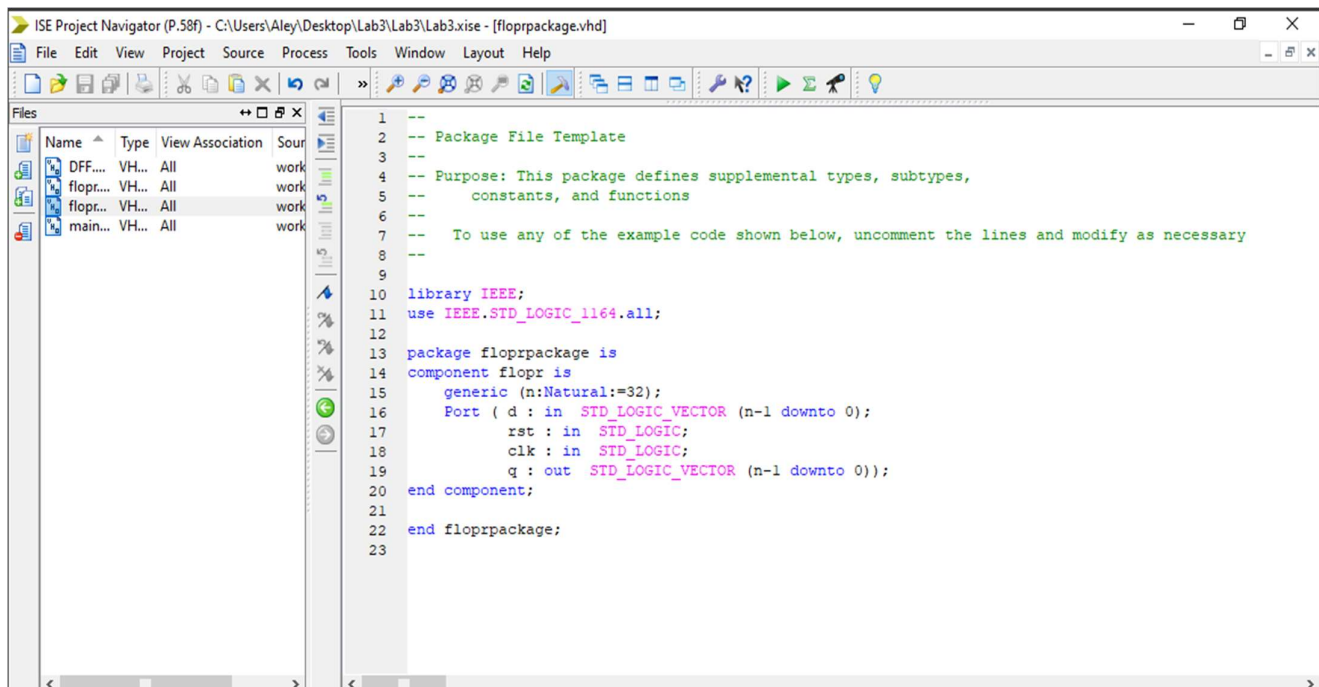
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Entity Code:



Package Code:



Main Module Code:

The screenshot shows the ISE Project Navigator interface. The main window displays the VHDL code for `mainmodule.vhd`. The code defines a generic entity `mainmodule` with a generic parameter `n` (default 32). It includes two output ports, `R1` and `R2`, both of type `STD_LOGIC_VECTOR` of size `n-1`. The architecture `Behavioral` implements two flopr blocks, `R1map` and `R2map`, using the `flopr` component from the `work.floprpackage`. The `R1map` block takes `tmp1` as input and `clk` as clock. The `R2map` block takes `tmp2` as input and `clk` as clock. The `tmp1` and `tmp2` signals are defined as `STD_LOGIC_VECTOR` of size `n-1`.

```
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use work.floprpackage.all;
23
24 entity mainmodule is
25     generic (n:natural := 32);
26     Port ( c : in  STD_LOGIC;
27           l : in  STD_LOGIC;
28           clk : in  STD_LOGIC;
29           R1 : out STD_LOGIC_VECTOR (n-1 downto 0);
30           R2 : out STD_LOGIC_VECTOR (n-1 downto 0));
31 end mainmodule;
32
33 architecture Behavioral of mainmodule is
34     signal tmp1,tmp2: STD_LOGIC_VECTOR (n-1 downto 0);
35     begin
36         tmp1 <= (others=>'1');
37         R1map : flopr generic map (n) port map(tmp1,c,clk,tmp2);
38         R2map : flopr generic map (n) port map(tmp2,not(1),clk,R2);
39         R1 <= tmp2;
40     end Behavioral;
41
42
43
```

The console window shows the synthesis results for the `mainmodule - Behavioral` process. The synthesis was completed successfully, and the console output includes the following information:

```
Minimum period: 0.575ns (Maximum Frequency: 1738.677MHz)
Minimum input arrival time before clock: 0.996ns
Maximum output required time after clock: 0.705ns
Maximum combinational path delay: No path found

Process "Synthesize - XST" completed successfully
```

Rtl:

