CSE 112

SOPHOMORE CESS

SUMMER 2023

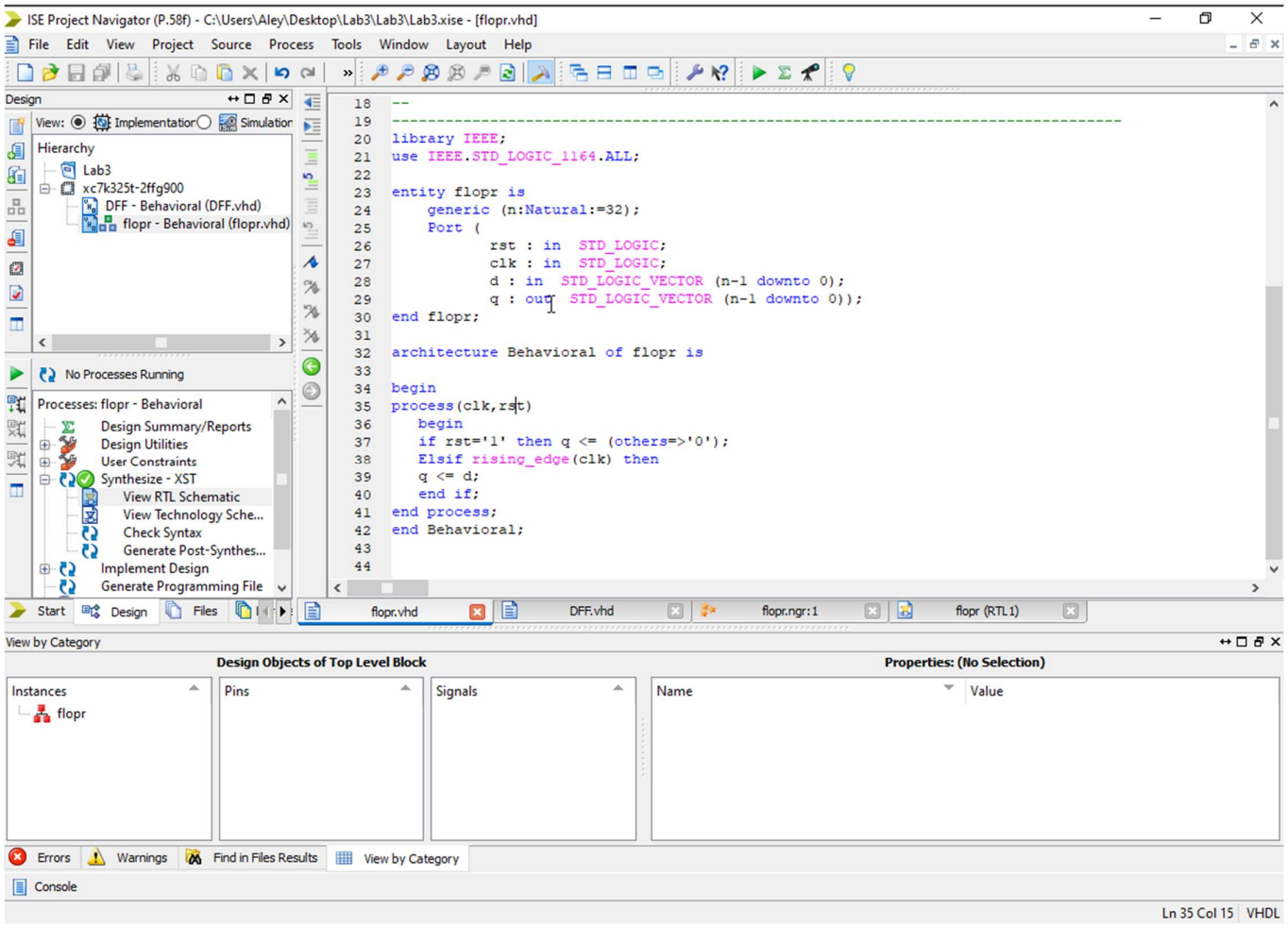
Lab (4):

Experiment Name: Flopr

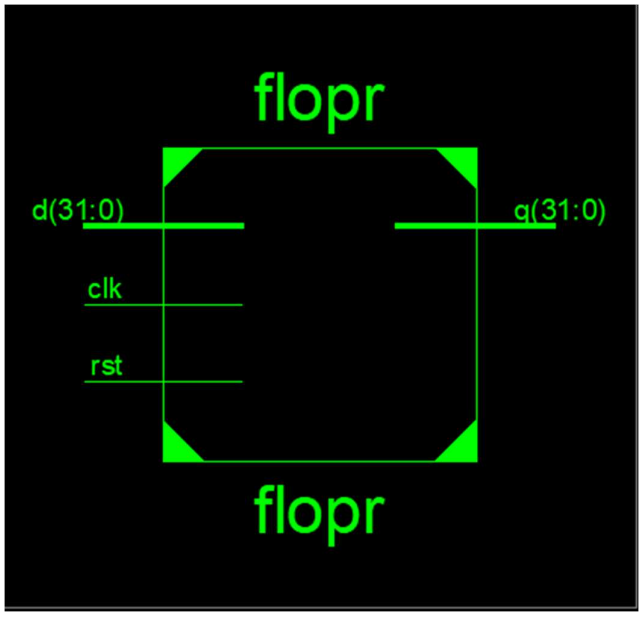
Student Name: Aley Amin Ahmed Shawky

Student ID: 21P0150

Code:


ISE Project Navigator (P.58f) - C:\Users\Aley\Desktop\Lab3\Lab3\Lab3.xise - [flopr.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Lab3
xc7k325t-2ffg900
DFF - Behavioral (DFF.vhd)
flopr - Behavioral (flopr.vhd)
No Processes Running
Processes: flopr - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sche...
Check Syntax
Generate Post-Synthes...
Implement Design
Generate Programming File
18 --
19 ----------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 entity flopr is
24 generic (n:Natural:=32);
25 Port (
26 rst : in STD_LOGIC;
27 clk : in STD_LOGIC;
28 d : in STD_LOGIC_VECTOR (n-1 downto 0);
29 q : out STD_LOGIC_VECTOR (n-1 downto 0));
30 end flopr;
31
32 architecture Behavioral of flopr is
33
34 begin
35 process(clk,rst)
36 begin
37 if rst='1' then q <= (others=>'0');
38 Elsif rising_edge(clk) then
39 q <= d;
40 end if;
41 end process;
42 end Behavioral;
43
44
Start Design Files
flopr.vhd DFF.vhd flopr.ngr:1 flopr (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
flopr
Pins
Signals
Name
Value
Errors Warnings Find in Files Results View by Category
Console
Ln 35 Col 15 VHDL

Rtl:


flopr
d(31:0)
q(31:0)
clk
rst
flopr