CSE111
Logic Design
Sophomore CESS
spring 2023

Major Task

Students :

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Phase 2

Objective: Refer to Fig. 2; Design a sequential circuit with X-type flip-flops and logic gates to count the sequence: 1, 6, A1, A2, A3, A4, A5, back to 1, and repeat; then display it on 7-segment. Where A1, A2, A3, A4, and A5 are defined, for example, as follows:

Your ID:	18p1271
Your colleague1 ID:	18p1529
Your colleague2 ID:	18p4382

- A1 = (1 + 1 + 4)/3 = 2 (the digit after 'p'. round up, if required)
- A2 = (2 + 5 + 3)/3 = 4 (round up, if required)
- A3 = (7 + 2 + 8)/3 = 5 (round down, if required)
- A4 = [(1 + 9 + 2)/3] – 1 = 3 (round down, if required)
- A5 = (A1 + A3 + A4)/3 = 4

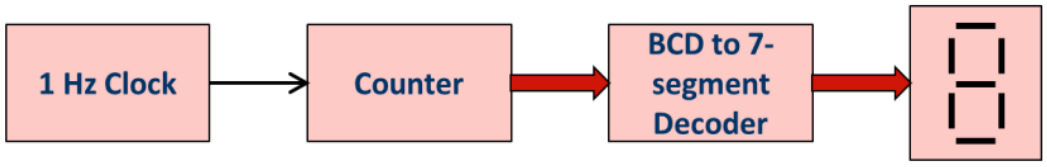
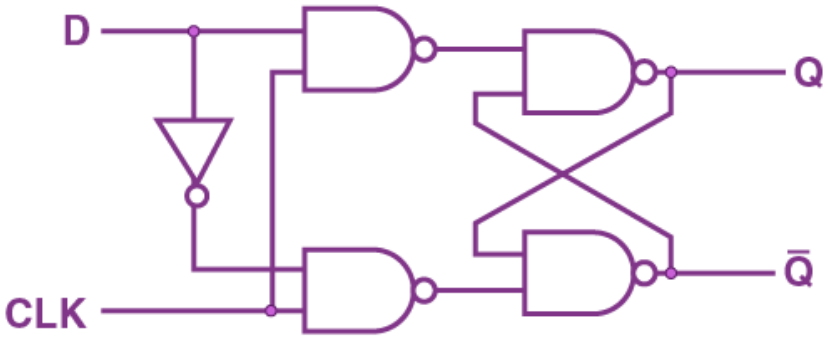


Figure 1: Block diagram of phase 2

Components used:

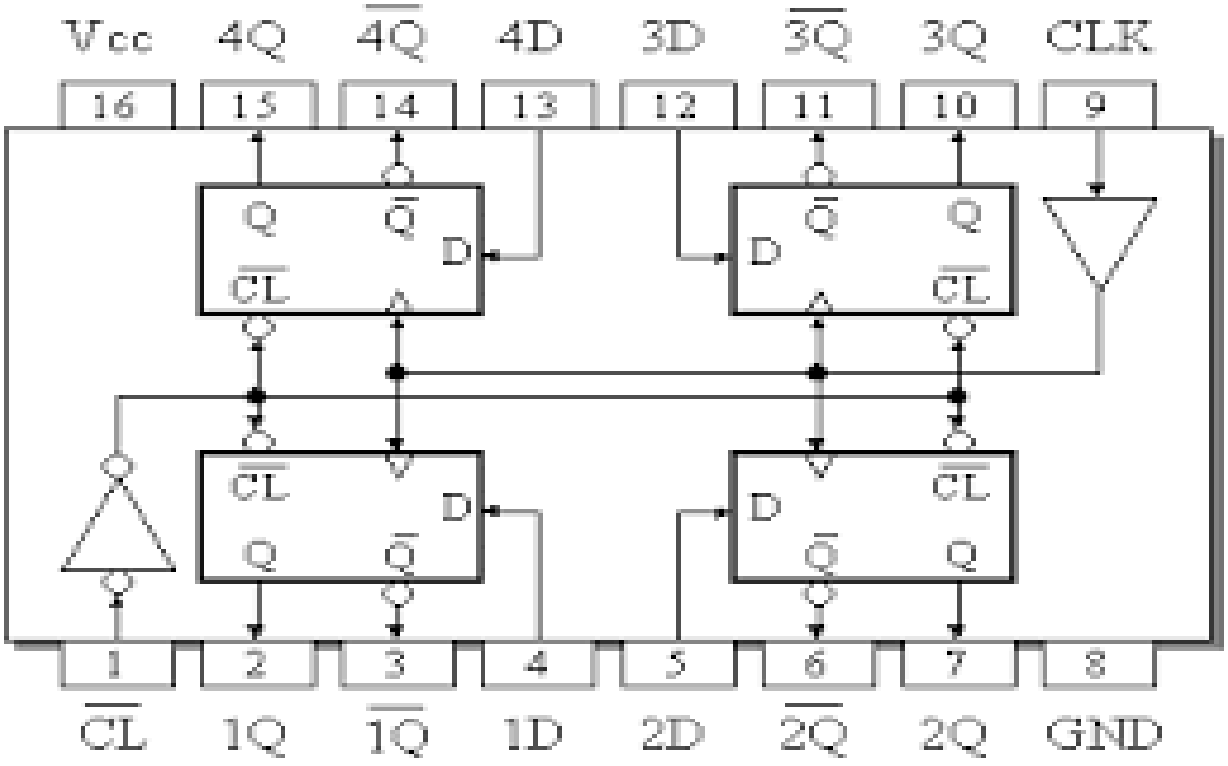
- 2x Breadboard
- Battery 9V
- Jumper wires
- resistances
- 2x capacitor
- 1x 555 timer
- 1x D-Flip Flop (74HC175)
- 1x 2 input And gate (74HC08)
- 1x3 input AND gate(74HC11)
- 1x Or gate (74HC32)
- 1x 7-segement decoder (74HC48)
- 1x 7 segment display

D F/F:

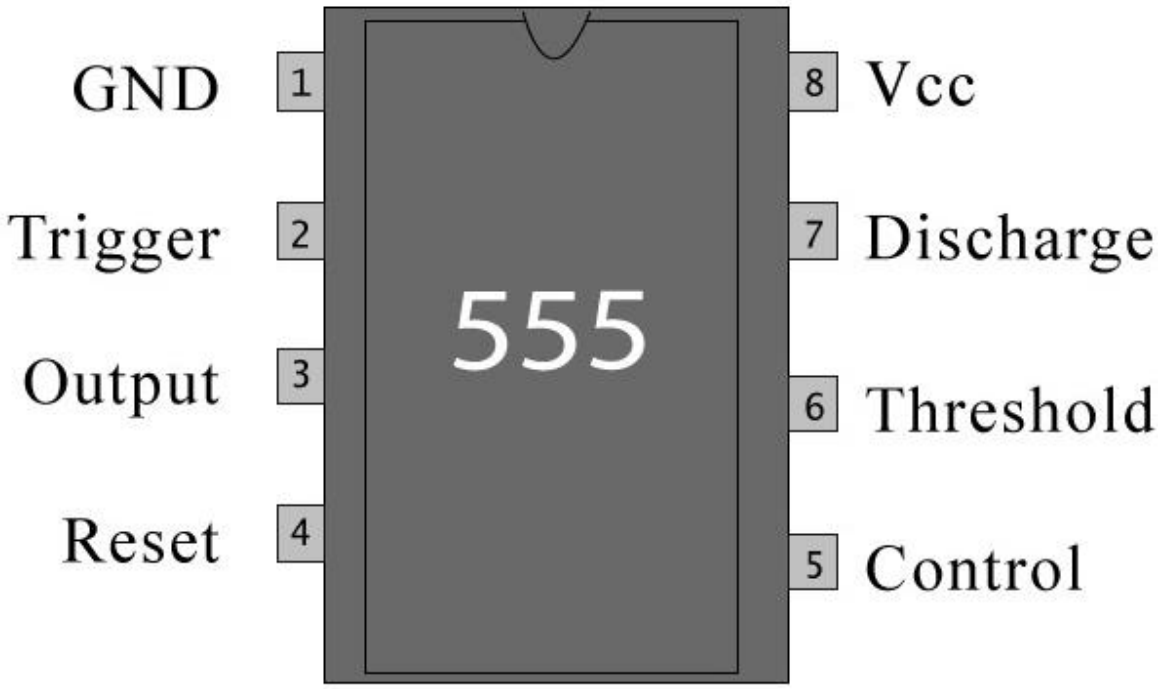


Truth Table

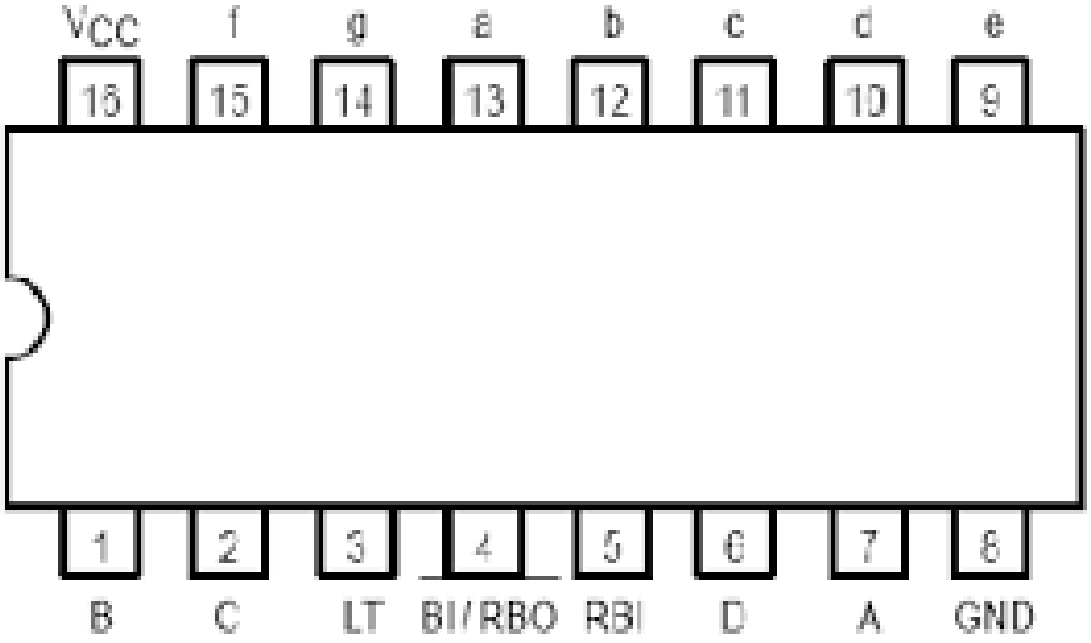
Q	D	$Q_{(t+1)}$
0	0	0
0	1	1
1	0	0
1	1	1



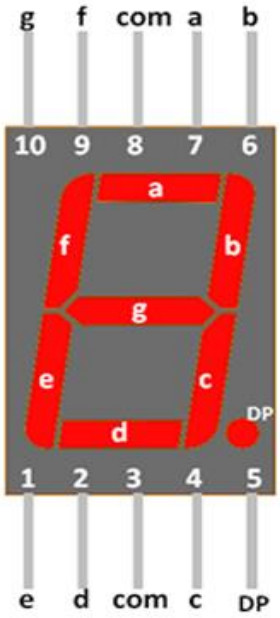
555 Timer:


GND
1
Trigger
2
Output
3
Reset
4
555
8
Vcc
7
Discharge
6
Threshold
5
Control

7-segement Decoder

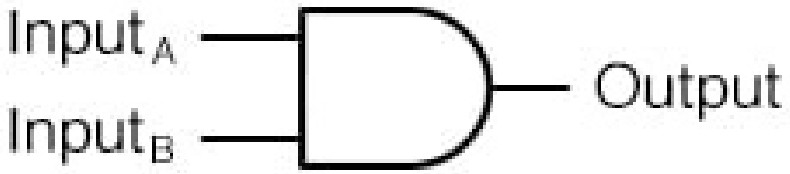


7-segemnt display

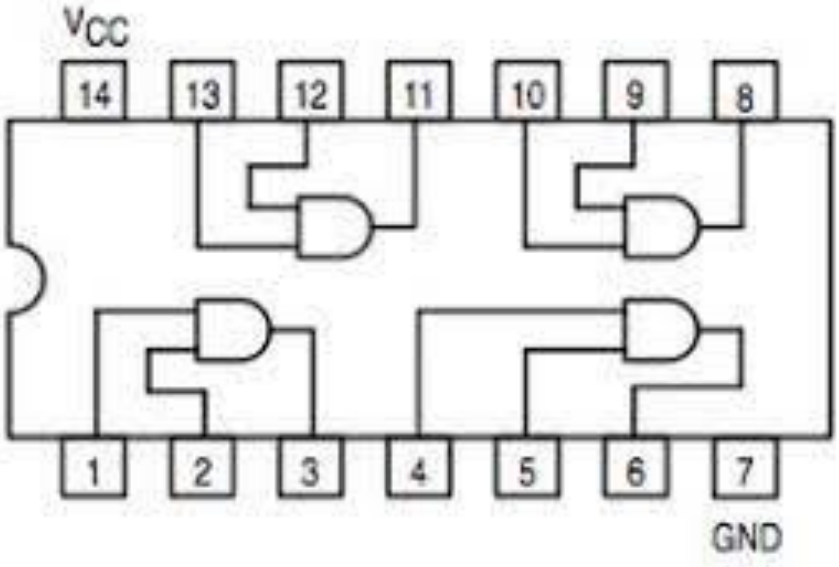


AND

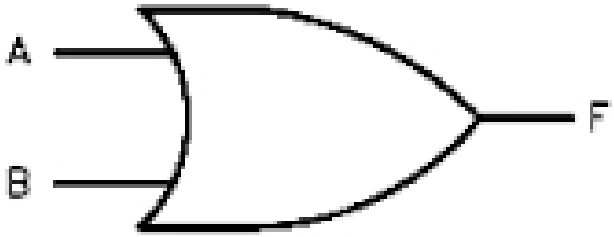
2 - input AND gate



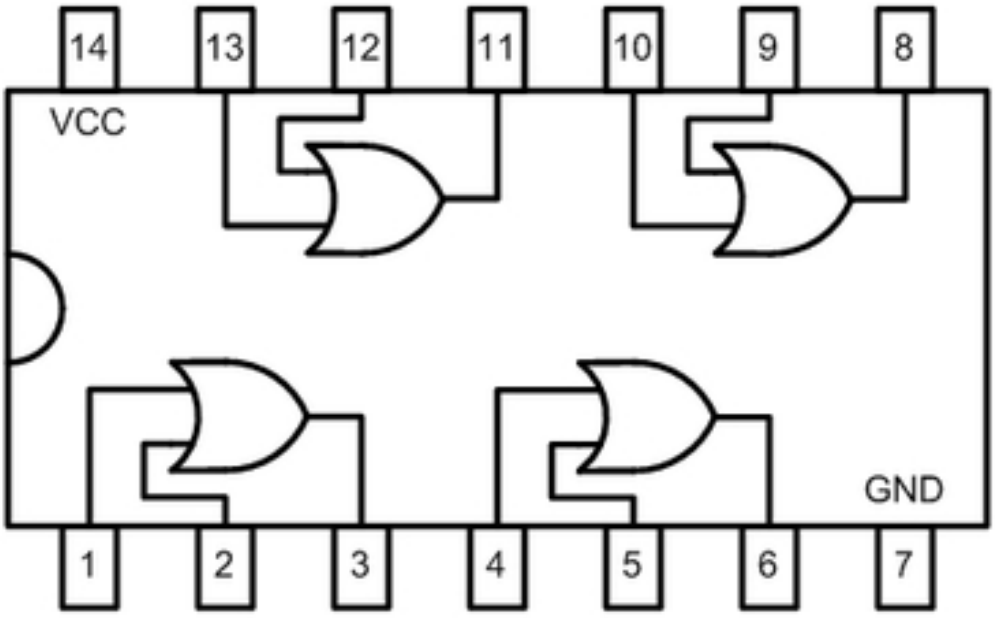
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



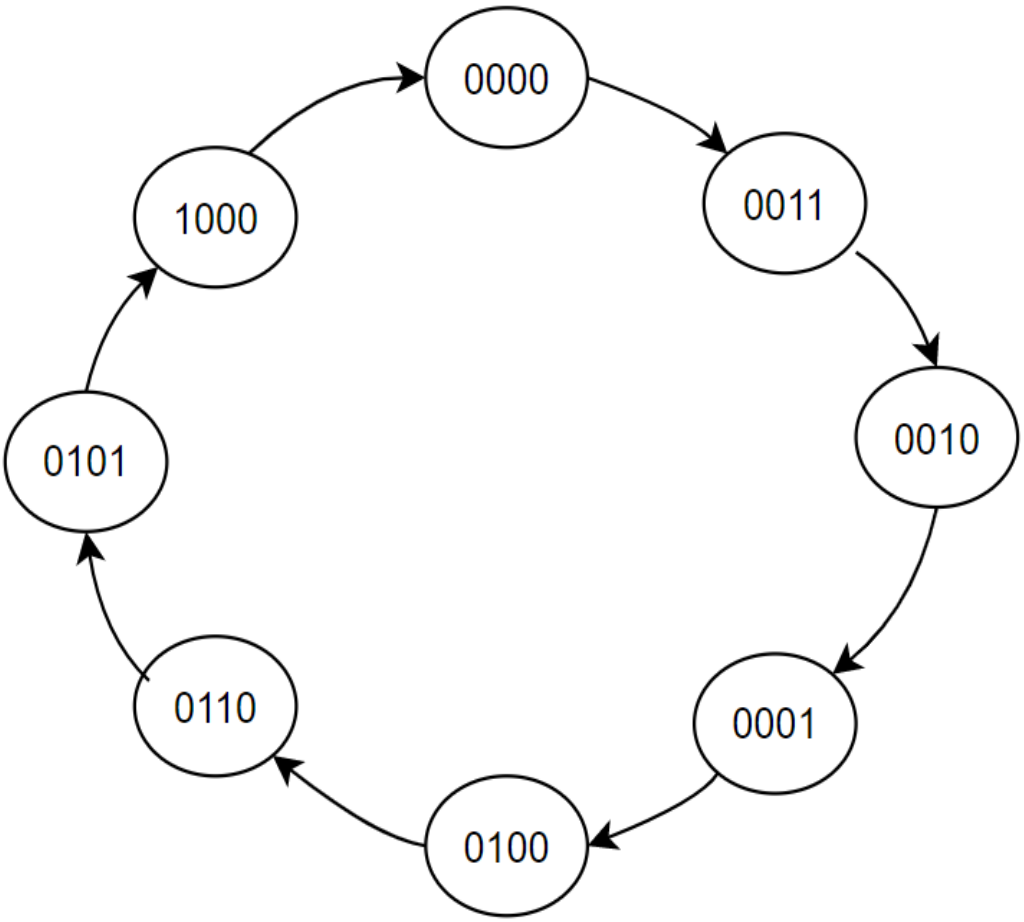
OR



INPUT		OUTPUT
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



State diagram:



State Table

A	B	C	D	A'	B'	C'	D'
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	x	x	x	x
1	0	0	0	0	0	0	0
1	0	0	1	x	x	x	x
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

Equations and k-map

1)

0	0	0	0
0	1	x	0
x	x	x	x
0	x	x	x

$$A(n+1)=BD$$

2)

0	1	0	0
1	0	x	1
x	x	x	X
0	x	x	x

$$B(n+1)=BD'+B'C'D$$

3)

1	0	1	0
1	0	x	0
x	x	x	X
0	x	x	x

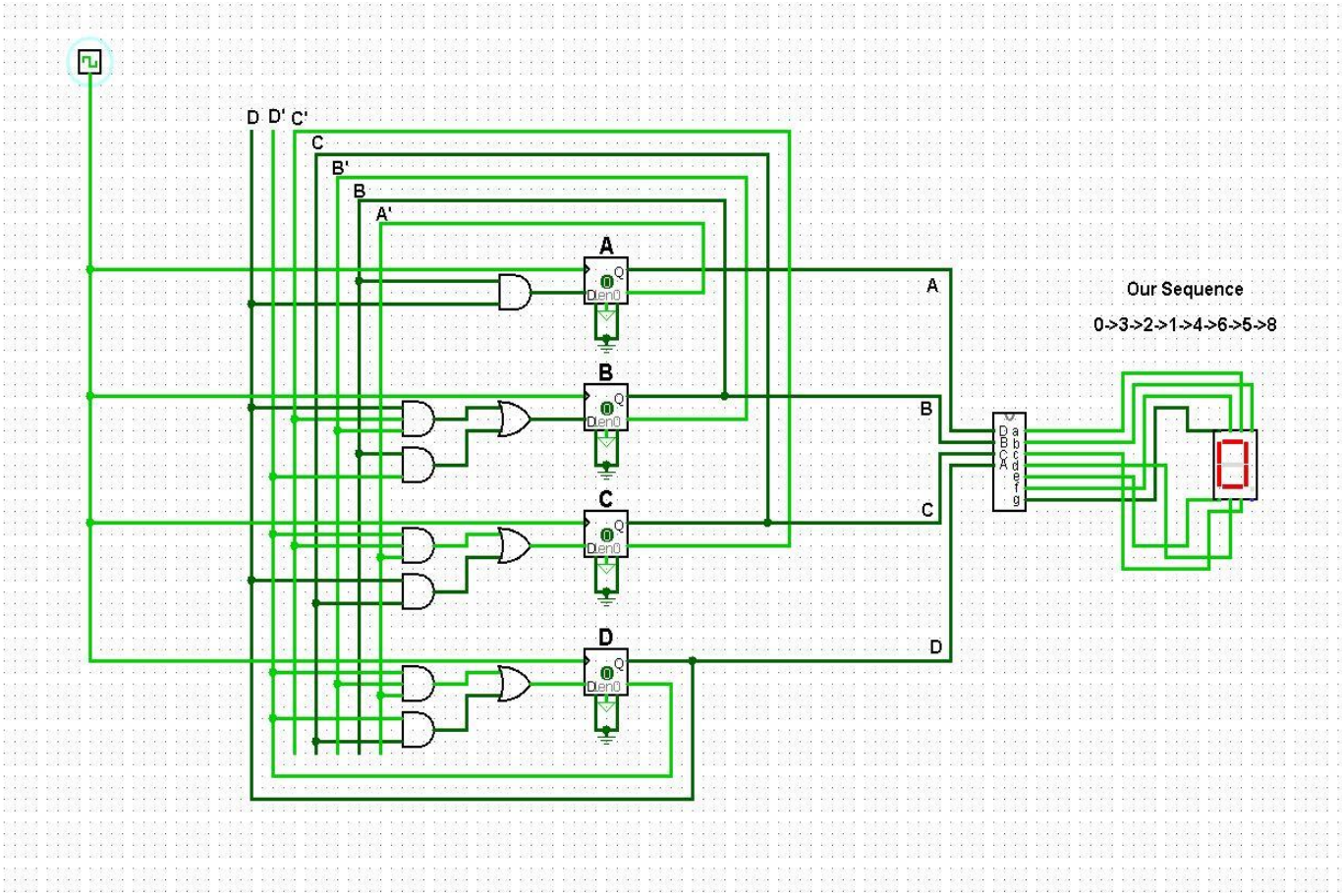
$$C(n+1)=CD+A'C'D'$$

4)

1	0	0	1
0	0	x	1
x	x	x	X
0	x	x	x

$$D(n+1)=CD'+A'B'D'$$

Circuit diagram:



Conclusion:

-Sequential circuit with sequence (0,3,2,1,4,6,5,8) was done using D FF connected by a clock to change the state from state to another. then the output was displayed on the 7-segment.