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WeFr 2-3:30pm

Fr, February 19, 6:30-8:00pm

EECS 141: SPRING 10—MIDTERM 1

NAME	Last First

SID	Solution

Last Updated on 2010/02/24

Problem 1 (15):

Problem 2 (12):

Problem 3 (15):

Total (42)	

[PROBLEM 1] CMOS NON-INVERTING BUFFER (15 pts)

The following circuit can be seemed as a “DIGITAL NON-INVERTING BUFFER”.

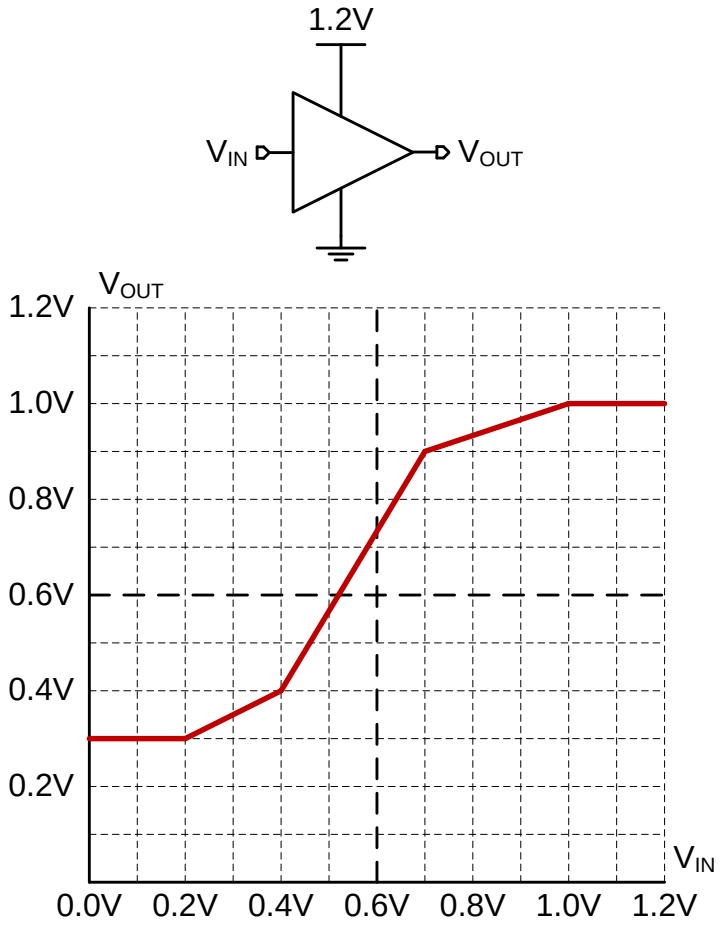


Fig.1 (a) DIGITAL BUFFER & VTC

(a) (3pts) Compute V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H.

$NM_L = V_{IL} - V_{OL} = 0.1V$
$NM_H = V_{OH} - V_{IH} = 0.3V$

(i) V_{IL}	**= 0.4V (0.5pts)**
(ii) V_{IH}	**= 0.7V (0.5pts)**
(iii) V_{OL}	**= 0.3V (0.5pts)**
(iv) V_{OH}	**= 1.0V (0.5pts)**
(v) NM_L	**= 0.1V (0.5pts)**
(vi) NM_H	**= 0.3V (0.5pts)**

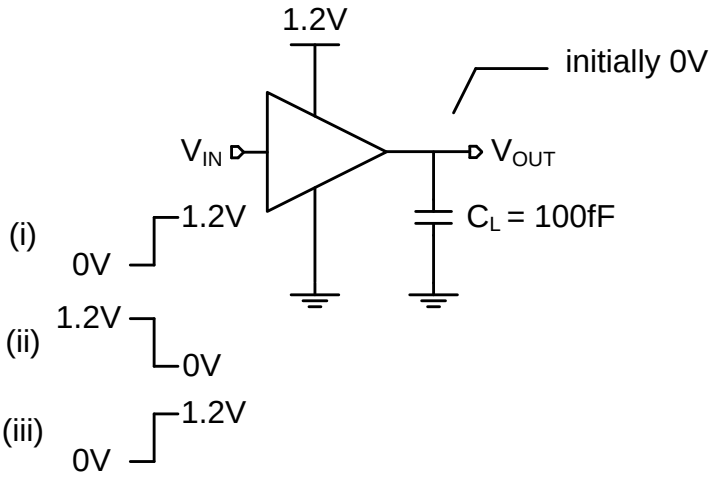


Fig.1 (b) One-stage DIGITAL BUFFER with 100fF C_L

(b) (6pts) For Fig.1.(b), the output voltage, V_{OUT}, is initially discharged, V_{OUT}=0. You may ignore the intrinsic capacitance, or diffusion capacitance, of the buffer.
Find the energy dissipated in the buffer during the first 0 to 1.2V step input (i), **First E_{DISS}**.
Then, after the output reaches its final value, a 1.2V to 0 step is applied to the input (ii). Find the energy dissipated in the buffer, **Second E_{DISS}**.
A second 0 to 1.2V step follows (iii). Find again the energy dissipated in the buffer (**Third E_{DISS}**).

i) 1^{st} $E_{DISS} = E_{SUPPLY} - E_{STORED}$, VOUT: 0V → 1.0V **(0.8pts)**
$= C_L*V_{DD}*(1.0) - ½*C_L*(1.0)^2$ **(1pts)** = 100f*(1.2-0.5) = 70fJ **(0.2pts)**

ii) 2^{nd} $E_{DISS} = E_{STORED} - E_{REMAINED}$, VOUT: 1.0V → 0.3V **(0.8pts)**
$= ½*C_L*(1.0)^2 - ½*C_L*(0.3)^2$ **(1pts)** = 50f*(1-0.09) = 45.5fJ **(0.2pts)**

iii) 3^{rd} $E_{DISS} = E_{SUPPLY} - E_{STORED}$, VOUT: 0.3V → 1.0V **(0.8pts)**
$= C_L*V_{DD}*(1.0-0.3) - ½*C_L*[(1.0)^2 - (0.3)^2]$ **(1pts)**
= 100f*1.2*0.7 – 50f*(1-0.09) = 38.5fJ **(0.2pts)**

(i) 1st E_{DISS} = 70fJ (0.2pts)

(ii) 2nd E_{DISS} = 45.5fJ (0.2pts)

(iii) 3rd E_{DISS} = 38.5fJ (0.2pts)

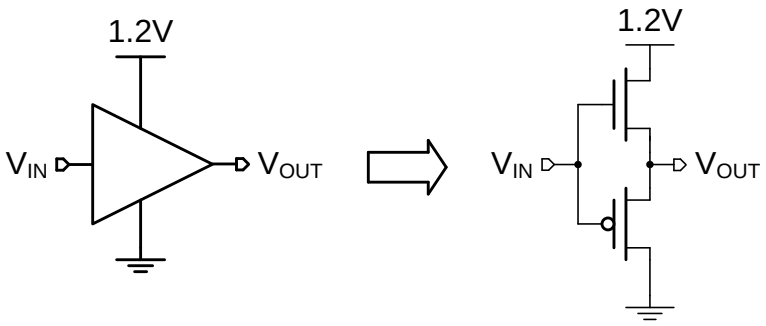
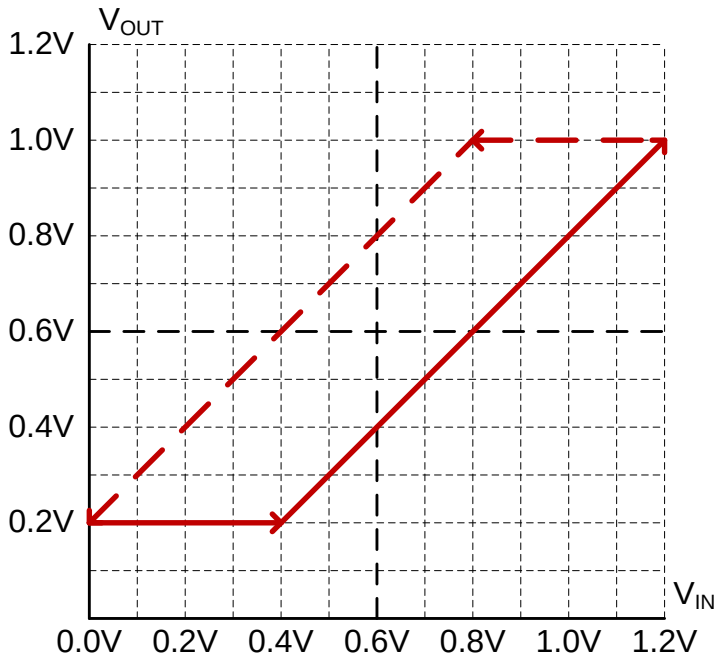


Fig.1 (c)

(c) (4 pts) One engineer tried to develop a transistor-level implementation of the buffer as shown in Fig.1(c). Draw the VTC of the circuit where VIN goes from 0V to 1.2V and then goes back to 0V. Here, the $V_{TN}=|V_{TP}|=0.2V$, R_{OFF}=inf., and no body effect, that is the threshold voltage is not dependent upon the voltage of the body.



Assume that the input is at 0 and the output is at $|V_{TP}|$. As the input is increased, the output will stay constant until the NMOS device turns on. That will occur at $V_{IN}=|V_{TP}|+V_{TN}$. The upper transistor behaves as a source follower and will pull the output along as the input rises until the output reaches $V_{DD}-V_{TN}$. However, as the input is reduced in value the output stays at its high value until the PMOS device turns on. This occurs at $V_{IN}=V_{DD}-(|V_{TP}|+V_{TN})$. Then the PMOS device acts as a source follower and the output drops linearly to $|V_{TP}|$ as the input is reduced.

VIL=0.4 (1pts), VIH=0.8 (1pts), VOL=0.2 (1pts), VOH=1.0 (1pts)

(d) (2pts) Can the gate of Fig 1.c still be considered a digital gate (or, is it still regenerative)? Explain in a couple of words why or why not.

A digital gate. **(1pts)**

The gain of the circuit is close to unity, but the circuit still has noise margin. Therefore, it has noise rejection properties. **(1pts)**

[PROBLEM 2] RING OSCILLATOR (12pts)

Consider the 5-stage ring oscillator shown in Fig.2a, which is used to generate a clock signal. The input gate capacitance of a minimum-sized inverter (size=1) is C_{IN}=10fF, while $R_{ON,N}$=$R_{ON,P}$=7.22kΩ, and R_{OFF}=inf. Assume that the input capacitance is proportional to its size, and R_{ON} is inversely proportional to its size. The diffusion capacitance, or intrinsic capacitance, of inverter is the same as the gate capacitance, γ=1. Ignore resistance and capacitance of the wires between the inverters.

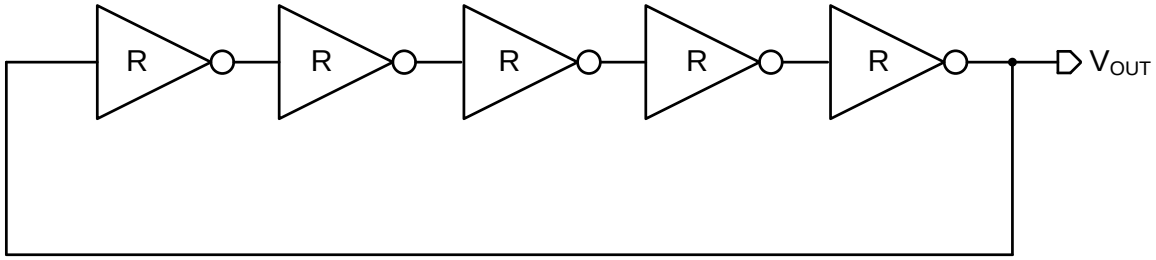
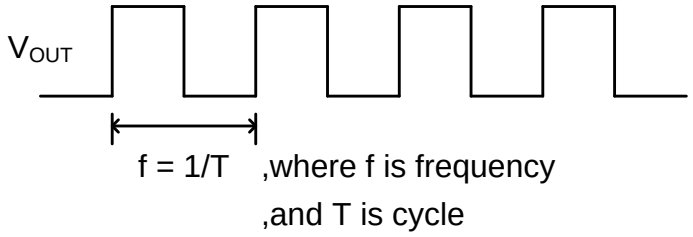
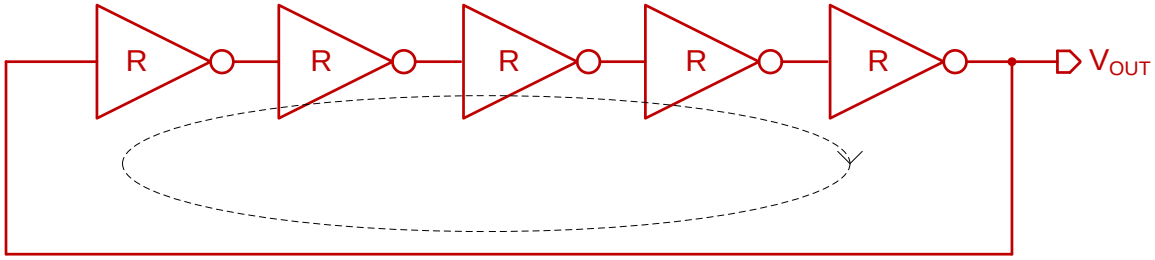


Fig.2 (a) 5-stage Ring Oscillator

(a) (6pts) Determine the oscillation frequency of this circuit at V_{OUT} for R=1 (that is, using unit inverters). Determine also the power dissipation of the circuit P_{SUPPLY} for VDD = 1.2V. You should take into account the gate and diffusion capacitances.



tinv = ln(2)*$R_{ON,MIN}$*$C_{IN,MIN}$ = ln(2)*7.22k*10f = 50.05pS ≅ 50pS **(2pts)**



Signal should turn twice of 5-stage inverter chain to make one cycle.

T= 2*5*$t_{P,INV}$ **(2pts)**= 10*tinv*(γ + f) = 10*50p*(1+1)=1nS **(0.3pts)**
F = 1/T = 1GHz

P_{SUPPLY} = C_{TOT}*VDD^2*f = 100f*1.2^2*1G = 144uW **(0.3pts)**
,where C_{TOT} = 5*(2*C_R) = 10*10f*R = 100f * R = 100fF due to R=1. **(1.4pts)**

f = 1GHz **(0.3pts)**
P_{SUPPLY} = 144uW **(0.3pts)**

(b) (6pt) Determine the oscillation frequency of ring oscillator and as well as the power dissipation, when the inverters are sized at R=2, R=4, and R=8, respectively. Please normalize your results with respect to $f_{R=1}$ and $P_{SUPPLY,R=1}$.

According to delay equation, the delay is independent of the size of inverter. So, there is no change in cycle even if the size of inverter is changed. **(2pts)**
$T= 2*5*t_{P,INV} = 10*tinv*(\gamma + f)$ **(0.7pts)**

In terms of energy, the energy is linearly proportional to the size of inverter (R). So, the energy is increased by the size of inverter (R). **(2pts)**
$P_{SUPPLY} = C_{TOT}*VDD^2*f = 5*(2*C_R)*VDD^2*f$ **(0.7pts)**

R	$f_R / f_{R=1}$	$P_{SUPPLY,R} / P_{SUPPLY,R=1}$
2	1 (0.1pts)	2 (0.1pts)
4	1 (0.1pts)	4 (0.1pts)
8	1 (0.1pts)	8 (0.1pts)

[PROBLEM 3] COMPLEX LOGIC AND LOGICAL EFFORT (15 pts)

(a) (2pts) Implement the logic function $F = \overline{A \cdot B + C}$ by using a complex static CMOS Gate. Place the PMOS and NMOS driven by input A closest to the output node, F, in your transistor stacks.

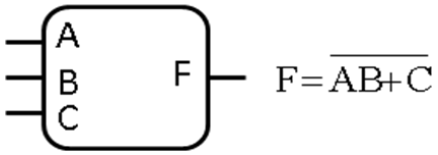
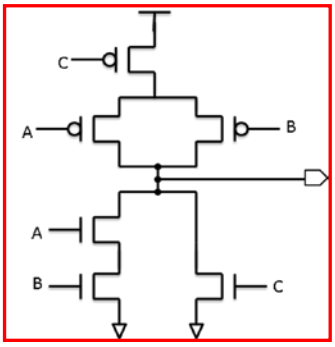


Fig.3 (a) Complex Gate



(2pts)

(b) (3pts) The unit inverter is shown in Fig. 3(b). Assume that C_D=C_G =2fF/μm. Size the *transistors of the complex gate in (a) such that the worst cast driving strength for all inputs is the same as a unit inverter. Give the width of all transistors in units of um. Determine the logical effort for each input?*

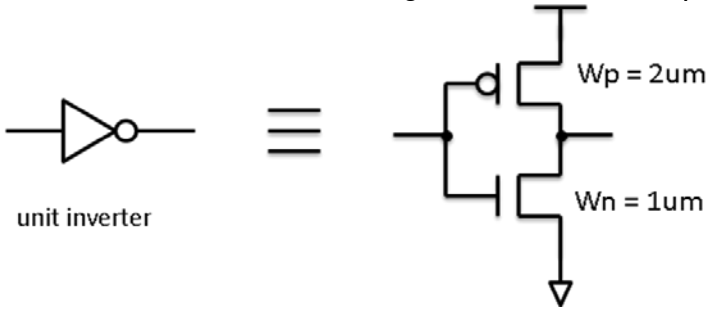
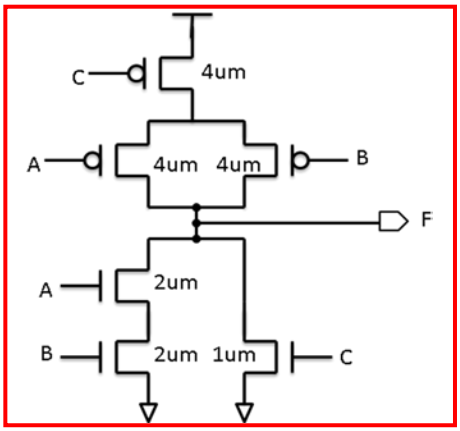


Fig.3 (b) Unit Inverter



Sizes of all transistors:
(In units of um)

$W_{pA}=W_{pB}=W_{pC}=4um$	(0.5 pts)
$W_{nA}=W_{nB}=2um$	(0.5 pts)
$W_{nC}=1um$	(0.5 pts)
$LE_A= 2$	(0.5 pts)
$LE_B= 2$	(0.5 pts)
$LE_C= 5/3$	(0.5 pts)

(c) (5 pts) In Fig. 3(c), we insert two unit-sized inverters to drive input A of the complex gate. For the complex gate, use the sizes of transistors that you derived in (b). Assume that $C_D=C_G$ =2fF/μm. The delay, Td1, measured from ***In*** to ***X*** is 40ps. What is the delay, Td2, measured from ***In*** to ***Y***?

(Note: If you don't know the answer for (a) and (b), replace the complex gate with a 3-input NOR gate, $F=\overline{A+B+C}$*. Size the transistors of 3-input NOR gate such that the worst cast driving strength for all inputs is the same as a unit inverter.)*

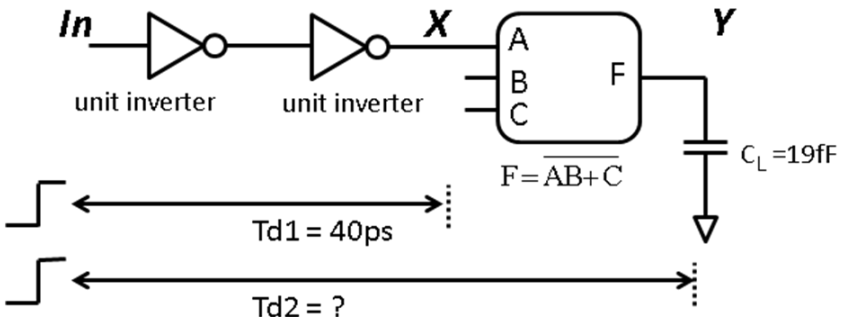


Fig.3 (c) Delay of the Complex Gate

Solution:

$$Td1 = t_{inv}\left[(1+\frac{C_{ginv2}}{C_{ginv1}})+(1+\frac{C_{gComplex,inputA}}{C_{ginv2}})\right] = t_{inv}\left[(1+\frac{6\,fF}{6\,fF})+(1+\frac{12\,fF}{6\,fF})\right] = 5t_{inv}$$ **(2 pts)**

$$Td2 = t_{inv}\left[(1+\frac{C_{ginv2}}{C_{ginv1}})+(1+\frac{C_{gComplex,inputA}}{C_{ginv2}})+(p+LE\frac{C_L}{C_{gComplex,inputA}})\right]$$ **(2 pts)**

$$= t_{inv}\left[(1+\frac{6\,fF}{6\,fF})+(1+\frac{12\,fF}{6\,fF})+(\frac{22\,fF}{6\,fF}+2\cdot\frac{19\,fF}{12\,fF})\right] = 11.83t_{inv}$$

$$\frac{Td2}{Td1} = \frac{Td2}{40\,ps} = \frac{11.83t_{inv}}{5t_{inv}} \rightarrow t_{inv} = 8\,ps$$

$$\Rightarrow Td2 = 94.67\,ps$$ **(1 pt)**

Td2= 94.67ps

(d) (5pts) The complex gate that you designed in (a) is used in the critical path of the logical network shown in Fig. 3(d). Assume that C_D=C_G =2fF/μm. What is the total path effort from In to Out? In order to minimize the delay, what should the effective fan-out per stage for this chain of gates be?

(Note: If you don't know the answer in (a) and (b), replace the complex gate with a 3-input NOR gate, $F = \overline{A + B + C}$*.)*

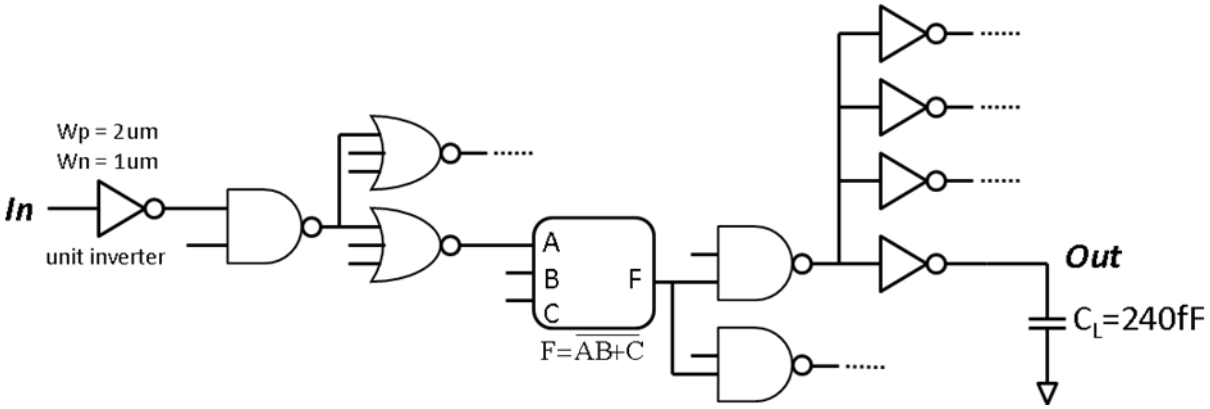


Fig.3 (d) Critical Path of Combinational Logic

Solution:

$$\prod LE = 1 \times (\frac{4}{3}) \times (\frac{7}{3}) \times 2 \times (\frac{4}{3}) \times 1 = \frac{224}{27} = 8.296$$ **(1 pt)**

$$\prod B = 1 \times 1 \times 2 \times 1 \times 2 \times 4 = 16$$ **(1 pt)**

$$F = \frac{C_L}{C_{in}} = \frac{240\,fF}{(\frac{2\,fF}{um})(2um + 1um)} = 40$$ **(1 pt)**

Path Effort: $PE = (\prod LE)(\prod B)F = \frac{224}{27} \times 8 \times 40 = \frac{143360}{27} = 5039.63$ **(1 pt)**

Effective Fan-out: $EF = \sqrt[N]{PE} = \sqrt[6]{5039.63} = 4.18$ **(1 pt)**

PE = 5039.63

EF = 4.18