1. Write a boolean expression that realizes the following truth table with inputs A and B and output Y (XNOR):

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Use sum of products

$Y =$ $\bar{A}\cdot\bar{B} + A\cdot B$

10 pts.
2

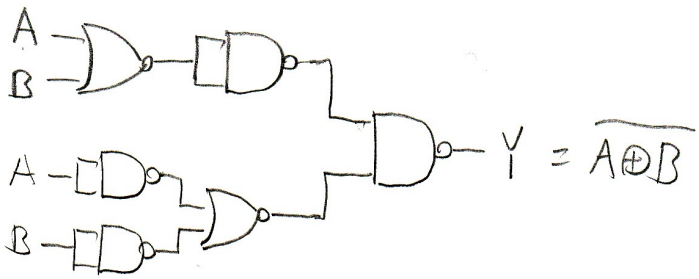
Implement this expression using only NAND and NOR gates.

$\bar{A}\cdot\bar{B} + A\cdot B = \overline{A+B} + (\overline{\bar{A}+\bar{B}})$ from Demorgan's Laws.

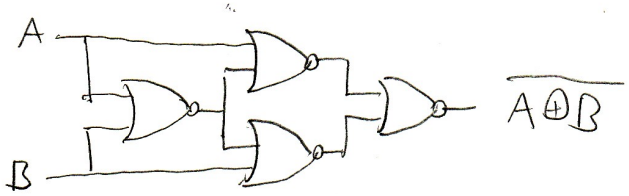
$= \overline{(\overline{A+B})\cdot(\overline{\bar{A}+\bar{B}})}$

↑ inverter using NAND gate.

15 pts.
3



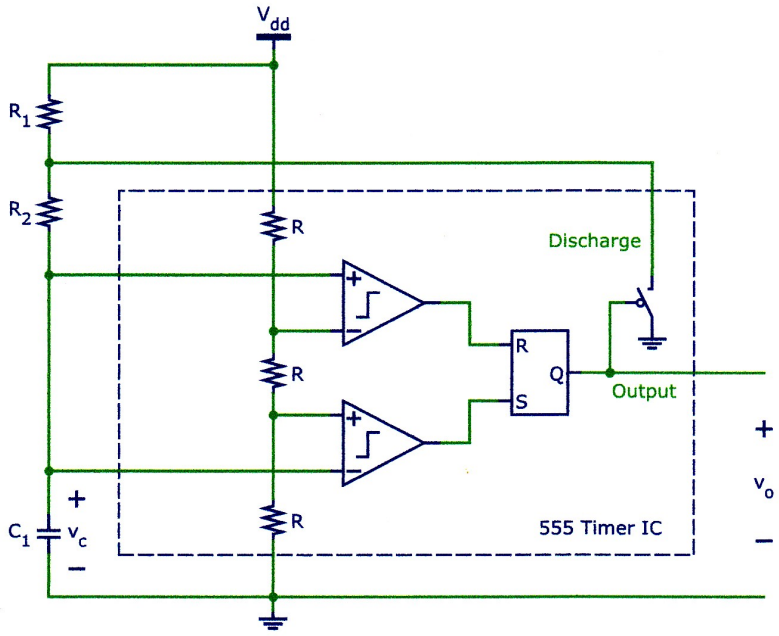
– OR –



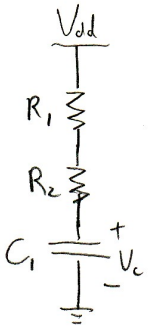
2. You are to design the clock circuit for a microprocessor with target frequency f_s using the 555 timer based circuit shown below. Use $V_{dd} = 2.7\,\text{V}$ and $R_1 = R_2 = 2\,\text{k}\Omega$.

   Find the value of C_1 such that $f_s = 2.1\,\text{MHz}$. Follow the approach suggested below. Show your approach.

C_1 [ ] 25 pts. 0



Charging



Charge from $\frac{1}{3}V_{dd}$ to $\frac{2}{3}V_{dd}$:

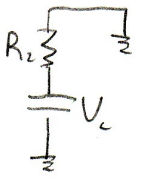
$$V_c = V_i + (V_{dd} - V_i)\cdot(1 - e^{-t/\tau})$$

$$\frac{2}{3}V_{dd} = \frac{1}{3}V_{dd} + \frac{2}{3}V_{dd}(1 - e^{-t/\tau})$$

$$e^{-t/\tau} = \frac{1}{2}$$

$$t_1 = -\tau \cdot \ln(1/2) = -C_1(R_1 + R_2)\ln\frac{1}{2}$$

Discharging



Discharge from $\frac{2}{3}V_{dd}$ to $\frac{1}{3}V_{dd}$

$$V_c = V_i e^{-t/\tau}$$

$$\frac{1}{3}V_{dd} = \frac{2}{3}V_{dd}e^{-t/\tau}$$

$$t_2 = -\tau \ln(1/2)$$

$$= -C_1 R_2 \ln(1/2)$$

$$= \frac{1}{f_s} = t_1 + t_2 \Rightarrow \frac{1}{f_s} = -C_1\left[(R_1 + R_2)\ln\frac{1}{2} + R_2 \ln\frac{1}{2}\right]$$

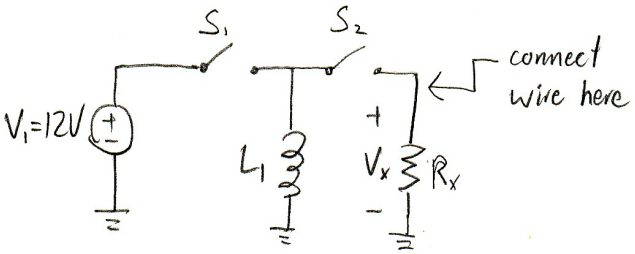
$$\Rightarrow C_1 = -\frac{1}{f_s}\left(R_1 \ln\frac{1}{2} + 2R_2 \ln\frac{1}{2}\right)^{-1}$$

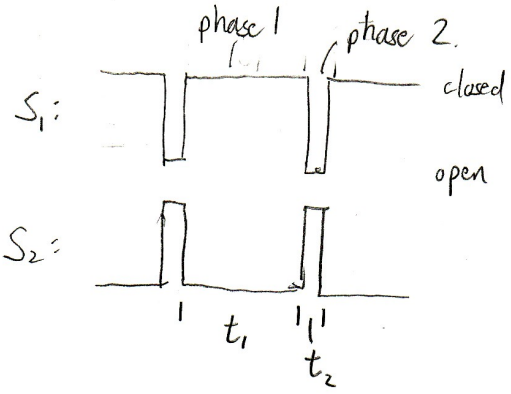
Version	Answer
1	114.5 pF
2	39.1 pF
3	56.6 pF

3. You are to design an electric fence for your cows. You have already strung a wire on poles around your property, and also made a good ground contact by burying a 3 foot long copper rod in the dirt. Using an Ohm-meter you find that the resistance between the wire and the copper rod is $R_x = 191\,\text{k}\Omega$. From the web you learned that for the cows to have respect (of the fence), you need to apply 1000 V voltage spikes between the wire and ground (spikes only).

   You have one 12 V car battery (no other source) and resistors, capacitors, inductors and switches (up to 10 of each). You also have timer circuits to control the switches, but to keep things simple you do not need to design the corresponding circuit. Just draw a timing diagram indicating for each switch when it is opened and closed.

   Design the circuit for generating the 1000 V spikes using only available parts. Show a complete circuit diagram using schematic symbols (no "artistic" pictures), and indicate where to connect the wire and copper rod. Include resistor R_x in your schematic. Determine and mark in the schematic the values for all components (show your calculations).





During phase 2, we need $V_x = 1000\,V$

$$\Rightarrow I_{L_1} = \frac{1000\,V}{R_x} = 5.24\,mA\ *$$

Inductor charges during phase 1.

$$I_{L_1} = \frac{V_1 \cdot t_1}{L_1} \Rightarrow t_1 = \frac{I_{L_1} \cdot L_1}{V_1}$$; choose $L_1 = 10\,mH$ (arbitrary reasonable value)

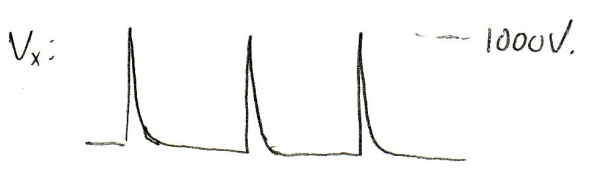
$$t_1 = \frac{10\,mH \cdot 5.24\,mA}{12\,V} = \underline{4.37\,\mu s}$$

During phase 2, inductor discharges.

$$\tau = \frac{L}{R} = 52.4\,ns.$$

choose $t_2 \gg \tau$ to ensure L_1 discharges completely.

$t_2 = \underline{1\,\mu s.}$



* Numbers differ for other versions. Approach is the same.

4. You have been hired by SnapOMatic, a fledgling startup making ultra-low power cameras. Your job is to redesign their image compression chip to use less energy.

The current solution consists of $N = 4 \times 10^6$ gates. Each gate drives an average capacitance $C_{in} = 3.4\,\text{fF}$. The image compression algorithm takes $M = 7 \times 10^6$ clock cycles (operations) per image. The activity factor, i.e. percentage of gate outputs changing in each clock cycle is $\eta = 22\,\%$. The maximum operating frequency f_s depends on the supply voltage V_{dd} and is

$$f_{s,\max} = 500\,\frac{\text{MHz}}{\text{V}^2} \times V_{dd}^2.$$

a) Calculate the time T_1 and energy E_1 required to compress one image if the processor is operating at its maximum frequency for $V_{dd} = 1\,\text{V}$.

$T_1 =$ ____ 4 pts. 1

$E_1 =$ ____ 4 pts. 2

b) The marketing department found a great opportunity for a chip that consumes only $E_x = 7.9\,\text{mJ}$ per compressed image. Calculate the operating frequency f_x and supply voltage $V_{dd,x}$ for the existing chip such that the energy per compressed image is E_x.

$f_x =$ ____ 4 pts. 3

$V_{dd,x} =$ ____ 4 pts. 4

c) Your friend who took CS61p learned about an parallelized image compression algorithm that has no overhead. What is the number of processors P needed to achieve image compression in $706\,\mu\text{s}$ and only 4.8 mJ energy per compressed image? At what frequency $f_{s,p}$ are they operating?

$P =$ ____ 5 pts. 5

$f_{s,p} =$ ____ 4 pts. 6

Ver.1 Ver 2 Ver 3.

a) $T_1 = \frac{M}{f_s} = \frac{7\times10^6}{5\times10^8 \cdot V_{dd}^2} = \{14\text{ms},\ 12\text{ms},\ 10\text{ms}\}$ //

$E_1 = \frac{1}{2} NCV_{dd}^2 \cdot M \cdot \eta = \{10.5\text{mJ},\ 26.5\text{mJ},\ 24.2\text{mJ}\}$ //

b) $V_{dd} = \sqrt{\frac{2E}{NCM\eta}} = \{0.869\text{V},\ 0.592\text{V},\ 0.614\text{V}\}$ //

$f_{s,max} = 500\text{MHz} \cdot V_{dd}^2 = \{378\text{MHz},\ 175\text{MHz},\ 188\text{MHz}\}$ //

c) $E = \frac{1}{2} NC V_{dd}^2 M\eta$; this is the same regardless of # processors.

Find V_{dd}:

$V_{dd} = \sqrt{\frac{2E}{NCM\eta}} = \{0.677\text{V},\ 0.596\text{V},\ 0.265\text{V}\}$

$f_{sp} = 500\text{MHz} \cdot V_{dd}^2 = \{229\text{MHz},\ 178\text{MHz},\ 35.1\text{MHz}\}$ //

$P = \frac{M/t}{f_{sp}} = \{44, 74, 260\}$ //