## UNIVERSITY OF CALIFORNIA

College of Engineering

Department of Electrical Engineering and Computer Sciences

		Days / Time	
LAB SECTION	:		
NAME: (print)	Last	First	Student ID#
NIAME	KEY	FINAL EXAMINATION Time allotted: 110 minutes	
EE40 Summer 09		SULUTIONS	Frank Liac

I acknowledge that the UC rules on academic honesty apply.

Signature

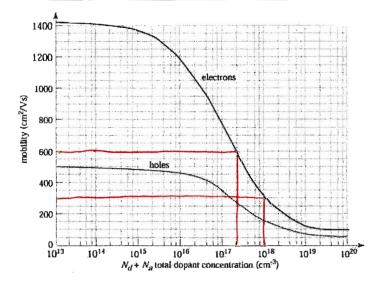
#### **INSTRUCTIONS:**

- 1. SHOW YOUR WORK. Partial credit will be given only if your methods are clear to the grader.
- 2. Clearly mark (BOX or UNDERLINE) your answers.
- 3. Specify the units on answers whenever appropriate. Points will be deducted for missing units.
- 4. Closed book, closed notes. You are allowed THREE 8.5" x 11" sheet of notes. Calculators are allowed.

## PHYSICAL CONSTANTS

<u>Description</u>	<u>Symbol</u>	<u>Value</u>	PROPERTIES OF S	ILICON A	AT 300K
Electronic charge	q	1.6×10 <sup>-19</sup> C	<u>Description</u>	<u>Symbol</u>	$10^{10}  \mathrm{cm}^{-3}$
Boltzmann's constant	$\boldsymbol{k}$	$8.62 \times 10^{-5} \text{ eV/K}$	Intrinsic carrier concentration	$n_{\rm i}$	
Thermal voltage at 300K	$V_{\rm T} = kT/q$	0.026 V	Dielectric permittivity	$\mathcal{E}_{\mathrm{Si}}$	1.0×10 <sup>-12</sup> F/cm

## Electron and Hole Mobilities in Silicon at 300K



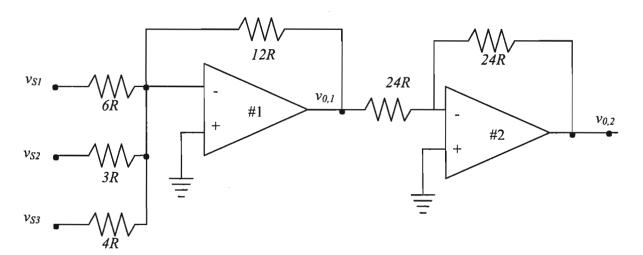
SCORE:	1	/ 8
	2	/ 28
	3	/ 40
	4	/ 34
	5	/ 28
	6	/ 12
то	 TAL:	/ 150



#### **Problem 1** [8 points]: Multiple Choice Questions

Select only ONE choice. No credit will be given to multiple answers.

a) What function does the following circuit implement? [4 pts]



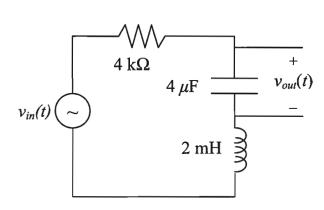
a) 
$$v_{o,2} = 12v_{s1} + 6v_{s2} + 8v_{s3}$$

c) 
$$v_{o,2} = -\frac{1}{2}v_{s1} - \frac{1}{4}v_{s2} - \frac{1}{3}v_{s3}$$

$$(b) v_{0,2} = 2v_{s1} + 4v_{s2} + 3v_{s3}$$

d) 
$$v_{o,2} = \frac{1}{2}v_{s1} + \frac{1}{4}v_{s2} + \frac{1}{3}v_{s3}$$

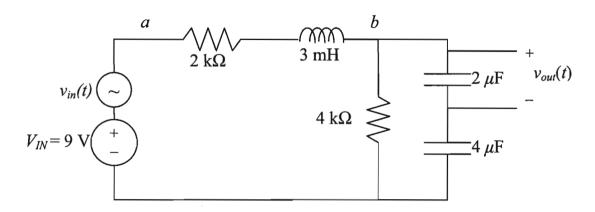
- 2) Consider the circuit below on the left:
- a) What is the resonant frequency of this circuit? [2 pts]
- a) 62.5 rad/s
- (b)  $11.2 \times 10^3 \text{ rad/s}$
- c)  $2 \times 10^6$  rad/s
- d)  $125 \times 10^6 \text{ rad/s}$
- b) What is the natural response of this circuit? [2 pts]
- a) Underdamped
- b) Critically Damped
- c) Overdamped

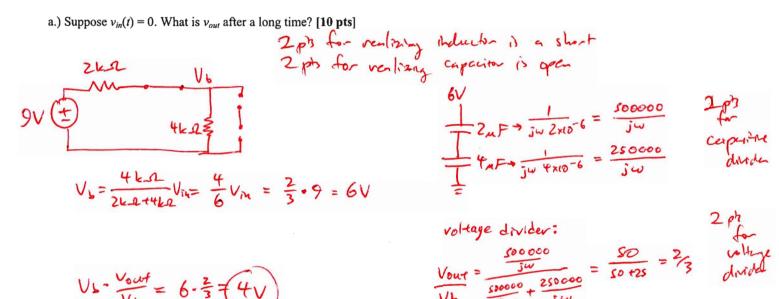


EE 40 Final Exam

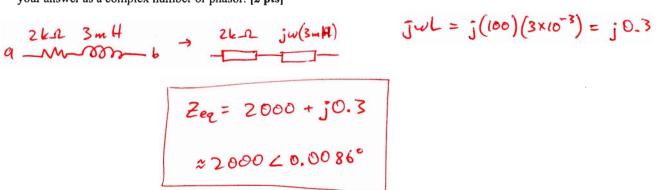
## Problem 2 [28 points]: Phasor Analysis

Consider the circuit below:





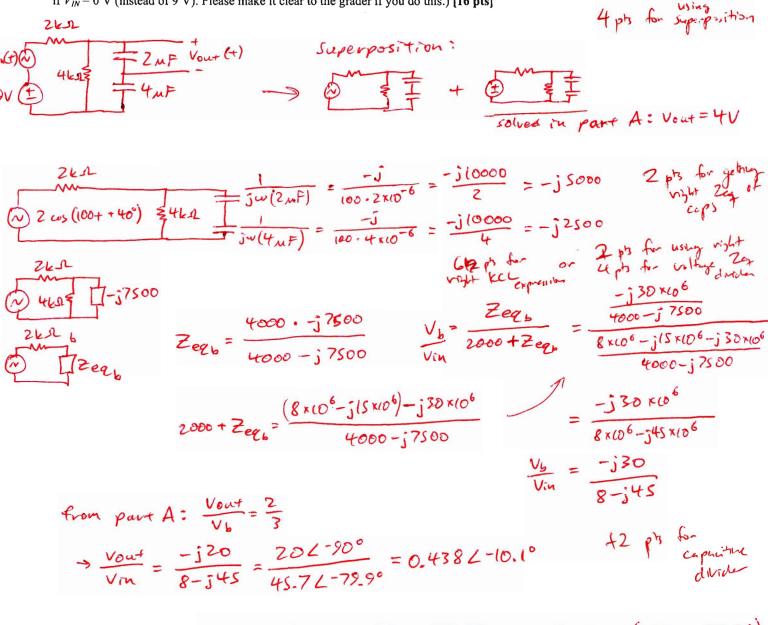
b.) If the angular frequency,  $\omega = 100$  rad/s, what is the equivalent impedance,  $\mathbf{Z}_{eq}$ , between nodes a and b? You may express your answer as a complex number or phasor. [2 pts]



#### EE 40 Final Exam

c.) To simplify the math in this part, assume that  $Z_{eq} = 2 k\Omega$ , (with no imaginary part). This is the  $Z_{eq}$  between nodes a and b (from part (b).

If  $v_{in}(t) = 2 \cos(100 t + 40^{\circ})$  and  $V_{IN} = 9 \text{ V}$ , what is  $v_{out}(t)$  in cosine form? (Note: for partial credit, find  $v_{out}(t)$  (in cosine form) if  $V_{IN} = 0 \text{ V}$  (instead of 9 V). Please make it clear to the grader if you do this.) [16 pts]

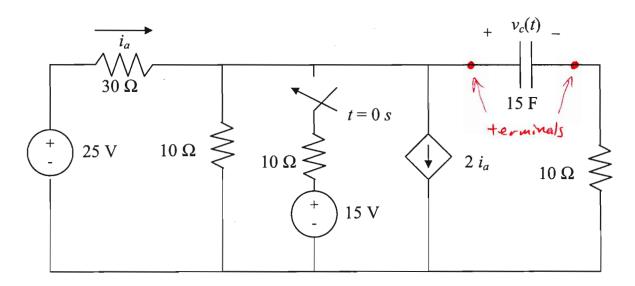


# LUTIONS

#### EE 40 Final Exam

#### Problem 3 [40 points]: First-Order Transients

Consider the circuit below. The switch has been open for a long time and then it is closed at 0 s.



a.) What is the time constant,  $\tau$ , of the circuit for  $t \ge 0$  s? (Note: because of the dependent source, you cannot use the equivalent resistance method of finding Req.) There is more space for work on the following page. [16 pts]

This can be done by either finding Vow and Isc at the terminals, & or zeroing all independent sources and applying a test voltage. 2 pm for decempting powers This is the first option.

 $i_a = \frac{2S - V_{oc}}{30}$ 1) 2ia Voc -ia + Voc + Voc - 15 + 2ia = 0

 $\frac{V_{0c}-2S}{20} + \frac{V_{0c}}{10} + \frac{V_{0c}-1S}{10} + \frac{2S-V_{0c}}{10} = 0$ 

 $ia = \frac{2S - V_{\chi}}{3D}$   $5V_{0c} - 2D = 0$ Voc = 20 = 4 V

$$8V_{x} = 20$$

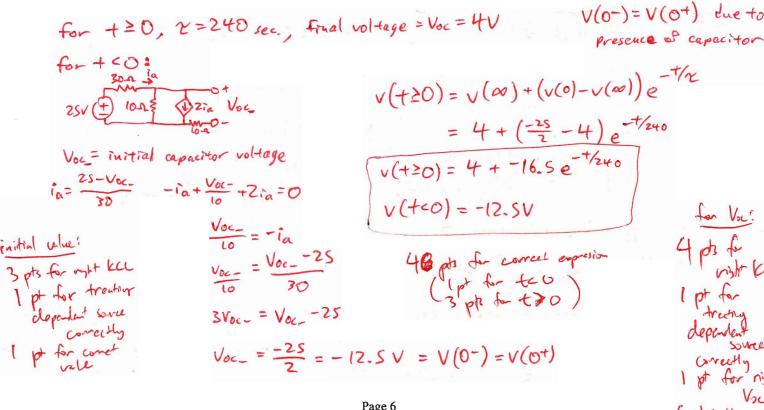
$$V_{x} = \frac{20}{8} = \frac{5}{2}$$

$$T_{sc} = \frac{V_{x}}{10} = \frac{1}{4}$$
Page 5

Req = 
$$\frac{V_{oc}}{T_{sc}} = 16\Omega$$
 Reg  $V = R_{eq}C = 16.15 = 240 \text{ sec}$ 

More space for part (a). Be sure to clearly indicate your final answer:

b.) Find the expression for  $v_c(t)$  (piecewise expressions are acceptable) for all values of t. Write your final in the box on the next page. [15 pts]

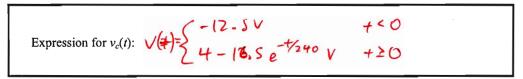


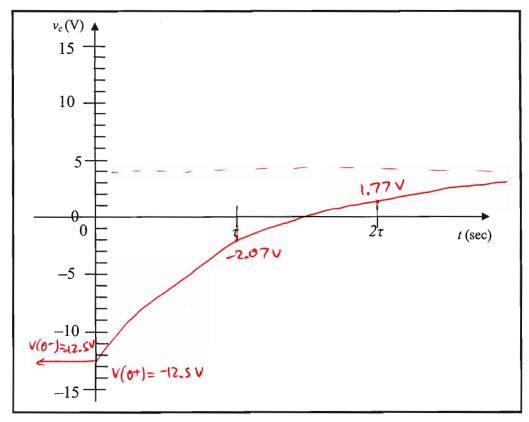
Page 6

## EE 40 Final Exam

c.) Plot  $v_c(t)$  for  $t \ge 0$  s. Label the values of  $v_c(0^-)$ ,  $v_c(0^+)$ ,  $v_c(t=\tau)$  and  $v_c(t=2\tau)$ ; be consistent with the given axes. [9 pts]

Answer:





2 pts for shipe

2 pts for veloi

3 pts for equality

veloi) to

velot)



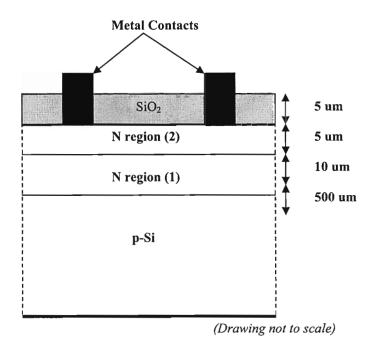
#### <u>Problem 4</u> [36 points]: Doping and Resistivity (You too can play with semiconductors!)

Suppose you decide to have fun with some fabrication equipment you purchased on eBay and set up in your garage.

a) You purchase some p-type wafers with a background concentration of  $10^{15}$  cm<sup>-3</sup>. On top of the p background, you use an ion gun to dope a region with a donor concentration of  $2x10^{17}$  cm<sup>-3</sup> and a depth of  $15 \mu m$ . Using the ion gun is so fun, that you dope again on top of the new n region with a donor concentration of  $8x10^{17}$  cm<sup>-3</sup> and a depth of  $5 \mu m$ . What is this doping step usually called in a typical fabrication process? (It's two words.) [2 pts]



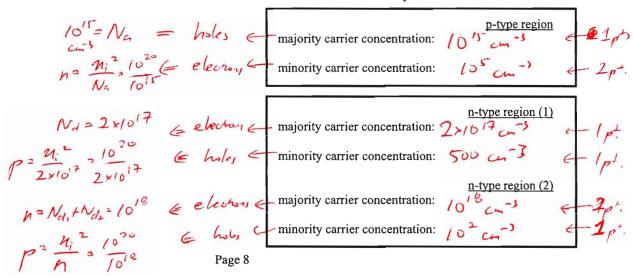
Next, silicon oxide is deposited on top of the substrate and then selectively etched to create openings for the metal contacts. After that, metal contacts are then deposited. Your final cross section is shown here:

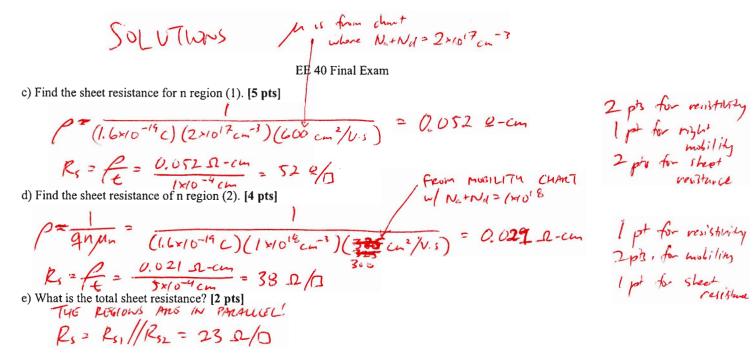


You would like to use this structure as a resistor.

b) Find the majority and minority carrier concentration for all three regions. [8 pts]

Write your answers here:

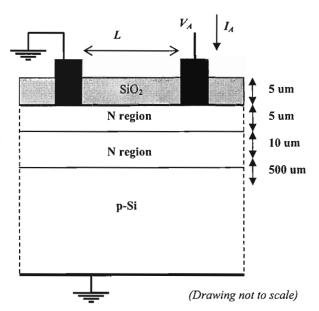




For the rest of the problem, assume your total sheet resistance from part (e),  $R_s$  is equal to 5  $\Omega$ /square. To test your resistor, you apply a bias,  $V_A$ , between the two metal contacts and according to common practice, you also connect the p-type substrate to ground. See the figure below. (Note: T = 300 K.)

f) If the length, L, between the contacts is 50  $\mu$ m and the width, W, (going into and out of the paper) of this entire region is 10  $\mu$ m, what is the current  $I_A$ for the following values of  $V_A$ V? (Follow the sign convention given in the figure.) [3 pts]

$V_A$	$I_A$
0.1 V	4 mA
0.5 V	20 mA
−0.5 V	-20 mA



j) You notice at a negative bias of -1 V, you measure large amounts of negative current, I<sub>d</sub>. Please explain what is happening. Be as specific as possible. [6 pts] WHEN VA <-0.7 V the WE HAVE FORMED A PN JUNCTION. pur junction turns on, causing large amounts of current in formed bins. (this corresponds to k) You also notice for large positive values of  $V_A$ , you measure large amounts of positive current,  $I_A$ . Please explain what is happening. Be as specific as possible. [4 pts] FOR LAKERS POSITIVE VALUES OF VA! THE PN JUNCTION IS IN REVENSE BIAS, THE CARTS CURRENT COMPS From REVERS BREAKOUN, MUST CITELY
Page 9

ENALANCHE.



#### Problem 4 [28 points]: MOSFET Behavior

In two tables below, label the region of operation and the find the drain current based on the information given. Ignore channel-length modulation. Definitions: (1) If  $V_{GS} = V_T$ , then the MOSFET is off. (2) If  $V_{DS} = V_{DSsat}$ , then the FET is in velocity saturation.

#### For NMOS Transistor:

 $\mu_n C_{ox} = 100 \,\mu\text{A/V}^2$ ;  $C_{ox} = 0.345 \,\mu\text{F/cm}^2$ ,  $v_{sat} = 8 \,\text{x} \cdot 10^6 \,\text{cm/s}$ ,  $\lambda = 0$ 

$V_T(V)$	V <sub>DSsat</sub> (V) (velocity	<i>W/L</i> (μm/μm)	V <sub>S</sub> (V)	$V_D(V)$	$V_G(V)$	Region of Operation	$I_{D}(A)$	9 Sihee	Vos 27	V= Vosat
0.5	saturation)	20/0.25	0	. 1	1	velocity	2.76 nA			
0.5	1	20/0.23	0	1	1	Saturation	2 7021			
0.5	1	20/0.25	0.3	1	1	January,	Aسر ۱۵۵			
0.3	0.5	10/0.1	0.3	0.4	1	lihear	350 MA			
0.3	0.5	10/0.1	0.2	1.5	1.5	velocity	2.76 mA			

Space for work: (Recommended for partial credit) (More space available on the next page.)  $V_{OS} = (.3 \text{ V} > V_{OS} + V_{OS}$ 

SATURATION: ID = 2 / Macox (Vcs - Vr)2

LINEAR: Is= Wm Cor (VGS-V7-V) Vos

#### For PMOS Transistor:

 $\mu_p C_{ox} = 50 \ \mu\text{A/V}^2$ ;  $C_{ox} = 0.345 \ \mu\text{F/cm}^2$ ,  $v_{sat} = 6 \ \text{x} \cdot 10^6 \ \text{cm/s}$ ,  $\lambda = 0$ 

.,						
$V_T(V)$	V <sub>DSsat</sub> (V) (velocity saturation)	W/L (μm/μm)	$V_S(V)$	$V_D(V)$	$V_G(V)$	Region of $I_D(A)$ Operation
-0.75	-1	20/0.25	0	1	2	OFF OA
-0.75	-1	20/0.25	1	0.5	0	SATURATION -125 LA
-0.3	-0.5	10/0.1	1.25	1	0.5	LINEAR -406 LA
-0.3	-0.5	10/0.1	2	1	0	SATURATION - 3, 52 mA

- Vo = 2V! (NOT -2V)

Space for work: (Recommended for partial credit) (More space available on the next page.)

VELOUTY STURMAROW: Io= WCom (Vss-Vt) Vsat

SATIMATION! To == (1/c,-VT)2

LINEAN! ID= - W/ Con (1Vcs-V-1-1/25/)(1Vos)

EE 40 Final Exam

Additional work space: (Recommended for partial credit)
Please make your methods clear to the grader if you use this space.

## Problem 5 [12 points]: EE Technology

Ť	F	Moore's Law describes the phenomenon where the number of transistors on a computer chip doubles every 1.5 to 2 years.
T	F	Any linear circuit can be reduced to an equivalent circuit comprising a current source with a parallel resistance.
<b>(</b>	F	A good voltage source should have a small series resistance.
T	F	A good current source should have a small parallel resistance.
T	<b>(F)</b>	SPICE is capable of solving voltages and currents in an electric circuit, but it cannot generate Bode plots.
Т	F	Decreasing the equivalent resistance, $R_{eq}$ , of a transistor in a logic gate will decrease the time delay, $\tau$ , of that logic gate, but will increase its dynamic power consumption. (Assume the clock frequency, $f$ , doesn't change.)

This page left blank. (If you use this page for extra work and want partial credit, please make that very clear to the grader.)