University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

J. Rabaey

WeFr 2-3:30pm

We, April 7, 6:30-8:00pm

EECS 141: SPRING 10—MIDTERM 2

NAME	Last First

SID	Solution

Problem 1 (10):

Problem 2 (12):

Problem 3 (12):

Total (34)	

MAKE SURE TO SHOW REASONINGS and DERIVATIONS.
A NUMERIC ANSWER ONLY DOES NOT SUFFICE!

[PROBLEM 1] COMPLEX LOGIC (10 pts)

(a) **(1 pts)** What is the logic function of the circuit shown below?

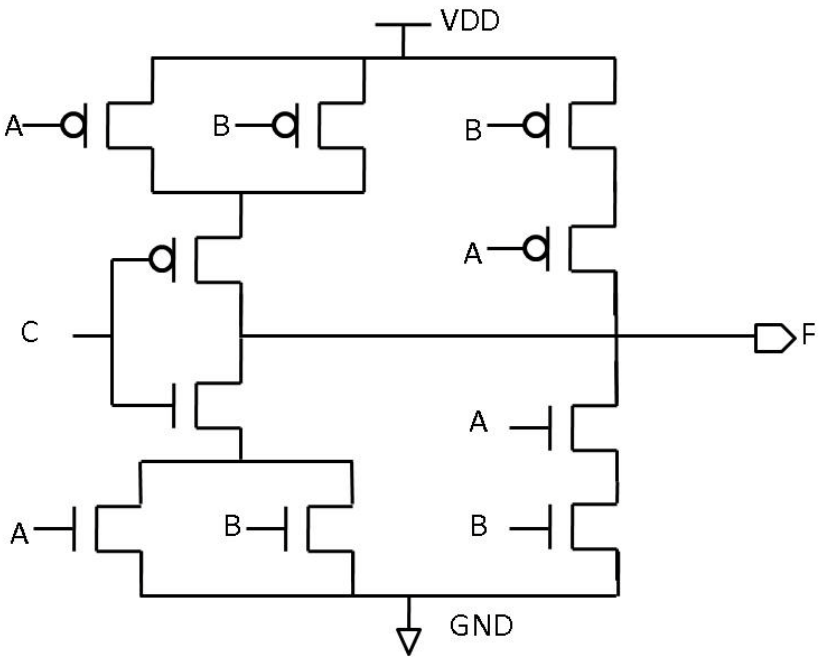


Fig.1

Solution:

$$PDN = \overline{AB + C(B + A)}$$

$$\left(PUN = \overline{A}\,\overline{B} + \overline{C}(\overline{A} + \overline{B}) = \overline{A + B} + \overline{C + AB} = \overline{(A + B)C(AB)} = \overline{AB + C(B + A)}\right)$$

$$F = \overline{AB + C(B + A)}$$
$$= \overline{AB + BC + CA}$$
$$= \overline{AB + C(B + A)}$$
$$= \overline{A}\,\overline{B} + \overline{C}(\overline{A} + \overline{B})$$

(1 pt)

$$F = \overline{AB + BC + CA} = \overline{AB + C(B + A)}$$

(b) **(4 pts)** Answer the following questions regarding the circuit shown in Fig. 1.

(i) Is this a static logic gate? Why or why not?

Solution: (1 pt)
Yes. It is a static gate because the output is always connected to a low impedance path to VDD or GND.

(ii) Are the PUNs and PDNs complementary networks (that is, can I use the Euler Graph technique to drive one from the other)? Explain.

Solution: (1 pt)
No. It is not purely complementary because the PUN is not dual of PDN. You can't use Euler Graph technique to drive one from the other.

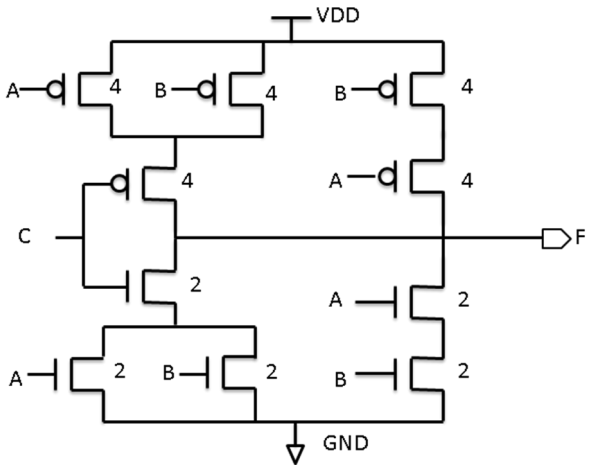
(iii) Identify the main advantage of the proposed circuit topology. Back up your answer.

Solution: (2 pts)
In comparison with pure complementary CMOS implementation, the PUN and PDN in Fig.1 are symmetrical (or mirrored). The logical effort is reduced by using this mirrored structure.

(This circuit has smaller transistors sizes in PUN because it has fewer PMOS stacks in PUN in comparison with conventional complementary CMOS implementation.)

(c) (2 pts) Size the transistors so that the worst-case driving strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What are logical efforts of the A and C inputs?

Solution:
Size the transistors:



LE_A = (4+2+4+2)/ 3 = 4 (1pt)

LE_C = (4+2)/ 3 = 2 (1pt)

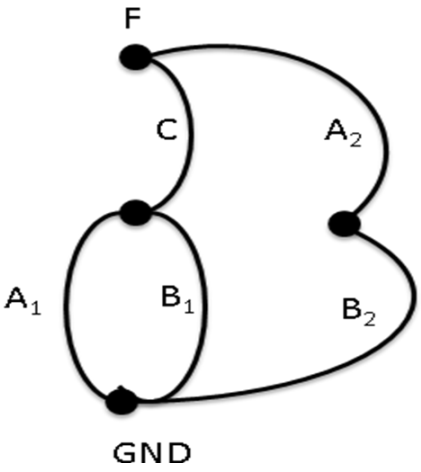
LE_A= 4
LE_C= 2

(d) **(3 pts)** Is it possible to implement this function using **single n- and p- diffusion strips**? In either case, draw the layout **stick diagram** that would lead to a small area standard cell layout.

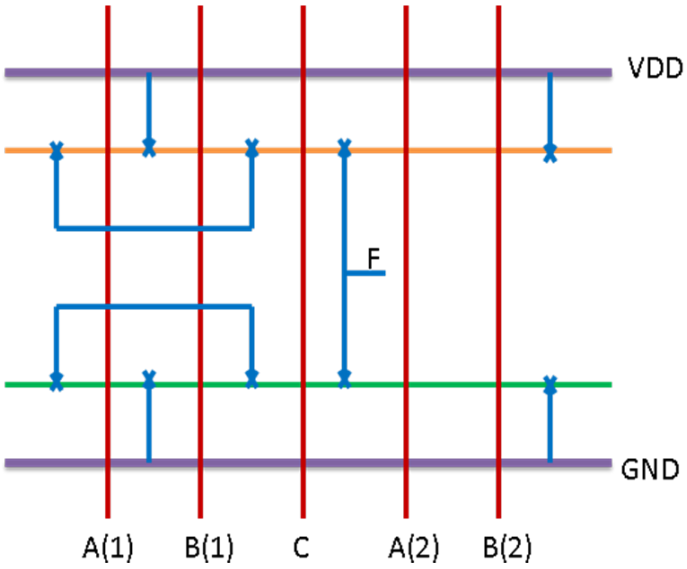
.

Solution:
Yes. PDN and PUN are symmetrical. If we can find the solution for a single n-mos diffusion strip, we can use the same solution for p-mos diffusion strip. That means we only need to find the Euler path for either PDN or PUN. (1pt)

The logic graph of PDN is shown below: (1pt)



There are many possible solutions of Euler path. For example: A_1 - B_1 – C - A_2 -B_2
The stick diagram is: (1pt)



[PROBLEM 2] PASS TRANSISTOR LOGIC (12 pts)

Consider the pass-transistor logic network of Fig. 2. The following (transistor) parameters are given: $V_{TN}=|V_{TP}|=V_T=0.3V$ and $V_{DD}=1.2V$. You may ignore body effect. **C_L= 20fF.** L of all transistors equals 0.1um. The equivalent model of the NMOS and PMOS transistors is given in the Figure as well. The model parameters can assumed to be constant and are NOT a function of biasing conditions. The nominal values for the parameters are given as: Reqn=12kΩ/□ and Reqp=24kΩ/□ (where the □ denotes the W/L ratio); and C_G=2fF/um, C_D=1fF/um (expressed as a function of the transistor width).
Consider the unit size inverter (S=1) to have the following dimensions: Wn=0.2um and Wp=0.4um.

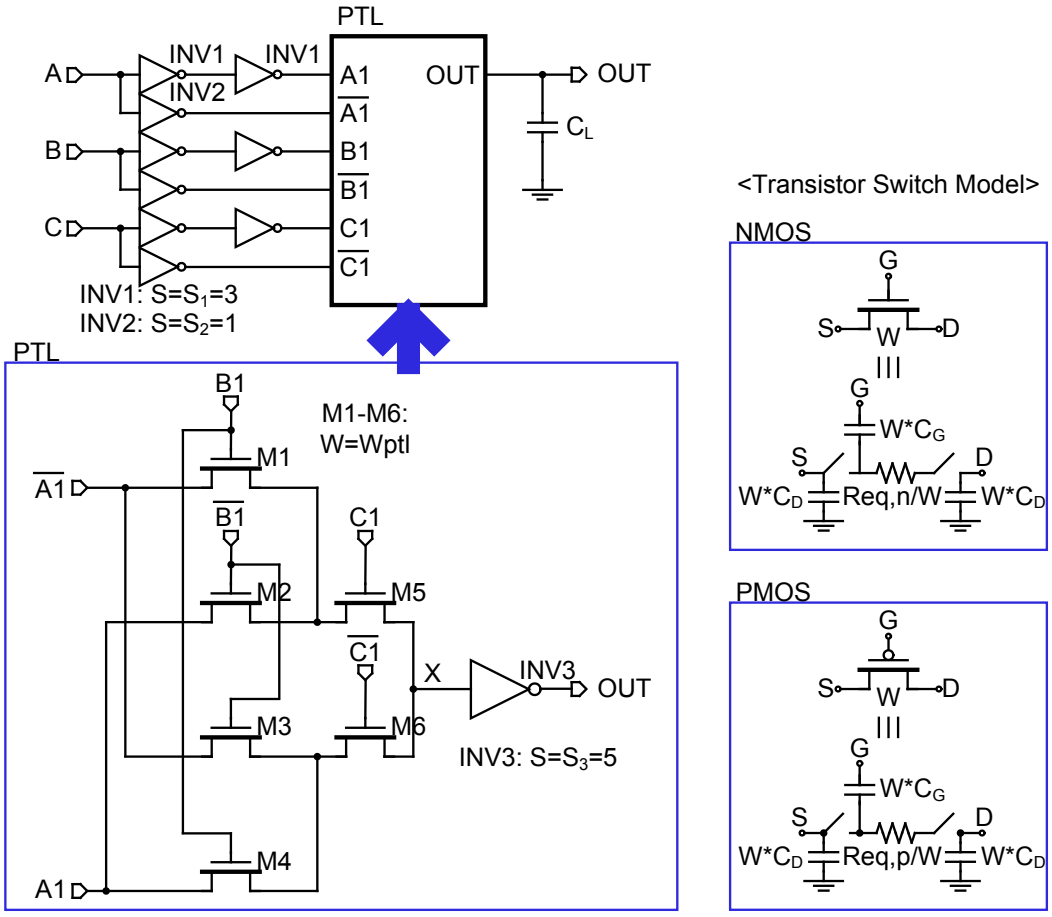


Fig.2 Pass Transistor Logic (PTL)

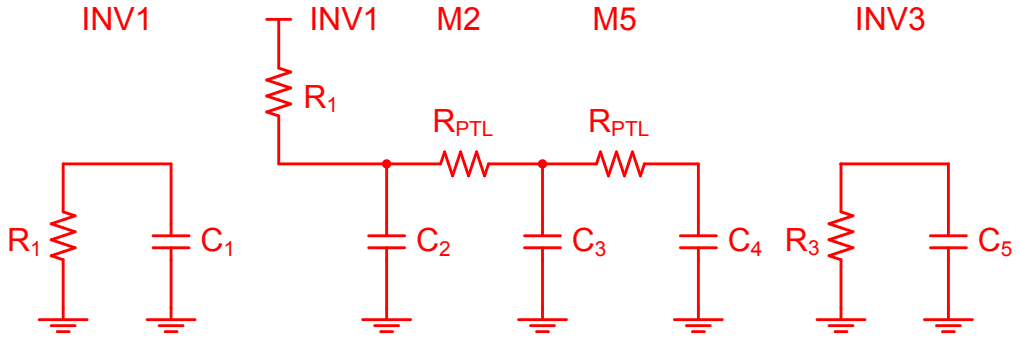
(a) **(1 pts)** What is function OUT of the circuit of Fig.2 as a function of the A, B, and C inputs?

C	B	A	OUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(0.5pts) with other proper reasoning

OUT = A ⊕ B ⊕ C (0.5pts)

(b) **(4 pts)** Assume that the critical path of the circuit of Fig.2 is from input A to OUT. For the sake of simplicity, **we decided to make all the pass-transistors (M1-M6) equal (size: Wptl)**. We now want to size these transistors so that the delay from A to OUT for a step input from 0 to V_{DD} is minimized.
Draw a **CLEAR** diagram of the critical path of the circuit with the related capacitors annotated, and provide an expression for the value of each capacitor and resistor in your diagram.



(1.0pts)

,where C1 = 3*(Wn+Wp)*(C_D + C_G)=9*(Wn+Wp)= 3*(0.2um+0.4um)*(1f + 2f) = 5.4fF **(0.5pts)**
C2 = 3*(Wn+Wp)*C_D + 2*Wptl*C_D = 1.8fF + 2fF*Wptl **(0.5pts)**
C3 = 3*1fF*Wptl + 1*2fF*Wptl = 5fF*Wptl **(0.5pts)**
C4 = 2*1fF*Wptl + 1*2fF*Wptl + (0.2um+0.4um)*5*C_G = 4fF*Wptl + 6fF **(0.5pts)**
C5 = 20fF + (0.2um+0.4um)*5*C_D = 23fF **(0.5pts)**

R1(INV1) = Reqn*L/(3*Wn) = Reqp*L/(3*Wp) = 12kΩ*0.1/(3*0.2) = 2kΩ
Rptl = 1.2kΩ/Wptl
R3(INV3) = Reqn*L/(5*Wn) = 12kΩ*0.1/(5*0.2) = 1.2kΩ **(0.5pts)**

(c) **(2 pts)** Derive an expression for the delay as a function of **Wptl** by using Elmore delay method.

τ = R1*C1 + R1*C2 + (R1+Rptl)*C3 + (R1+Rptl+Rptl)*C4 + R3*C5
= 2k*5.4f+2k*(1.8f+2f*Wptl)+(2k+1.2k/Wptl)*5f*Wptl+(2k+2*1.2k/Wptl)*(4f*Wptl+6f)+1.2k*23f
= 10.8p + 3.6p + 4p*Wptl + 10p*Wptl + 6p + 8p*Wptl + 12p + 9.6p + 14.4p/Wptl + 27.6p **(1.5pts)**

If you got wrong model in (b) but got correct time constant from your own model, it is 0.5points.

Tp = ln(2)* τ **(0.5pts)**
= 7.5p + 2.5p + 2.8p*Wptl + 6.9p*Wptl + 4.2p + 5.5p*Wptl + 8.3p + 6.7p + 10p/Wptl + 19.1p

(d) **(2 pts)** Determine the value of **Wptl** that minimizes the delay, and find that minimum delay.

If you got wrong model in (b), there is minus 0.5 points at each step.

i) $\partial Tp/\partial Wptl = 2.8p + 6.9p + 5.5p - 10p/(Wptl)^2 = 0$ **(1pts/0.5pts)**

Wptl = 1.23um

ii) $Tp = \ln(2) * \tau$ **(1pts/0.5pts)**

= 7.5p + 2.5p + 2.8p*Wptl + 6.9p*Wptl + 4.2p + 5.5p*Wptl + 8.3p + 6.7p + 10p/Wptl + 19.1p

= 7.5p + 2.5p + 2.8p*1.23 + 6.9p*1.23 + 4.2p +5.5p*1.23 + 8.3p + 6.7p + 10p/1.23 + 19.1p

= 75.13pS

If you are wrong with unit, there is minus 0.2 points.

Wptl = 1.23 um
Tp(Elmore) = 75.13pS

(e) **(3 pts)** Another approach to derive the delay of critical path and derive the optimum sizing of the pass-transistors is to use the Logical Effort approach. Explain QUALITATIVELY how you would apply this to this problem. Do you expect the result to be the same as obtained in (d)? Explain why?

i) LE approach: If you get proper procedure to get delay with LE method, you can get full credit for LE application.

Wptl=1.23um
tinv = ln(2)*Rmin*Cginv,min = ln(2)*(12k*0.1/0.2)*2f*(0.2+0.4) = 5pS

LE of PTL = Rgate*Cgate/(Rinv*Cinv) = (1/0.6+1/1.23+1/1.23) / (1/0.6) ≅ 2 **(0.5pts) – Find LE for PTL**

Branch effort is hard to get in pass transistor logic. If we think (inverter + PTL) as one stage gate to get logical effort, there is one branch at node X. At node A1, branch effort cannot be included because we considered (inverter + PTL) as one stage gate.
b = 1 @ node X

Parasitic delay of PTL is also hard to get. If we think equivalent inverter having the same pull down strength is 0.6um of PMOS and 0.3um of NMOS.
p = (1.23+1.23) / (0.3+0.6) ≅ 2.7 **(0.5pts) – Find B & P for PTL**

3-tage delay:
Tp = ∑[(LE*b*f) + γ*p]*tinv = [(1*1*1+0.5*1) + (2*1*5/3+0.5*2.7) + (1*1*20f/6f+0.5*1)]*tinv
≅ 10*tinv = 50pS
(0.5pts) – Delay equation (you should mention the number of stage at least.)

ii) Difference between Elmore delay and delay of LE
→ Two methods have different **(0.5pts)** result because there is no consideration on capacitance and branch effort inside of PTL by using logical effort method. Moreover, it is hard to get proper branch effort and parasitic delay in PTL. **(1pts)**

[PROBLEM 3] Dynamic Logic (12 pts)

In this problem, you may assume that equivalent resistances of a NMOS and PMOS are Reqn=12kΩ/□ and Reqp=24kΩ/□. C_D = C_G=2fF/um (Notice: **This is different from problem 2**). The unit inverter size is Wn=1um and Wp=2um (S=1). The L for all transistors is 0.1um .V_{TN}=|V_{TP}|=V_T=0.3V and V_{DD}=1.2V. Ignore body effect and charge sharing.

(a) (4 pts) A 2-input domino AND gate is shown below. Find the logical efforts for the first stage and second stage (LE_1 and LE_2) for both **the evaluation phase (EV) and precharge phase (PR)?** Please write down the equations of your calculation for each LE.

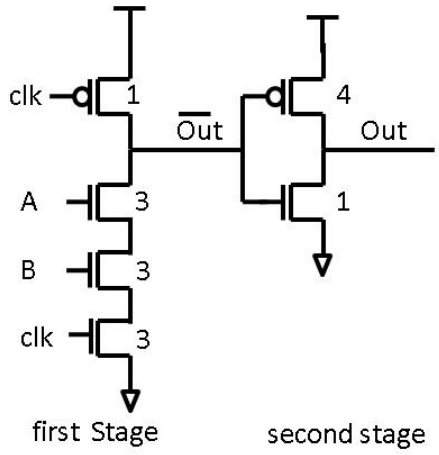


Fig.3a Domino Logic

Solution:

For evaluation phase:

First stage: (input A or B, pull-down) $LE_{1,EV}$ = (3 x1) / (3x1) = 1 (1 pts)

Second stage: (out_bar, pull-up) $LE_{2,EV}$ = ((2+0.5) x 1) / (3 x1) = 5/6 (1 pts)

For evaluation phase:

First Stage: (clk, pull-up) $LE_{1,PR}$ = ((1+3)x2) / (3x1) = 8/3 (1 pts)

Second Stage: (out_bar, pull-down) $LE_{2,PR}$ = ((4+1)x1) / (3x1) = 5/3 (1 pts)

Evaluation Phase:
$LE_{1,EV}$ = 1
$LE_{2,EV}$ = 5/6

Precharge Phase
$LE_{1,PR}$ = 8/3
$LE_{2,PR}$ = 5/3

(b) **(3 pts)** A 4-input AND gate can be implemented by using three 2-input domino AND gates as shown in Fig.3a. We properly size each stage in the 4-input AND gate to minimize the delay of the evaluation phase. What is the minimum delay ($\mathbf{T_{p,EV}}$) in the worst-case during the evaluation phase?

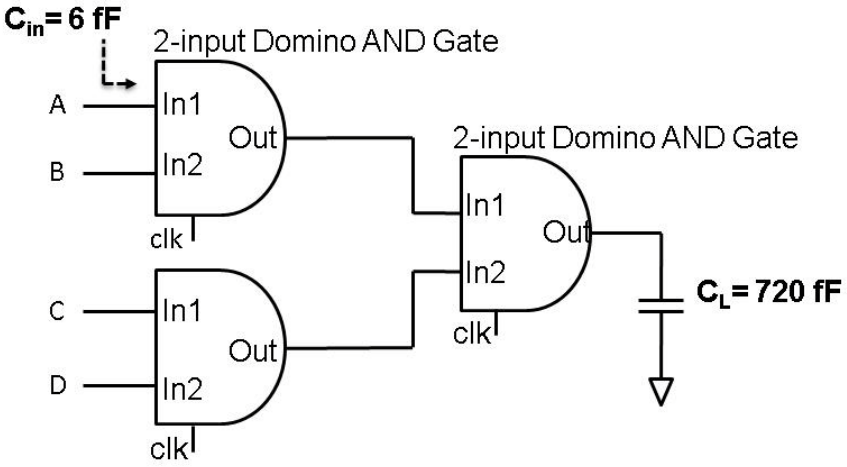


Fig.3b 4-input AND gate with domino logic in Fig.3a.

Solution:

In the evaluation phase:
There are 4 stages:

LE_{EV}:	1	5/6	1	5/6	
b:	1	1	1	1	
p:	4/3	5/6	4/3	5/6	(0.5 pts)
F=	720fF/ 6fF =120				(0.5 pts)
EF = (πLExπbxF)^0.25 = 3.02					(1 pt)

$\mathbf{T_{p,EV}}$ = tinv x (4x EF + ∑p) = tinv x (4 x 3.02+ (4/3+5/6+4/3+5/6)) = 16.41 tinv
= 16.41 x (ln(2) x1.2kΩx 6fF) =81.90 ps (1 pt)

$T_{p,EV}$ = 81.90 ps

(c) (3 pts) With the same sizing, what is the high-to-low delay ($T_{p,PR}$) during the precharge phase?

Solution:

In the precharge phase:
The three 2-input domino AND gate precharge **in parallel**. The precharge delay only a single 2-input domino AND gate **(only one dynamic sage + one inv stage)**. (0.5 pts)

LE_{PR}: 8/3 5/3
p: 8/3 5/3 (0.5 pt)

EF = 3.02 from the calculation for evaluation phase. With the same sizing, we can calculate the delay easily by using the same EF of evaluation phase and adjust the EF with ratios of LEs in precharge phase. (0.5 pt)

$T_{p,PR}$ = tinv x (EF x ($LE_{1,PR}$ / $LE_{1,EV}$) + EF x ($LE_{2,PR}$ / $LE_{2,EV}$) + ∑p) (1 pt)
= tinv x (EF x (8/3) / 1 + EF x (5/3) / (5/6)+ ∑p)
= tinv x (3.02*14/3 + (8/3 +5/3))
= tinv x 18.43
= (ln(2) x 1.2kΩx 6fF) x 18.43 = 91.98 ps (0.5 pt)

$T_{p,PR}$ = 91.98 ps

(d) **(2 pts)** One engineer developed new domino logic as shown in Fig.3c**.** We use this new domino gate for implementing the 4-input AND gate of Fig.3b. Describe qualitatively how this change impacts the evaluation and precharge times of the gate in comparison with the results of parts (b-c).

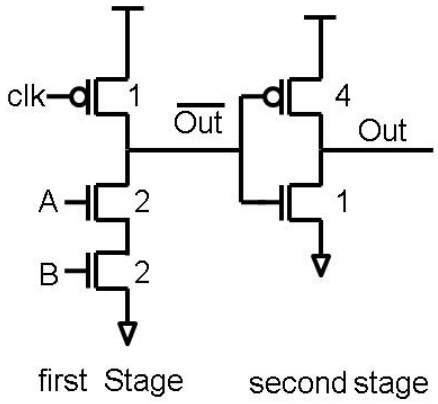


Fig.3c New domino logic for 4-input AND gate in Fig.3b

Solution:

In this footless 2-input domino gate, the foot NMOS switch connected to clk is eliminated.

Evaluation time:
We have smaller LE for first stage. The delay of evaluation phase will be reduced. (1 pt)

Precharge time:
The LE for clk is 4 times smaller. So the precharge delay for a single 2-input domino gate will be reduced. (0.5 pts)

However, the worst case pattern is A=B=C=D = 1 in previous evaluation phase. During the precharge phase, PMOS precharge current competes with the NMOS pull-down current due to no foot NMOS clock switch in this implementation. Because of the sizing ratio of PMOS and NMOS, the out_bar node (dynamic node) may not be pulled up high enough to reach the switching threshold. The precharge operation may fail for the worst case input pattern. (0.5 pts)