UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits Fall 2011

MIDTERM EXAMINATION #2

Time allotted: 75 minutes

NAME: _____ Solution

STUDENT ID#: _____

INSTRUCTIONS:

1. **Unless otherwise stated, assume**
   a. **temperature is 300 K**
   b. **material is Si**
   c. **No Early effect**
   d. **All capacitors are shorted at the operating frequency**

2. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
   Specially, while using chart, make sure that you indicate how you have got your numbers. For example, if reading off mobility, clearly write down what doping density that corresponds to.
3. **Clearly mark (underline or box) your answers.**
4. **Specify the units on answers whenever appropriate.**

SCORE:	**1**	**/ 20**
	2	**/ 15**
	3	**/ 15**
Total		**/ 50**

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

PROPERTIES OF SILICON AT 300K

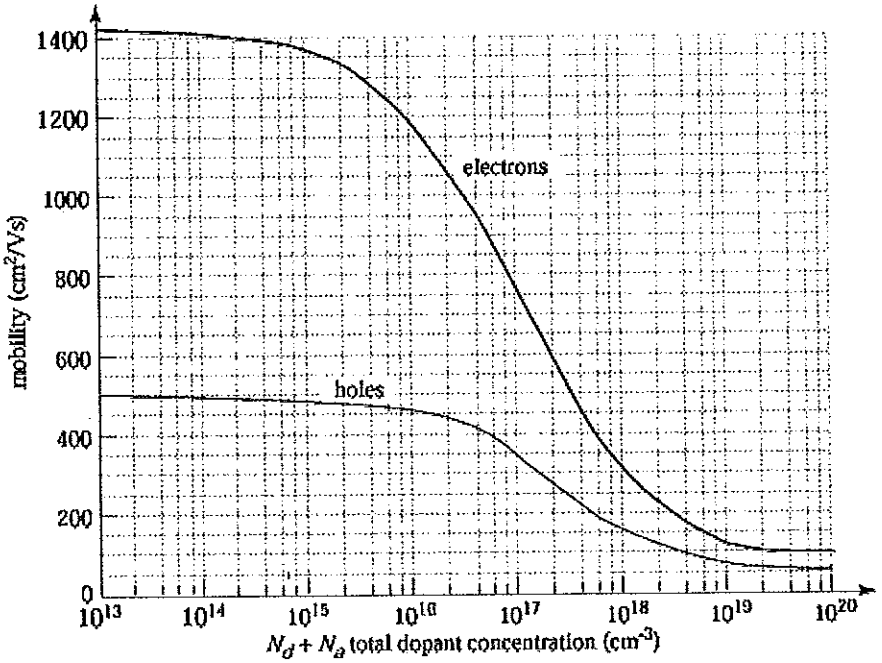
Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

USEFUL NUMBERS

$V_T \ln(10) = 0.060$ V at T=300K

Depletion region Width: $W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)\left(V_{bi}-V_{Applied}\right)}$

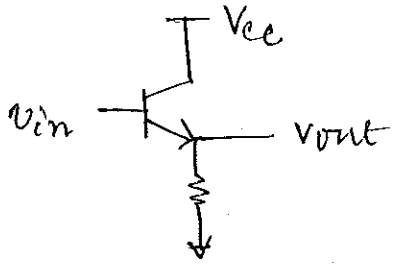
Electron and Hole Mobilities in Silicon at 300K



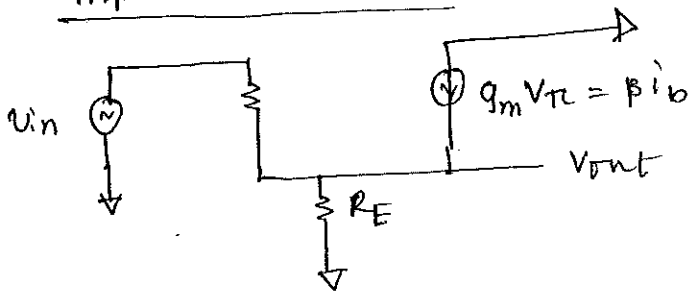
Prob 1. [20]

(a) [8 pt] Say, we want a high input resistance and low output resistance amplifier. There is no requirement on the gain. Which amplifier topology will you use? By using a small signal model, **derive** the input and output resistance of this amplifier. You could use the simplest configuration of the amplifier for your analysis.

common collector or emitter follower



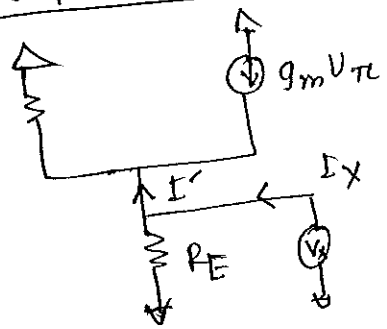
Input resistance:



$$v_{in} = i_b r_\pi + (\beta i_b + i_b) R_E$$

$$R_{in} = \frac{v_{in}}{i_b} = r_\pi + (\beta+1) R_E$$

Output resistance:



$$R_{out} = R_E \,||\, \frac{V_X}{I'}$$

$$V_X = -v_\pi$$

$$I' = -i_b - \beta i_b = -(\beta+1) i_b = -(\beta+1)\frac{+V_\pi}{r_\pi}$$

$$= \frac{V_X(\beta+1)}{r_\pi}$$

$$\therefore \frac{V_X}{I'} = \frac{r_\pi}{\beta+1} \simeq \frac{1}{g_m}$$

$$\therefore R_{out} \simeq 1/g_m \,||\, R_E$$

(b)[8 pt] Now consider a problem where we need a circuit that gives (i) low input resistance (ii) low output resistance and (iii) high amplitude of the gain. The sign of the gain is not important. How will you design such a circuit? Note that, you are free to use more than one transistor in your design. Make sure you adequately explain your circuit.

We can design a two stage circuit

req: low input resistance req: low output resistance.

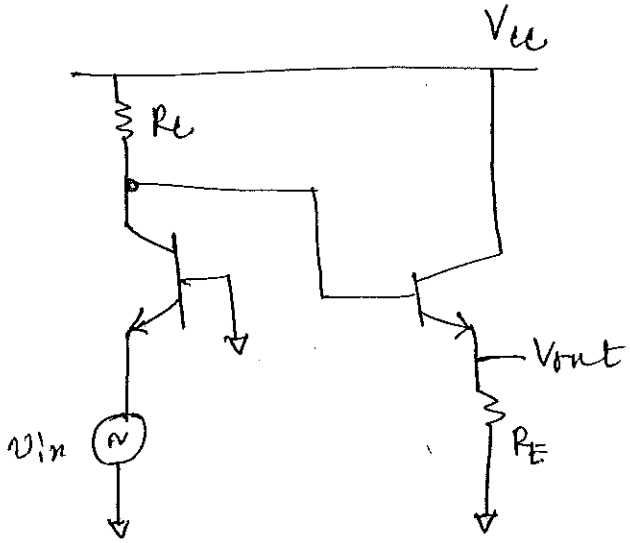
We note that total gain, $A_v = A_{V_1} \times A_{V_2}$

Thus if one of the stages has high gain, all the requirements can be satisfied.

Then: stage 1 : CB (low input resistance & high gain)

stage 2 : cc (low output resistance & $A_v \approx 1$)

can be chosen.

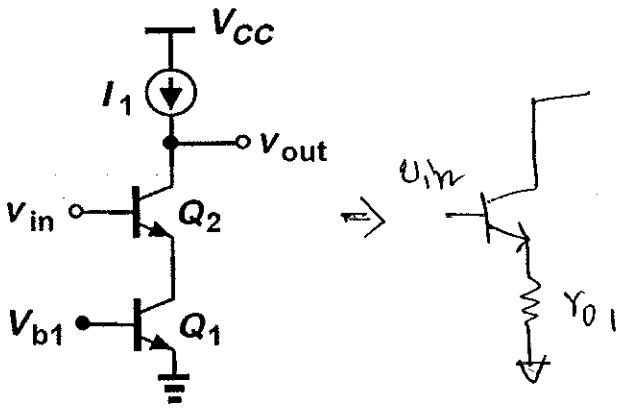


$R_{in} \sim 1/g_m$

$R_{out} \sim R_E \,||\, \left(1/g_m + \frac{R_c}{\beta+1}\right)$

$A_v \sim g_m R_c \times 1 \sim g_m R_c$

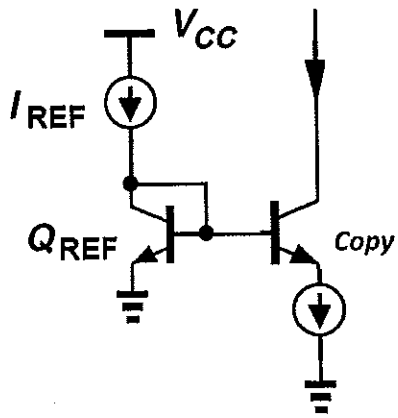
(c) [4 pt] Is the following a good cascode? Qualitatively explain why or why not.



it is not a good cascode because Q_1 acts as an emitter degeneration resistor and lowers gain.

Prob 2 [15 pt]

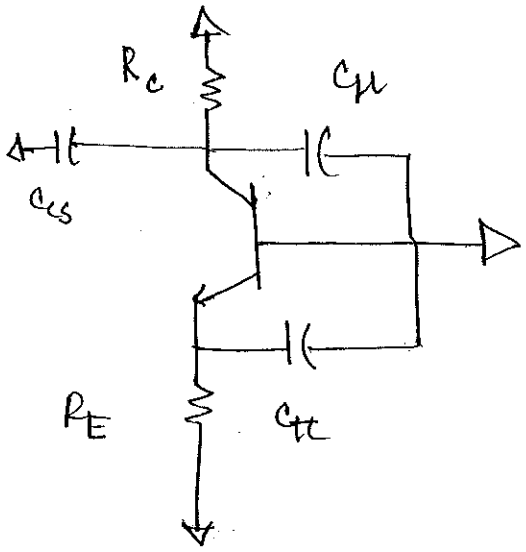
(a) [4 pt] Is the following a good current mirror? Qualitatively explain why or why not? Note that the current source on the copy transistor is NOT a golden current source.



it is <u>not</u> a good mirror.

This is because I_{copy} is set by the current source at the copy transistor and does not depend on $I_{c,ref}$.

(b) [6 pt] For a common base amplifier, find out the input and output pole frequencies. Which one is expected to be larger?

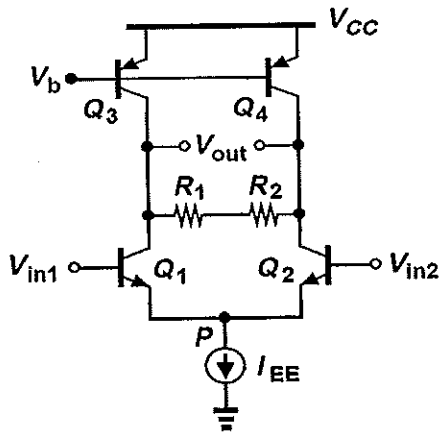


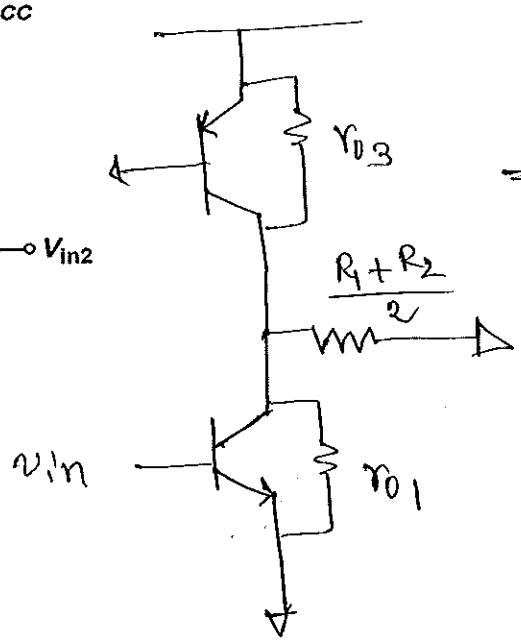
$$\omega_{P_{in}} = \frac{1}{\left(\frac{1}{g_m} \parallel R_E\right) C_{TL}} \approx \frac{g_m}{C_{TL}}$$

$$\omega_{P_{out}} \approx \frac{1}{R_L (C_\mu + C_{CS})}$$

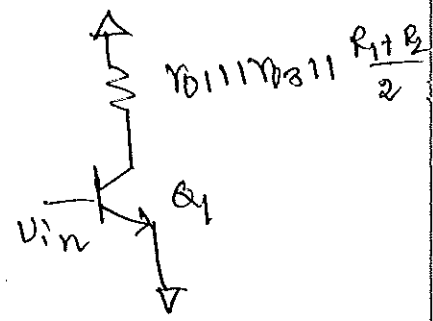
$\omega_{P_{in}} > \omega_{P_{out}}$ since $g_m \gg R_L$

(c)[5 pt] Find out the gain of the following amplifier when R_1 and R_2 are NOT equal. Also consider Early effect in your analysis.





$\Rightarrow$



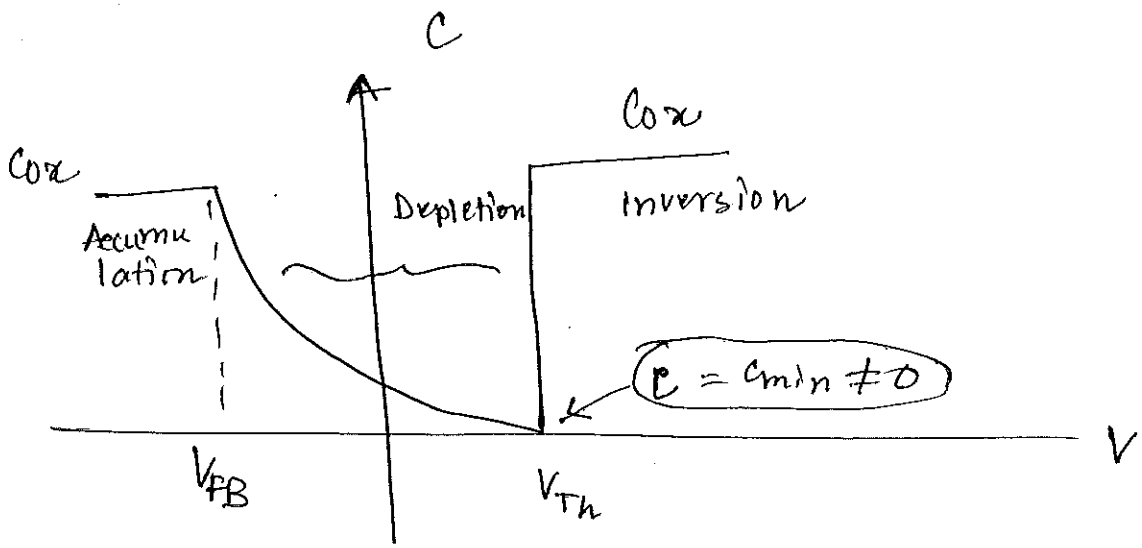
$$A_V = -g_{m_1}\left(r_{O_1} \parallel r_{O_3} \parallel \frac{R_1+R_2}{2}\right)$$

Prob 3. [15 pt]

(a) [5 pt]

Condition	True	False
A MOSFET with p-type body will have p+ source and drain		✓
The doping of the body and the polysilicon gate are of the same type		✓
Between two gate oxides, the one with the higher permittivity is preferred	✓	
The pinch-off region looks like a reverse biased p-n junction	✓	
Channel length modulation becomes more prominent for shorter channel length devices	✓	

(b)[4 pt] For a p-body MOS capacitor, draw the C-V plot clearly showing the different regions of operation and also the flatband and threshold voltages.



(c) [6 pt]

(i) [2 pt] Write down the different charges present in the channel at inversion. Do all these charges contribute to current flow? Why or why not?

(ii) [1 pt] Write down a mathematical expression for the charge density per unite area that provides current in the inversion region as a function of gate voltage.

(iii)[3 pt] Starting from $I=WQv$, where W is the width of the transistor, Q is the charge density per unit area and v is the velocity of electrons, find out the expression for current in a velocity saturated MOSFET. From an experimental measurement, how will you say that the MOSFET is indeed velocity saturated?

(i) immobile depletion charge

mobile inversion charge

(ii) $Q = C_{ox}(V_{gs} - V_{th})$

(iii) $I = WQ v_{sat}$

$= W C_{ox}(V_{gs} - V_{th}) v_{sat}$

For velocity saturated MOSFET I_D changes linearly with V_g.

For a conventional MOSFET, $I_D \sim V_g^2$