Final Project

Design and Implementation of a Digital Lock

Digital Logic Laboratory (ECE2610)
Final Project
MARKING SHEET

Group number and Student Names: ……..
……..
……..

Laboratory Section: …… **Date:** ……

Item	Criteria	Description	Weight %	Mark	Comment
1	**Project Deliverables: (35%)** • State Diagram. (15%) • Testbench and simulation results. (25%) • Final Report. (60%)	Each group should submit a report and explain their design and how they come up with each Verilog module	35		
2	**Project Video**	Each group should submit a video that demonstrates a working prototype with different inputs to the system.	30		
3	**Q/A**	Each member in the group should answer questions related to their design.	35		
4	**Extra Credit**	Optional.	Up to 30%		

Digital Logic Project

The final project is about design and implementation of a digital lock. All the needed information can be found in the next page.

- **Project Deliverables: (35%)**

Task	Weight %	Due date
State Diagram	15	**November 26, 2020**
Testbench and simulation results	25	**December 3, 2020**
Final Report	60	**December 12, 2020**

Your report must include the following sections:

- Title page
- Table of contents
- Abstract
- Introduction
- Design
- Results
- Conclusion

- **Project Video: (30%)**

Each group should submit a video of maximum of 2 minutes that demonstrates a working prototype with different inputs to the system. Each member in the group should present his/her part.

Due: December 10, 2020

- **Q/A: (35%)**

A time slot will be assigned to each group, and each member in the group should answer questions related to their design.

Date: **December 10, 2020**

Digital Lock

Consider a digital lock with a three digit combination lock. The combination lock code is **241**.

- Initially the digital lock is in its' idle mode. The operation of digital lock is as follows:

1- Assign numbers 1 to 5 to the push buttons on the FPGA board as depicted in Fig. 2.

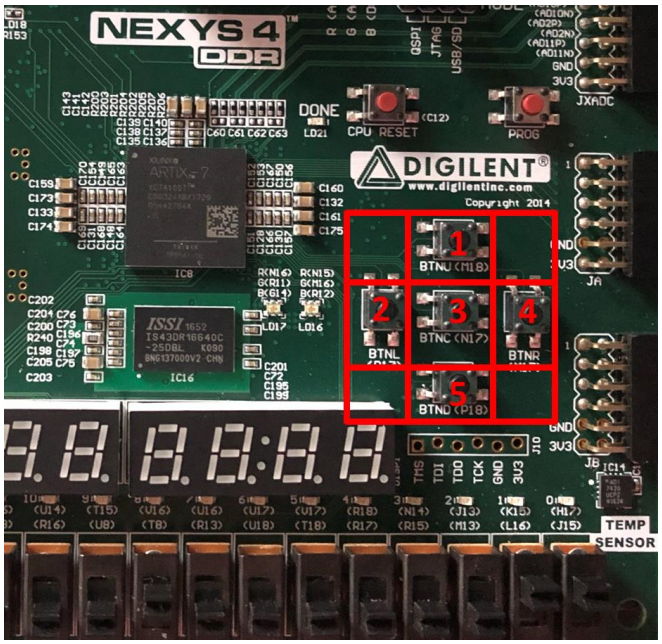

Fig 2. Push buttons as a keypad

2- User needs to enter the digits sequentially and the code will be displayed on the seven segments.

3- If the user enters an incorrect combination he/she will have one more chance to enter the code otherwise he/she will not be allowed to enter any codes.

The goal of this project is the design and implementation of a digital lock using the Nexys4 board. The top level design of this digital lock is shown Figure 2. It consists of the following modules:

1. **Cntr_Unit:** To lower down the FPGA internal clock to 10Hz.
2. **FSM_Lock_Unit:** The FSM that controls the digital lock operation.
3. **Disp_Unit:** It accepts the binary data for seven segment displays and decode and display them using time division multiplexing.
4. **PB{1,2,3,4,5}:** These push buttons from FPGA board are used to enter the combination code.

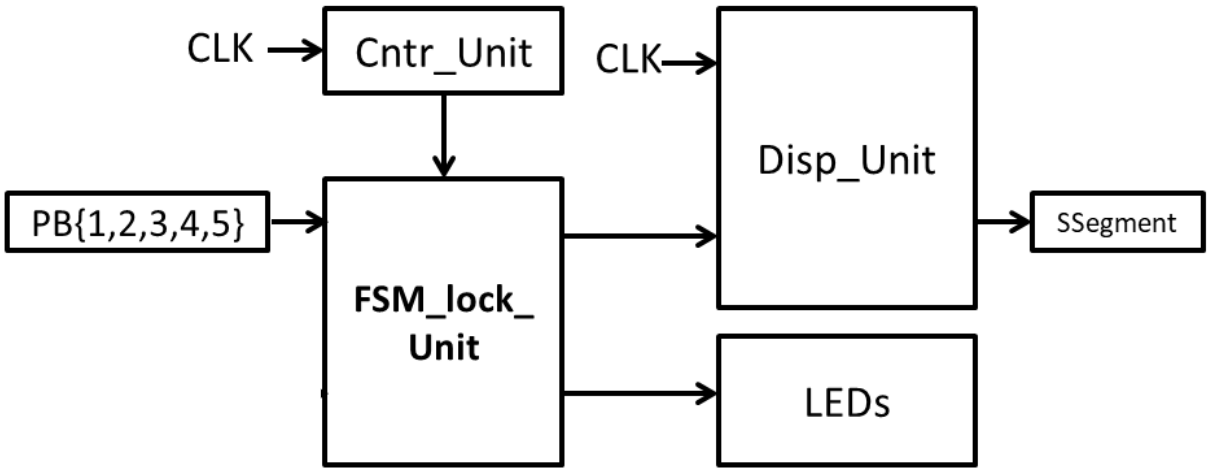

Fig 3. Top level schematic of the digital lock

Design of Finite State Machine for Digital Lock Operation

Draw a FSM state diagram with 3 inputs, first digit (d_1), second digit (d_2), and third digit (d_3), 5 output signals, first digit on display (disp_1), second digit on display (disp_2), third digit on display (disp_3), Unlock signal (Unlck), and number of remaining tries (N). Create a Verilog code for this FSM and use the Nexys4 board to verify its correct operation.

- Note that in your design you need to design each block separately and then for the overall system you need to instantiate all the modules in the top level module.