

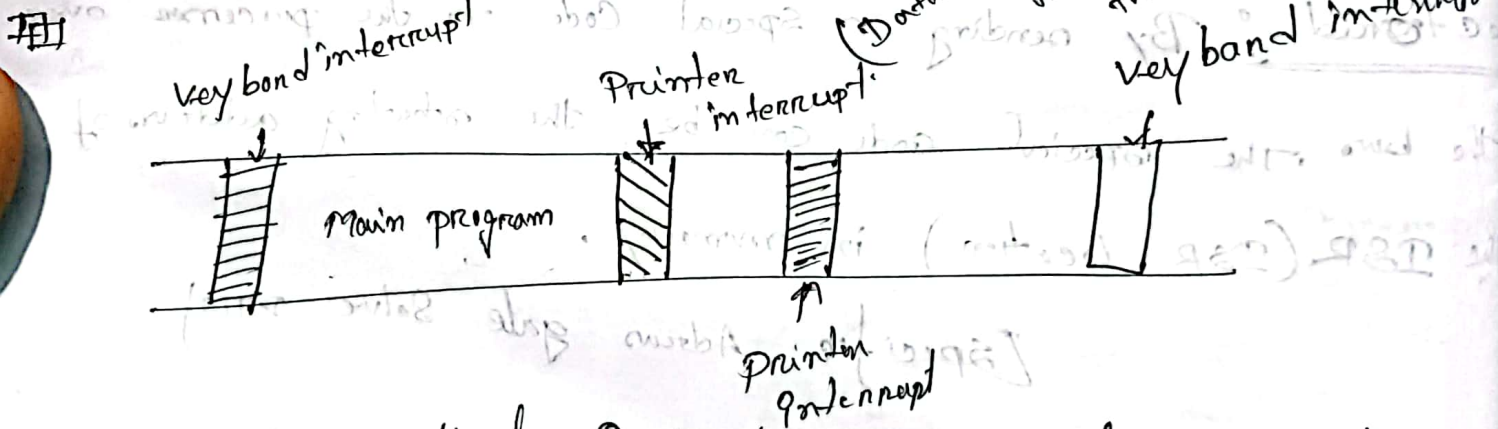
## Interrupt Vector Table

Purpose of Interrupts : when useful

• Interrupts are useful when interfacing I/O devices or relatively low data transfer, such as keyboard inputs.

• Interrupts processing allows the processor to execute other software while the keyboard operation is taking about to type next.

[Interrupts allow a very slow device (key board) to execute its own time for execution]



• Time line that indicates interrupt usage in typical system

→ here time line shows typing on keyboard, a printer removing data from memory and program executing.

# Interrupt vector table (IVT)

- Interrupt vector, and vector table are crucial to an understanding of hardware and software interrupts.
- The IVT is located in the first 1024 bytes of memory address 000000H - 0003FFH.
- Contains 256 different 4 byte interrupt vectors.

\* [ 0-255 interrupt vector, each 4 byte  $\Rightarrow 4 \times 256 = 1024$  bytes ]  
[ procedure name and its address ]

• IVT to 1st 2 bytes contain the offset address.

• " " 2nd 2 " " " " segment " " "

## Table Described

• IVT Link between

Intn type code & procedure

• 8086 256 bytes

00H - FFH

• 1 instruction, 4 byte, i.e. double word. (word = 2 byte, double word = 4 byte)

• The double word to address of procedure name

and service routine name



Higher addressed word pointer with base address of

segment, New IP

Then New CS: New IP provides physical address.

each type (2 New CS, 2 New IP) 4 bytes.  $50 \times 256 \times 4 = 1024$  byte.

standing - 3FFH

ending address - 3FCH

ending address  
ending address  
3 FCH + 3 = 3FFH

3FCH + 3 = 3FFH

Calculate 16

255 x 4 = 1020

convert hex

new CS :-

new IP :-

CS: base address  
IP offset

Available Interrupt Pointers (24)

reserved Interrupt Pointers (27)

Dedicated Interrupt Pointers (6)

3FFH	3FFH	type 255 pointer (available)	255
084H	084H	type 33 pointer (available)	33
080H	080H	type 32 pointer (available)	32
07FH	07FH	type 31 pointer (reserved)	31
014H	014H	type 5 pointer (reserved)	32
0A0H	0A0H	type 4 pointer overflow	16
008EH	008EH	type 3 pointer 1 bit INT instruction	12
0081	0081	type 2 pointer non maskable	8
004F	004F	type 1 pointer single step	4
00H	00H	type 0 pointer divide error	
00H		16 bits	

• INT 3 groups

• Dedicated (INT 0-4) \* reserved (INT 5-31)

\* Available (INT 32-255)

INT(0) : (Device error)

- at 2<sup>nd</sup> Johnson Division error 2<sup>nd</sup>, Divisor 2<sup>nd</sup> 600.
- Dividend 0 2<sup>nd</sup> 600 Device error 2<sup>nd</sup>.
- The ISR address is 0x4 = 000004H in the IVT.

INT1 (single step) : The ISR ~~on contents~~ generally display

contents of all register.

location 1x4 = 000004H in the IVT.

In eng : This interrupt occurs whenever in Division.

error i.e. when the result of a Division is too large to be stored. This condition normally occurs when Division is small or compared to the Dividend or Division is zero.



## Int 2 (non maskable Interrupt)

Response on NMI Line

ISR address  $2 \times 4 = 0000BH$

Int 3 : used to cause breakpoints in the program.  
It is useful in debugging large programs.  
It is programmed to display of all reg on screen.  
vector  $3 \times 4 = 0000CH$

## Int 4 (Overflow)

It occurs if the overflow flag is set, MP  
executes the INTO (Interrupt on overflow)

used to detect overflow error on ALU.

ISR Street  $4 \times 4 = 0040H$  in INT

## Reserved INT (5-31)

It is reserved by Intel to be used high processor  
80386, Pentium. not available for user

## ② Available interrupts: (INT 32-255)

- It is user defined, Software Interrupts.
- Service various user defined condition.

BOUND: It has 2 operands, and compares a register with two words of memory data.

IRET: The IRET instruction, in a special return instruction used to return from both software and hardware interrupts.

real mode & protected mode

real mode

protected mode

• Old version of INT handling

• new extended version of real mode

• max of 1MB of RAM

• max 16 mb of RAM.

• max INT vector table (IVT)

• max INT description table (IDT)

• Multitasking not possible

• Multitasking possible

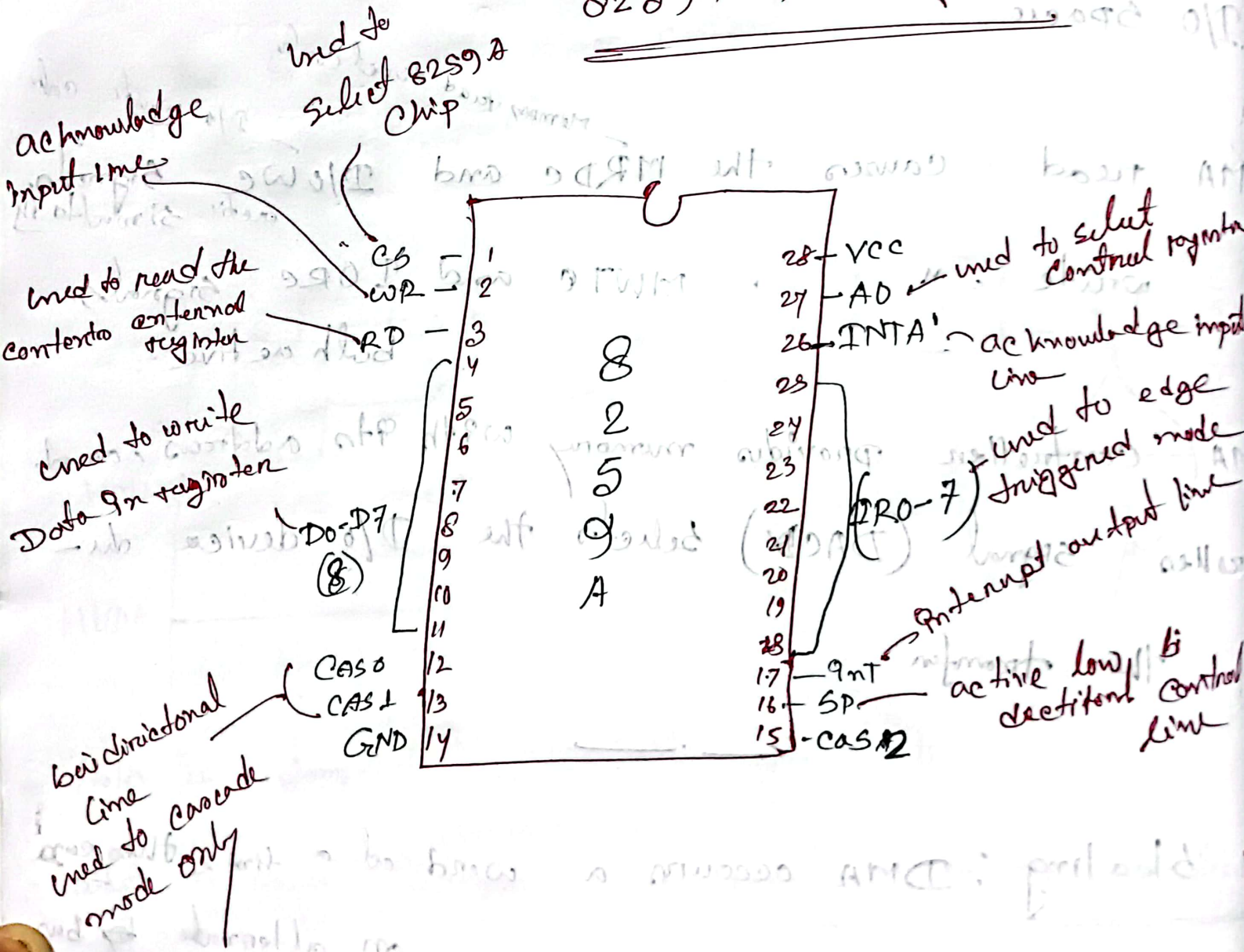
operation: when mp complete, the executing the current instruction it determines whether an INT is active

operation: here INT has the same assignment as real mode, but the INT vector table is different



Fig 4 Pin Diagram

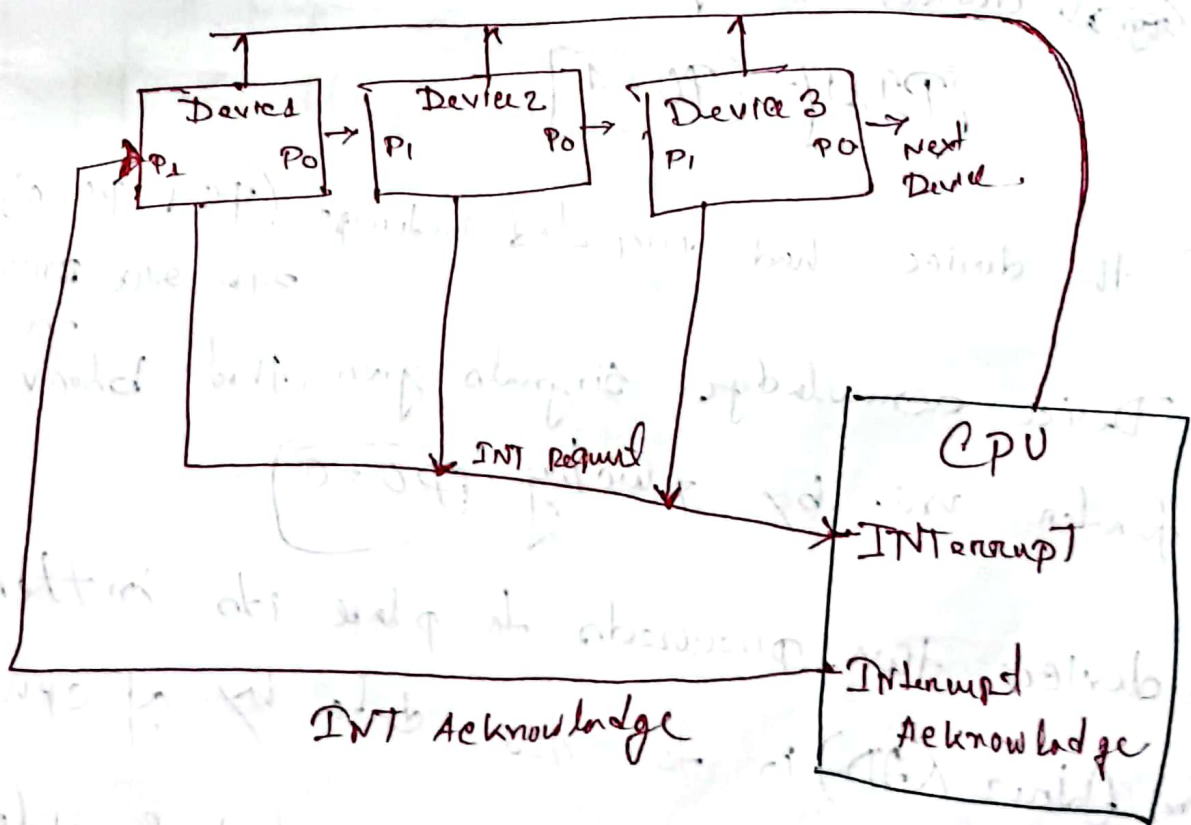
# 8259A Pin Diagram



# Daisy Chaining

- Priority Interrupt to execute one by one.
- connecting all device that can tag. in T in serial manner
- this configuration governed by the priority of devices.

[210 Higher priority]



VAD with vector Address



## working

priority interrupt

INT, req.

- when no int are pending  $\rightarrow$  to  $\uparrow$  High state, device turns  $\rightarrow$  to become low state.
- Cpu acknowledge Int req from line and enables the int acknowledge
- The signal received at the PI (priority input) of device
- If device not requested, proceed this to Next.
- ~~Signal~~ devices through  $\rightarrow$  to PO (priority output)

$$\boxed{PI=1} \quad \boxed{PO=1}$$

- If the device had requested interrupt ( $PI=1$ ,  $PO=0$ )
- The Device acknowledge signals given, that block.
- $\rightarrow$  to further we by placing  $\boxed{PO=0}$
- The device then proceeds to place its in the next vector Address (VAD) in to the data by of cpu
- The Device puts its Int. req. signal high state to indicate interrupt has turn off.
- If  $PI=0$  and  $PO=0$  then say acknowledge signal has blocked.