MP = I/O operation

Memory mapped I/O	Standard ~~Isolated~~ mapped I/O (I/O mapped I/O)
• I/O devices are treated as memory.	• I/O devices are treated as I/O devices.
• 16 bit (A0-A15) / addrss 2^{20}	• 8 bit (A0-A7) / Adrss 2^{16}
• Data transfer for same Memory & I/O	• Diffrnt for memory and I/O.

#Disadvantage of memory Mapped I/O

• There is no IN, OUT, and other instruction here.
The memory mapped I/O is slow because less efficiency

Memory mapped I/O vs Isolated I/O

Memory Mapped IO	Isolated I/O
. It uses memory from the main memory	. It uses seperated memory space.
. Smaller in size	. Comparatively larger in size.
. faster operation	. Slower operations.
. Any instruction which refernces to memory can be used	. Limited instruction can be used. those are IN, out, INS, OUTS;
. Lesser efficient	. More efficient due to seperate buses.
. Memory and I/O have same address space.	. Memory and I/O have seperated addrss space.

why memory address Decoding necessary.

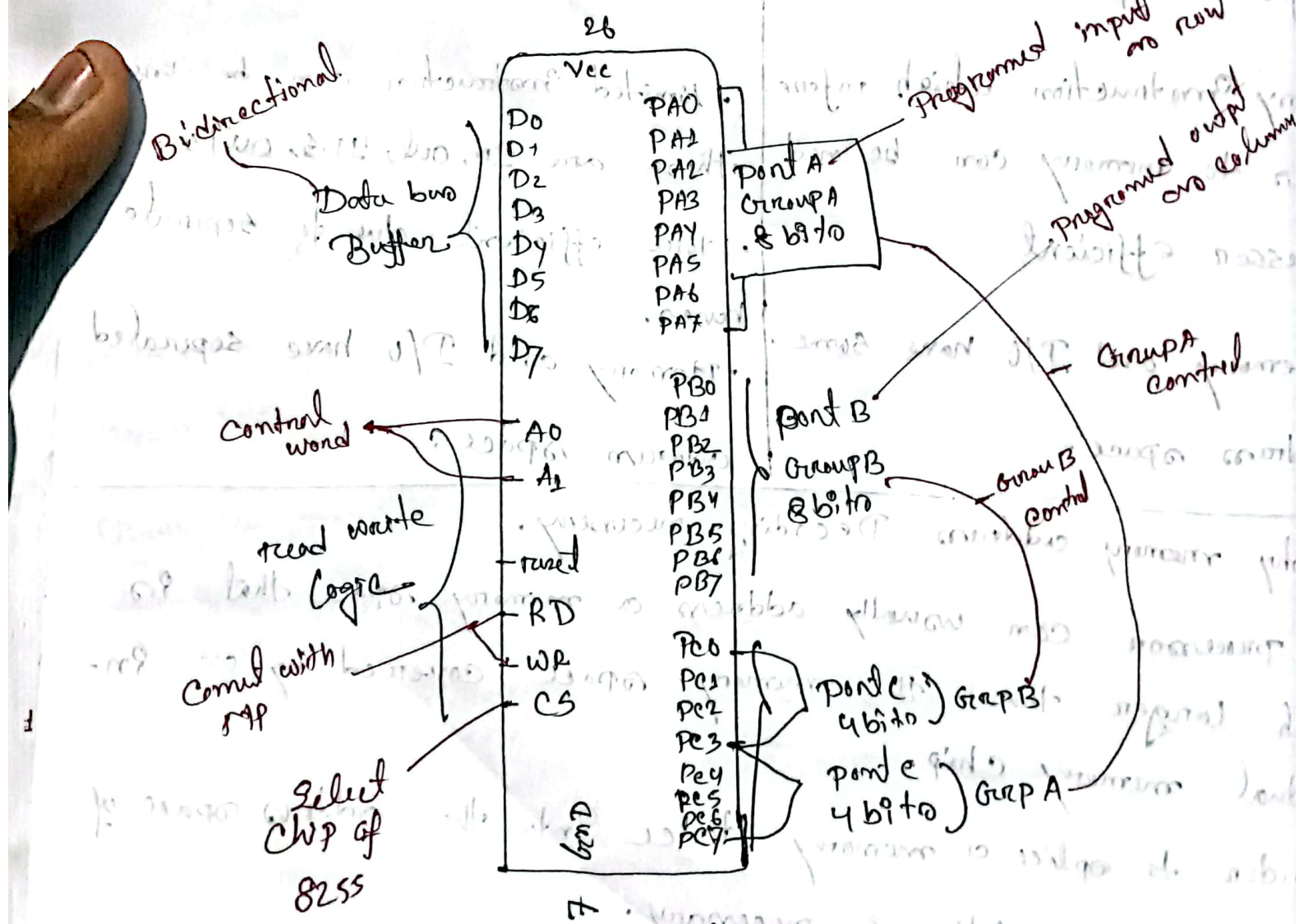
The processor can usually address a memory space that is much larger than the memory space covered by an individual memory chip.

In order to splice a memory device into the address space of the processor decoding is necessary.

Example:

8088 issue 20 bit address, on other side EPROM BIOS 2716 has only 2KB memory along with 11 address pin. now EPROM can be placed 2Kb section of 1MB address space, and the decoder can decode 9 extra address pin here.

8255 Pin Diagram: (~~PPI Peripheral interface~~ adapter)



[control takes singnal from control word and forwards it on respective ports)

8 bit I/O ports works

bi directional.

	Mode 0	Mode 1	mode 2	BSR mode
port A	yah	yah	yah	NO
port B	"	"	NO	NO
port C	"	NO	NO	yes.

Mode 0 and 1 operation:

mode 0 is a basic input/output mode that allows the pins of grp B to be programmed as simple input and latched output connection

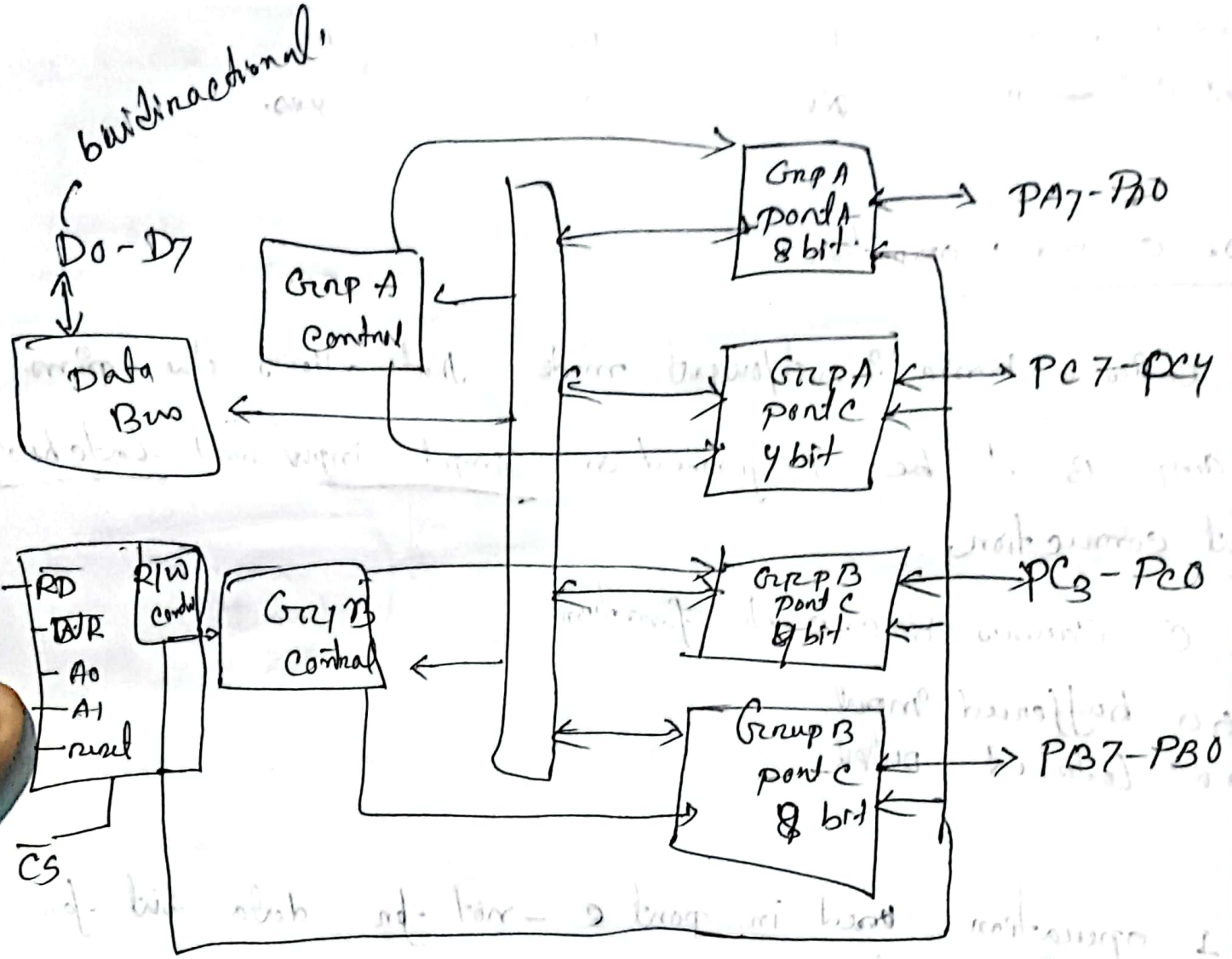
Mode 0 causes 82C55 to function.
as a buffered input
or a latched output

mode 1 operation. used in port C - not for data but for control or handshaking signals.

- to help operate either or both port A & B as.
  strobed input ports

8255A programmable peripheral Interface

(P P I)



8255A

Mode 0 : here port A and B used 8 bit ports and port C as 4 bit ports. Each port can generated either input or output mode where output latched input not latched

Port here do not have Interrupt capability.

Mode 1 : here mode 1, port A & B used as 8 bit I/O ports. They can configured as either output or input ports. Each ports uses 3 lines from port C as handshake signals. Input output are latched.

Test & AND

- Difference between Test and And operation: is that test does not alter the destination operand. The test instruction Performs a bitwise AND on two Operands. The flag SF, ZF, PF, CF, OF and AF are modified while the result of the AND is discarded

Example If we need to check whether a number is even or odd. we can using test operation

Test AL 0111

JZ Even_Number

the And operation return 1, otherwise it return 0

for example operand1 : 0101.

After And → operand1 : 0001.

CMP & SUB (Difference)

Recall that SUB subtracts producing a result but also setting flag (CF, OF, SF, ZF).

[ফলাফল স্টোর হয় না flag সেট হয়]

The CMP instruction is the same to the sub but only sets flags.

Ah changes

MOV Ah 101B = 5

SUB Ah, 010B = 2

Ah = 0011 = 3

CF = 0 OF = 0

ZF = 0 SF = 0

Ah no changes.

MOV Ah 101B = 5

CMP Ah 010B = 2.

Ah = 0101 = 5

CF, OF, ZF, SF = 0

here the value are changes with the SUB but not changing in the CMP (5 ই থাকে কিন্তু sub এ (5-2) = 3 হয়েছে)

DMA

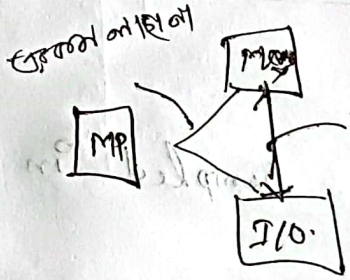
DMA (Direct memory access) : The DMA I/O technique provides direct access to the memory while the MP is temporarily Disabled.

Some Disk memory system And video system are often DMA produced

floppy, fixed, optical disk storage

Digital, analog monitor

DMA occur between an I/O device and memory with out the use of MP

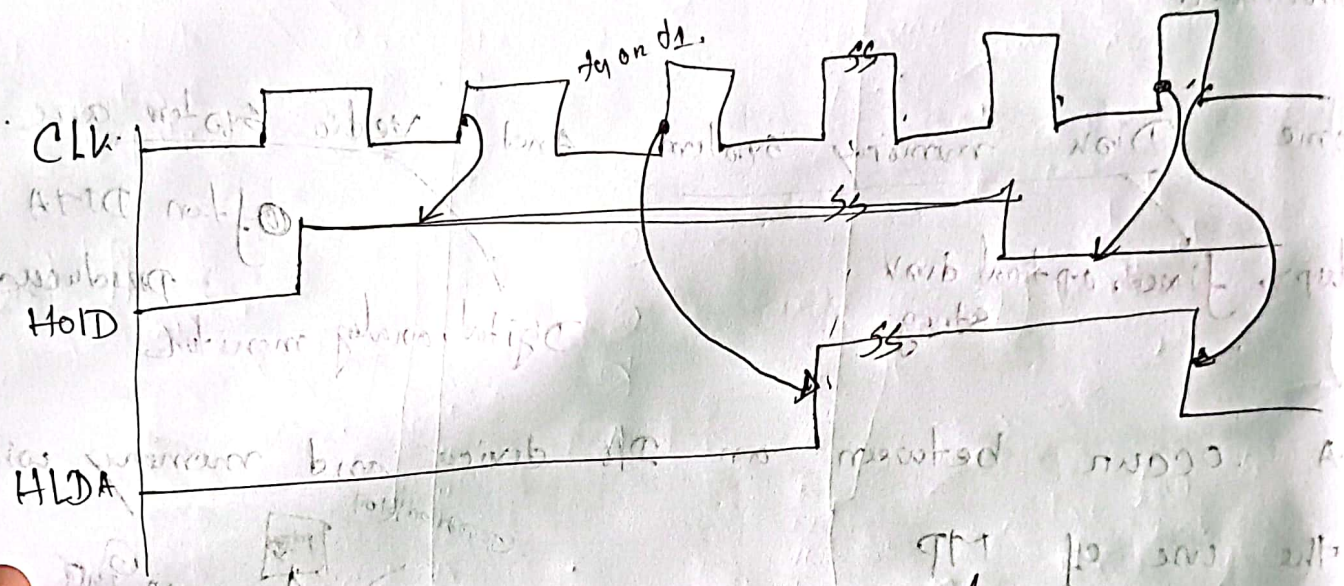


⇒DMA read : Transfer data from memory to I/O device.

⇒DMA write : " " I/O to memory "

DMA operation : 2 control signal are used to request and acknowledge a direct memory access transfer on the MP based system

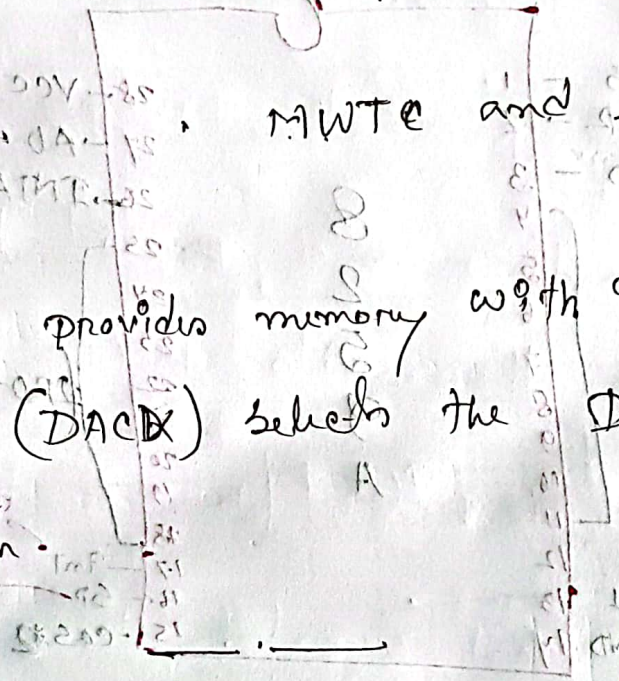
- The hold pin is an input used to request a DMA action.
- The HLDA pin is an output that acknowledges the DMA operation.



- Hold pin sampled in any clocking cycle.
- when processor recognize the hold, it stops executing software and enters hold cycle.
- Hold input has higher priority than INTR or NMI.
- If MP pin only reset pin is Higher priority than Hold.
- HLDA becomes active to indicate the processor has placed its buses at high impedance state.

HLDA outputs is a signal to the ~~release~~ request device that the processor has release control of its memory & I/O space

- DMA read causes the MRDC and IOWC signals. (Memory read control, I/O write control) active simultaneously
- " write " MWTC and IORC signals. both are active.
- DMA controller provides memory with its address, and controller signal (DACK) selects the I/O device during the transfer.



DMA - Stealing : DMA occours a word at a time, this can allow the CPU to access memory on alternate bus cycle. Its called DMA stealing. [CPU is from one bus cycle to memory access]

DMA interleaved :

when memory cycles are much faster than processor cycles, then its possible, where DMA controller uses memory and CPU.