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Application Note

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Designing for Board Level Electromagnetic Compatibility

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This application note discusses board level electromagnetic compatibility (EMC), from component selection, circuit design, to printed circuit board layout.

The text is divided into the following parts:

- PART 1: An overview of EMC
- PART 2: Component selection and circuit design techniques
- PART 3: Printed circuit board layout techniques
- APPENDIX A: Glossary of EMC terms
- APPENDIX B: Immunity measurement standards

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PART 1:
AN OVERVIEW OF ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

Electromagnetic interference (EMI) is a major problem in modern electronic circuits. To overcome the interference, the designer has to either remove the source of the interference, or protect the circuit being affected. The ultimate goal is to have the circuit board operating as intended — to achieve electromagnetic compatibility (EMC).

Achieving board level EMC may not be enough. Although the circuit may be working at the board level, but it may be radiating noise to other parts of the system, causing problems at the system level. Furthermore, EMC at the system or equipment level may have to satisfy certain emission standards, so that the equipment does not affect other equipment or appliances.

Many developed countries have strict EMC standards on electrical equipment and appliances; to meet these, the designer will have to think about EMI suppression — starting from the board level.

Elements of the Electromagnetic Environment

A simple EMI model consists of three elements:

- EMI source
- Coupling path
- Receptor

This is shown graphically in Figure 1.

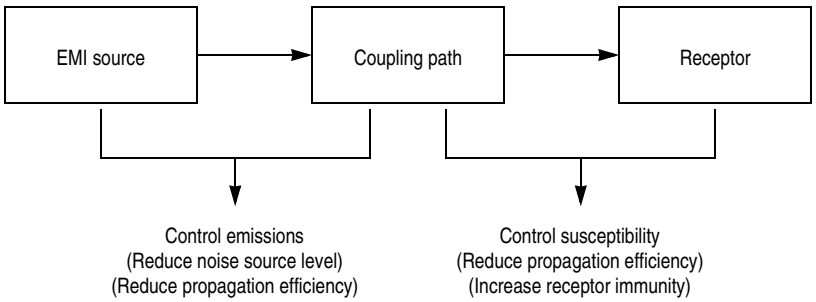

Figure 1. EMI Elements

EMI source

EMI sources include microprocessors, microcontrollers, electrostatic discharges, transmitters, transient power components such as electromechanical relays, switching power supplies, and lightning. Within a microcontroller system, the clock circuitry is usually the biggest generator of wide-band noise, which is noise that is distributed throughout the frequency spectrum. With the increase of faster semiconductors, with faster edge rates, these circuits can produce harmonic disturbances up to 300 MHz.

Coupling path

The simplest way noise can be coupled into a circuit is through conductors. If a wire runs through a noisy environment, the wire will pick up the noise inductively and pass it into the rest of the circuit. An example of this type of coupling is found when noise enters a system through the power supply leads. Noise carried on the power supply lines are conducted to all circuits.

Coupling can also occur in circuits that share common impedances. For instance, two circuits that share the conductor carrying the supply voltage and the conductor carrying the return path to ground. If one circuit creates a sudden demand in current, the other circuit's voltage supply will drop due to the common impedance both circuits share between the supply lines and the source impedance. This coupling effect can be reduced by decreasing the common impedance. Unfortunately, source impedance coupling is inherent to the power supply and cannot be reduced. The same effect occurs in the return-to-ground conductor. Digital return currents that flow in one circuit create ground bounce in the other circuit's return path. An unstable ground will severely degrade the performance of low-level analog circuits, such as operational amplifiers, analog-to-digital converters, and sensors.

Coupling also can occur with radiated electric and magnetic fields which are common to all electrical circuits. Whenever current changes, electromagnetic waves are generated. These waves can couple over to nearby conductors and interfere with other signals within the circuit.

Receptor

All electronic circuits are receptive to EMI transmissions. Most EMI are received from conductive transients, although some are received from direct radio frequency (RF) transmissions. In digital circuits, the most critical signals are usually the most vulnerable to EMI. These include reset, interrupt, and control line signals. Analog low-level amplifiers, control circuits, and power regulators also are susceptible to noise interference.

To design for EMC and to meet EMC standards, the designer should minimize emissions (RF energy exiting from products), and increase susceptibility or immunity from emissions (RF energy entering into the products). Both emission and immunity can be classified by radiated and conductive coupling, as shown in Figure 1. The radiated coupling path will be more efficient in the higher frequencies while a conducted coupling path will be more efficient in the lower frequencies.

Cost of EMC

The most cost-effective way to design for EMC is to consider the EMC requirement at the early stages of the design (see Figure 2).

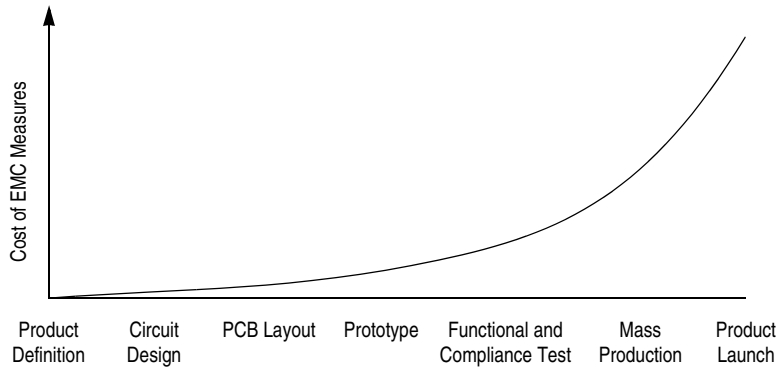

Figure 2. Cost of EMC Measures

It is unlikely that EMC will be the primary concern when the designer first chooses the components, designs the circuit, and designs the PCB layout. But if the suggestions in this application note are kept in mind, the possibility of poor component choice, poor circuit design, and poor PCB layout can be reduced.

PART 2:
COMPONENT SELECTION AND CIRCUIT DESIGN TECHNIQUES

Component selection and circuit design are major factors that will affect board level EMC performance. Each type of electronic components has its own characteristics, and therefore requires careful design considerations.

The following sections will discuss some common electronic components and circuit design techniques for reducing or suppressing EMI.

Component Packages

There are basically two types of packages for all electronic components: leaded and leadless.

Leaded components have parasitic effects, especially at high frequencies. The lead forms a low value inductor, about 1nH/mm per lead. The end terminations can also produce a small capacitive effect, in the region of 4pF. Therefore, it is usually the lead length that should be reduced as much as possible.

Leadless and surface mount components have less parasitics compared with leaded components. Typically, 0.5nH of parasitic inductance with a small end termination capacitance of about 0.3pF. From an EMC viewpoint, surface mount components is preferred, followed by radial leaded, and then axial leaded.

Resistors

Surface mount resistors are always preferred over leaded types because of their low parasitic elements. For the leaded type, the carbon film type is the preferred choice, followed by the metal film, then the wire wound.

The metal film resistor, with its dominant parasitic elements at relatively low frequencies (in the MHz), is therefore suitable for high power density or high accuracy circuits.

The wire wound resistor is highly inductive, therefore it should be avoided in frequency sensitive applications. It is best for high power handling circuits.

In amplifier designs, the resistor choice is very important. At high frequencies, the impedance will increase by the effect of the inductance in the resistor. Therefore, the placement of the gain setting resistors should be as close as possible to the amplifier circuit to minimize the board inductance.

In pull-up/pull-down resistor circuits, the fast switching from the transistors or IC circuits create ringing. To minimize this effect, all biasing resistors must be placed as close as possible to the active device and its local power and ground to minimize the inductance from the PCB trace.

In regulator or reference circuits, the DC bias resistor must be placed as close as possible to the active device to minimize decoupling effect (i.e. improve transient response time).

In RC filter networks the inductive effect from the resistor must be considered because the parasitic inductance of the wire wound resistor can easily cause local oscillation.

Capacitors

Selecting the right capacitor is not easy due to their many types and behaviors. Nonetheless, the capacitor is one component that can solve many EMC problems. The following sections describe the most common types, their characteristics and uses.

Aluminium electrolytic capacitors are usually constructed by winding metal foils spirally between a thin layer of dielectric, which gives high capacitance per unit volume but increases internal inductance of the part.

Tantalum capacitors are made from a block of the dielectric with direct plate and pin connections, which gives a lower internal inductance than aluminium electrolytic capacitors.

Ceramic capacitors are constructed of multiple parallel metal plates within a ceramic dielectric. The dominant parasitic is the inductance of the plate structure and this usually dominates the impedance for most types in the lower MHz region.

The difference in frequency response of different dielectric materials mean a type of capacitor is more suited to one application than another. Aluminium and tantalum electrolytic types dominate at the low frequency end, mainly in reservoir and low frequency filtering applications. In the mid-frequency range (from kHz to MHz) the ceramic capacitor dominates, for decoupling and higher frequency filters. Special low-loss (usually higher cost) ceramic and mica capacitors are available for very high frequency applications and microwave circuits.

For best EMC performance, it is important to have a low ESR (equivalent series resistance) value as this provides a higher attenuation to signals, especially frequencies close to the self-resonant frequency of the capacitor in use.

Bypass capacitors

The main function of the bypass capacitor is to create an AC shunt to remove undesirable energy from entering susceptible areas. The bypass capacitor is acting as a high frequency bypass source to reduce the transient circuit demand on the power supply unit. Usually, the aluminium or tantalum capacitor is a good choice for bypass capacitors, its value depends on the transient current demand on the PCB, but it is usually in the range of 10 to 470μF. Larger values are required on PCBs with a large number of integrated circuits, fast switching circuits, and PSUs having long leads to the PCB.

Decoupling capacitors

During active device switching, the high frequency switching noise created is distributed along the power supply lines. The main function of the decoupling capacitor is to provide a localized source of DC power for the active devices, thus reducing the switching noise propagating across the board and decoupling the noise to ground.

Ideally, the bypass and decoupling should be placed as close as possible to the power supply inlet to help filter high frequency noise. The value of the decoupling capacitor is approximately 1/100 to 1/1000 of the bypass capacitor. For better EMC performance, decoupling capacitors should placed as close as possible to each IC, because track impedance will reduce the effectiveness of the decoupling function.

Ceramic capacitors are usually selected for decoupling; choosing a value depends on the rise and fall times of the fastest signal. For example, with a 33MHz clock frequency, use 4.7nF to 100nF; with a 100MHz clock frequency, use 10nF.

Apart from the capacitive value when choosing the decoupling capacitor, the low ESR of the capacitor also affects its decoupling capabilities. For decoupling, it is preferable to choose capacitors with a ESR value below 1Ω.

Capacitor self-resonance

The following briefly discusses how to choose the value of bypass and decoupling capacitors based on their self-resonant frequency. In Figure 3, the capacitor remains capacitive up to its self-resonant frequency. After that, the capacitor turns inductive, due to its lead length and trace inductance. Table 1 lists the self-resonant frequency for two types of ceramic capacitors, one with standard 0.25 inch leads with interconnect inductance of 3.75nH and the other surface mount with interconnect inductance of 1nH. We see that the self-resonant frequency of the surface mount type is double that of the through-hole type.

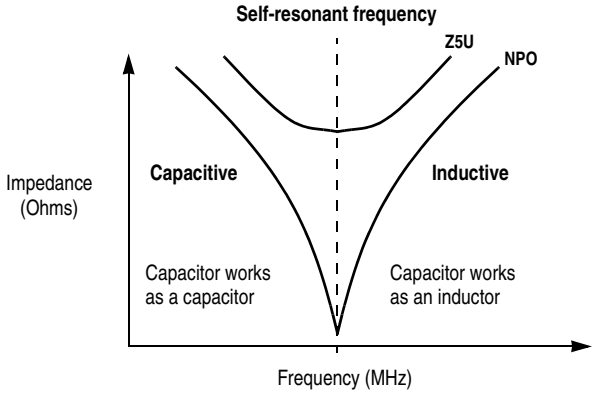

Figure 3. Impedance and Different Dielectric Materials

Table 1. Capacitor Self-Resonant Frequencies

Capacitor Value	Through-hole (0.25 leads)	Surface mount (0805)
1.0 μF	2.5 MHz	5 MHz
0.1 μF	8 MHz	16 MHz
0.01 μF	25 MHz	50 MHz
1000 pF	80 MHz	160 MHz
100 pF	250 MHz	500 MHz
10 pF	800 MHz	1.6 GHz

Another factor that affect the effectiveness of the decoupling capacitor is the dielectric material of the capacitor. Two common materials are used in the manufacture of decoupling capacitors: barium titanate ceramic (Z5U) and strontium titanate (NPO). Z5U has a larger dielectric constant, with a self-resonant frequency from 1 MHz to 20 MHz. NPO has a lower dielectric constant, but a higher self-resonant frequency (greater than 10 MHz). Therefore, Z5U is more suitable for low frequency decoupling, while NPO is good for decoupling at over 50 MHz.

A common practice is to use two decoupling capacitors in parallel. This configuration can provide a wider spectral distribution to reduce the switching noise induced by the power supply networks. Multiple decoupling capacitors connected in parallel can provide 6 dB improvement to suppress RF currents generated by active device switching.

The multiple decoupling capacitors not only provide wider spectral distribution, but also provide greater trace width such that to reduce lead inductance. Therefore, it will significantly improves the effectiveness of decoupling. The value of the two capacitors should differ by two orders of magnitude to provide effective decoupling (e.g. 0.1 μF + 0.001 μF connected in parallel).

A point should be noted for digital circuit decoupling. A low ESR value is more important than the self-resonant frequency because a low ESR value can provide a lower impedance path to ground such that to provide adequate decoupling by the capacitor when the capacitor becomes inductive when over the self-resonant frequency.

Inductors

The inductor is the component which forms a link between magnetic and electric fields, hence are potentially more susceptible than other components as they have an inherent ability to interact with magnetic fields. Similar to capacitors, the inductor, when used intelligently, can provide a cure to many EMC problems.

There are basically two types of inductors: open-loop and closed-loop. Their difference is in their magnetic field loop. In the open-loop design, the magnetic field passes through air to complete its field, while in the closed-loop design, the magnetic field flows through its core material to complete the magnetic circuit. This is illustrated in Figure 4.

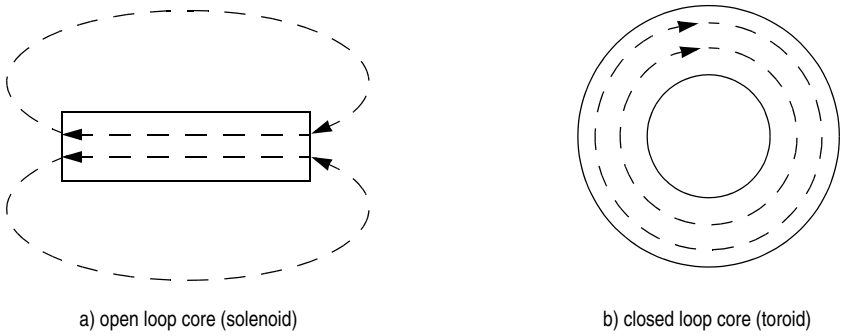

Figure 4. Magnetic Field in Inductor Core

One advantage of the inductor over the capacitor or resistor is that there are no parasitic inductance, hence there is very little difference between surface mounts and the leaded types.

Since the magnetic field of the open-loop inductor passes through air, this causes radiation and can cause EMI problems. For the choice of open-loop inductors, the bobbin type is better than the rod or solenoid type because the magnetic field is controlled by the core (i.e. localized magnetic field within the core).

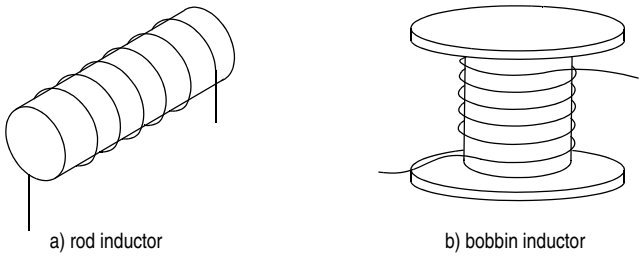

Figure 5. Open Loop Inductors

For the closed-loop inductor, the magnetic field is totally controlled by the core. Therefore, this type of inductor is more ideal in circuit designs, except they are more expensive. One advantage of the toroid shape of the closed-loop inductor is that it not only keeps the magnetic loop within the core, it also has a self-cancelling effect on any incident field radiating into the inductor.

There are two types of core material for the inductor: iron and ferrite. Iron core inductors are used for low frequency applications (tens of kHz) while ferrite core inductors are used for high frequency applications (to MHz). Therefore, the ferrite core inductor is more suitable for EMC applications.

There are two special types of inductor that are used specifically in EMC applications: ferrite beads and ferrite clamps.

The ferrite bead is a single turn inductor and is usually a single lead through the ferrite material to form the one turn. This device provides 10dB attenuation over the high frequency range, and a low attenuation at DC.

Similar to the ferrite bead, the ferrite clamp provides 10 to 20dB attenuation in both common mode (CM) and differential mode (DM) in the higher MHz region.

In DC-DC converter applications, the inductor must have low emissions and be able to handle high saturation currents. Based on these requirements, the bobbin shape inductor has these characteristics to fit this application. In power supply applications, a LC filter is needed to provide impedance matching between low impedance supply and high impedance digital circuit. The circuit shown in Figure 6 can be used.

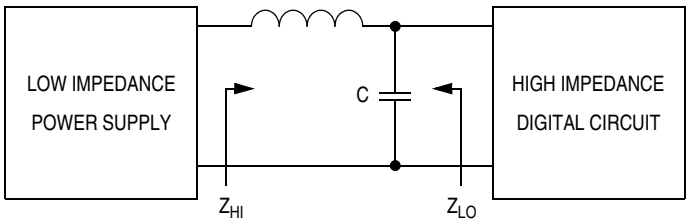

Figure 6. LC Filter

One of the most popular use of the inductor is in the AC mains filter, as shown in Figure 7.

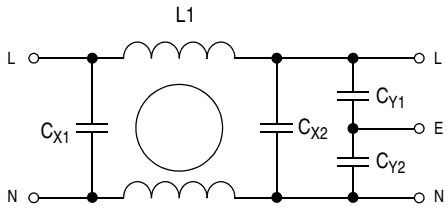

Figure 7. AC Mains Filter

In Figure 7, L1 is the common mode choke, which provide both common mode filtering by its leakage inductance and differential mode filtering by its primary inductance. L1, C_{X1}, and C_{X2} forms the differential filtering network which is to filter out noise between the supply lines. L1, C_{Y1}, and C_{Y2} forms the common mode filtering network which reduces noise from ground loops and earth offset. For a 50Ω terminating impedance, the EMI filter typically can fall-off at about 50dB/decade in differential mode and 40dB/decade in common mode.

Diodes

The diode is the simplest form of semiconductor devices. Based on their individual characteristics, some diodes can help to resolve and protect from EMI related problems. Table 2 summarizes the type of diodes.

Table 2. Diode Characteristics

	Characteristic	EMC Application	Comments
Rectifier diode	Large current; slow response; low cost.	Nil	Power supply units.
Schottky diode	Low forward voltage drop; high current density; fast reverse transient time.	Fast transient signals and spike protection.	Switched mode power supplies.
Zener diode	Operation in reverse mode; quick reverse voltage transients; clamp positive transients only; tight clamp voltage specifications (5.1 V ±2%).	ESD protection; over voltage protection; low capacitance high data rate signalling protection.	—
Light emitting diode (LED)	Forward conduction mode; no EMC impact by itself.	Nil	Radiated emission when LED is mounted on a panel at a distance away from the PCB.
Transient voltage suppressor diode (TVS)	Similar to zener diode but in an avalanche mode; wide clamp voltage tolerance (e.g. 5V means clamp between 6V to 12V); clamp positive and negative voltage transients.	High voltage transient from ESD lighting – induced transient main spikes.	—
Varistor diode (VDR: voltage dependent resistor) (MOV: metal oxide varistor)	Metal coated ceramic pills (each pill works as schottky diode with high potential barrier; mains line protection; fastest response to transients.	First line ESD protection; high voltage and high transient protection.	Alternative to zener or TVS.

Some diode applications

Many circuits operate with inductive loads, with high switching currents that cause transients to be generated within the system. The diode is one of the best device that can be used at the source of the noise as a transient voltage suppressor. The examples below are some transient suppression techniques using diodes.

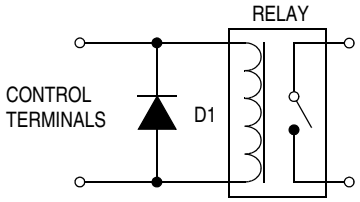

Figure 8. Relay Transient Suppression

In Figure 8, the control terminals will turn the coil on and off. The switching transient from the coil will be coupled or radiated to other parts of the circuit. The diode, D1, is used to clamp this voltage transient.

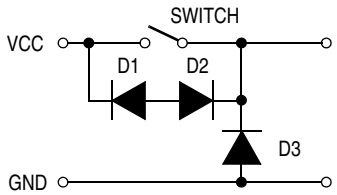

Figure 9. DC Switch Transient Suppression

The diode configuration in Figure 9 is used to suppress the voltage transients from the high-voltage switch.

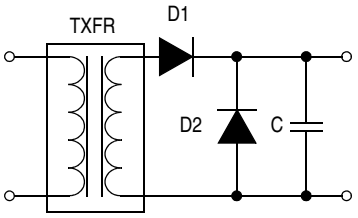

Figure 10. Transformer DC Transient Suppression

Figure 10 shows the typical transformer and rectifier configuration. D2 is a schottky or zener, used to suppress the transients after the rectifier.

In motor control applications, both brush and brushless motors will generate brush noise or commutator noise when the motor is running. Therefore, suppression diodes are necessary to reduce the noise. To improve the effectiveness of the suppression, the diodes should be placed as close as possible to the motor contacts.

In power line inlet circuits, a TVS or high voltage varistor should be used to provide the suppression.

One EMI problem in signal connector interfacing circuits is electrostatic discharge (ESD). Shielded cables or connectors can be used to as protection from external ESD. The alternative is to use TVS or varistors to protect the signal lines.

Integrated Circuits

The majority of modern digital integrated circuits (IC) are manufactured using CMOS technology. The static power consumption of CMOS devices may be lower, but with fast switching rates the CMOS device demands transient power from the supply. The dynamic power demand of a high speed clocked CMOS device may exceed an equivalent bipolar device. Therefore, decoupling capacitors must be used on these devices to reduce the transient power demand from the power supply.

Integrated circuit packages

Nowadays, there are many packages for the integrated circuit. As with discrete components, the shorter the lead, the less the EMI problem. Therefore, the surface mounts are preferred for better EMC performance because of lower package parasitics and smaller loop area. Further improvements are the use of die bonds, directly on the PCB.

The pin assignment of an IC can also affect EMC performance. ICs with supply lines near the center of the package provide the shortest length from the die to pin, and thus have lower lead inductance. Adjacent VCC and GND pins make decoupling capacitor placement easier and more effective (small loop area).

The clock circuit is a major factor that affects EMC performance of both integrated circuits and the PCB or the whole system. Most of the noise from ICs are related to the clock frequency and its harmonic content. Therefore, both circuit design and PCB layout techniques should be applied to the system clock circuit to minimize the noise generated. Good grounding, adequate decoupling capacitors, and bypass capacitors can reduce emissions. The use of high impedance buffers for clock distribution also help to reduce any reflections and ringing from the clock signals.

For combination logic circuits, clock jitter, signal and power line harmonics may occur when mixed logic families are used, such as TTL and CMOS. This is mainly due to their different switching thresholds. Therefore, the best way to avoid these potential problems is to use ICs from one logic family. Nowadays, most designers would choose CMOS devices because they have a higher noise margin. It is also the preferred logic family for interfacing with microcontrollers, as they are also manufactured using CMOS technology. One important point regarding CMOS devices is that unused input pins should be tied either to the power rail or ground. In MCU circuits, noisy environments may cause these unterminated inputs to behave erratically, and cause the MCU to execute runaway code.

Voltage Regulators

For the typical regulator circuit, adequate decoupling capacitors should be placed as close as possible to the output of the regulator because the distance between the output of the regulator and the load will create an inductive effect in the trace and causes internal oscillation of the regulator. Typically, a 0.1 μF decoupling capacitor is added to both input and output of the regulator to prevent possible internal oscillation and to filter high frequency noise. In addition, a relatively large bypass capacitor should be added (10 μF per ampere) to reduce output ripple. Figure 11 shows the bypass and decoupling capacitors for the regulator. The capacitors should be placed as close as possible to the regulator device.

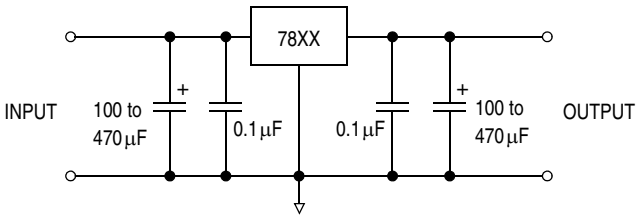

Figure 11. Regulator Bypass and Decoupling

Line Terminations

When a circuit is operating at high speeds, the impedance matching between the source and destination is very important. Because mismatching will cause signal reflection and ringing. The excess RF energy will radiate or couple to other parts of the circuit, causing EMI problems. Termination of signals help to reduce these undesirable effects.

Termination not only reduce signal reflection and ringing by matching the impedance between source and destination, but can also to slow down the fast rising and falling edges of the signals.

There are several termination methods, each has its advantages and disadvantages. Table 3 lists a summary of the termination methods.

Table 3. Summary of Termination Methods

Termination Type	Relative Cost	Delay Added	Power Required	Critical Parameters	Characteristics
Series	Low	Yes	Low	$R_S = Z_0 = R_0$	Good DC noise margin
Parallel	Low	Small	High	$R = Z_0$	Power consumption is a problem
RC	Medium	Small	Medium	$R = Z_0$ C = 20 to 600pF	Check bandwidth and added capacitance
Thevenin	Medium	Small	High	$R = 2 \times Z_0$	High power for CMOS
Diode	High	Small	Low	—	Limits overshoot; some ringing at diodes

Series/Source termination

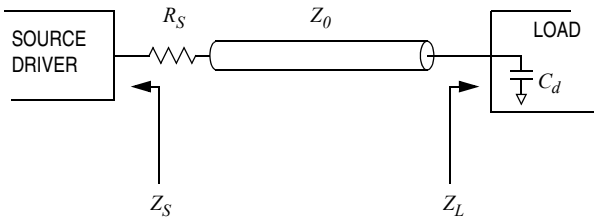

Figure 12. Series Termination Circuit

Figure 12 shows the series/source termination method. The source termination resistor, R_S, is added to achieve impedance matching between the source, Z_S, and the distributed trace, Z_0. It can also absorb reflection from the load.

R_S must be placed as close as possible to the source driver. The value of R_S is the real part in the equation: $R_S = (Z_0 - Z_S)$. Typically, R_S equals to approximately 15 to 75Ω.

Parallel termination

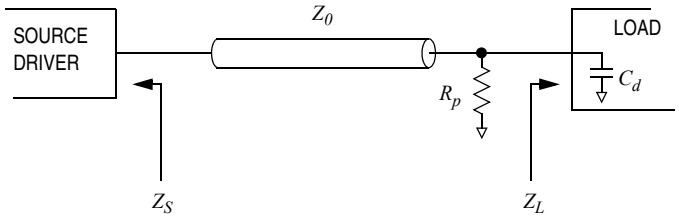

Figure 13. Parallel Termination Circuit

Figure 13 shows the parallel termination method. The parallel termination resistor, R_P, is added, such that $R_P // Z_L$ is matched with Z_0. But this method is not suitable for hand-held products, because of the low value of R_P (typically 50Ω), and will consume high power and requires the source driver to drive a high current (100mA @ 5V, 50Ω). This method also adds a small delay by $Z_{0L} \times C_d$, where $Z_{0L} = R_P // Z_L$ and C_d is the input shunt capacitance of the load.

RC termination

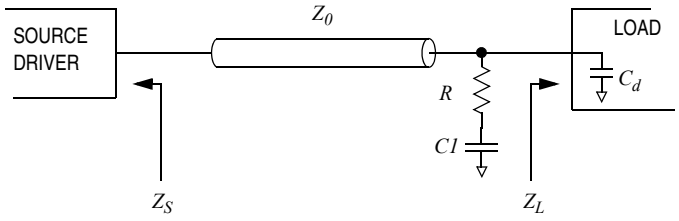

Figure 14. RC Termination

Figure 14 shows the RC termination method. Similar to parallel termination, but with addition of $C1$. The R is same as the parallel termination to provide impedance matching with Z_0, and $C1$ provides the drive current to drive the R and filter out the RF energy from the trace to ground. Therefore, the RC termination need less source driver current than the parallel termination.

Values R and $C1$ depends on Z_0, Tpd (round trip propagation delay), and C_d.

Time constant, $RC = 3 \times Tpd$, where $R // Z_L = Z_0$, $C = C1 // C_d$

Thevenin termination

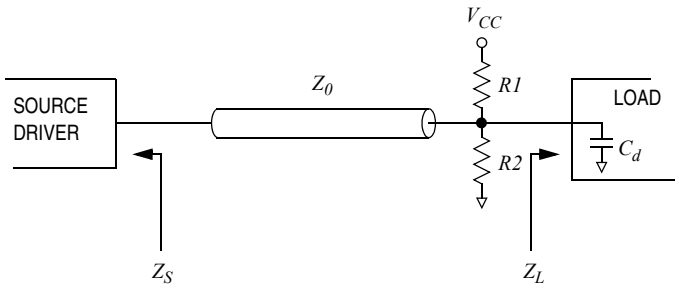

Figure 15. Thevenin Termination Circuit

Figure 15 shows the thevenin termination method. It is formed by the $R1$ pull-up and $R2$ pull-down resistors, such that the logic high and low can meet the requirement of the destination load.

The value of $R1$ and $R2$ can be determined by $R1 // R2 = Z_0$.

$R1 + R2 + Z_L$ is such that the maximum current cannot exceed the source driver capability.

For example, $R1$= 220Ω, $R2$ = 330Ω

$$V_{ref} = \frac{R2}{R1 + R2} \times VCC = \frac{330}{330 + 220} \times 5 = 3\text{V}$$

where VCC is the supply voltage.

Diode termination

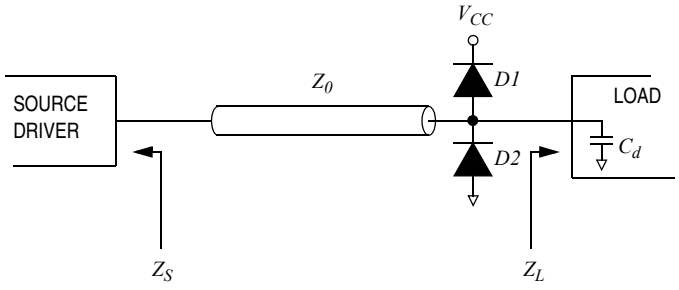

Figure 16. Diode Termination

Figure 16 shows the diode termination method. It is similar to the thevenin termination, except that the resistors are replaced by diodes, which has a lower power consumption. The $D1$ and $D2$ configuration is used to limit overshoots of the reflected signal from the load. The diodes do not affect the line impedance, unlike the thevenin termination. Schottky and fast switching diodes are good choice to use for this type of termination.

The advantage of this termination is that Z_0 does not need to be known, and it can be used in conjunction with other types of terminations. This termination is commonly used inside MCUs for protection of I/O ports.

Microcontroller Circuits

Nowadays, many IC manufacturers continually reduce the die size of the microcontroller to achieve more parts per silicon wafer. Reduced die size usually results in faster transistors. Consequently, although the MCU clock rate may not increase, the rise and fall times will increase and the harmonic content will therefore move up the frequency scale. In many cases, the reduction in die size may not be communicated to the user, hence, a MCU may initially be fine in a circuit, then sometime during its production life cycle EMC problems could arise. The best way to adapt to a possible die shrink is to design a clean circuit from the start.

Many real-time applications require high-speed MCUs, the designer must take care of their circuit design and PCB layout to reduce potential EMC problems. The electrical power required by MCUs increase as their processing power increases. It is not uncommon to have a supply circuit (e.g. a regulator) very close to the microcontroller, with a separate bypass capacitor to reduce its effect on the DC supply to other circuits.

MCUs usually have an on-chip oscillator, that requires its own crystal or resonator connection, and avoids using clocks from other clock driver circuits. This independent clock allows better immunity from noise radiated from other parts of the system. The MCU is usually the highest power demand device at the clock frequency, hence locating the clock close to the MCU ensures minimum drive demand at the clock frequency.

I/O port pins

With most MCUs, pins are usually high impedance inputs or mixed inputs/outputs. High impedance input pins are susceptible to noise and can register false levels if not properly terminated. Pins which are inputs and not internally terminated need some high resistance (e.g. 4.7kΩ or 10kΩ resistor) attached to each pin to ground or supply to ensure a known logic state. Unconnected input pins often float to the mid-point of the supply rail or to an undefined voltage due to internal leakage paths.

For the IRQ or reset pins (input pins) the termination is more important than the general I/O ports. If noise causes these two pins to mis-trigger it will have a catastrophic effect on circuit behavior. A high current consumption is often observed, particularly in CMOS devices, when the input pins are unconnected, as the input latch is half open, half closed, resulting in a leakage current internal to the IC. Terminating high impedance input pins can therefore lead to a reduction in supply current, as well as other EMC benefits.

IRQ pin

Owing to the effects that interrupts have on MCU operation this is one of the most sensitive pins on the device. The IRQ could be polled from devices at a distance to the MCU on the PCB, or even on a plug-in adapter or subsystem cards. Consequently, it is important to ensure that any line connecting to an interrupt request is protected against ESD transients. Bidirectional diodes, transorbs or metal oxide varistor terminations on the IRQ line are usually adequate for ESD and will help reduce overshoot and ringing without producing a significant line load. For cost sensitive applications, a resistive termination will also maintain the IRQ line in a fixed state.

Reset pin

Improper resets can cause many problems since different applications impose very different conditions on the start up and power down of the MCU. Reset in its most basic function ensures that the MCU starts executing code in a controlled manner once power is applied.

At power on, the supply rises to the MCU operating voltage, and it will be some time before the oscillator becomes stable. Therefore, it is necessary to have some time delay on the reset pin. The simplest delay is a resistor-capacitor (RC) network, where the capacitor is charged up by the current flowing through the resistor until it reaches a level detected by the MCU reset pin circuitry as a logic 1 state.

Ideally there are no restrictions on the values of the resistors and capacitors, but there are other considerations. Internal leakage currents for the reset pin are normally specified at 1 μA (for Freescale HC08 MCU) maximum, which means that the resistor has a maximum value of 100 kΩ and the capacitor should not be an electrolytic type, keeping the stop current to a minimum. Ceramic capacitors are recommended as a compromise between low cost, low leakage, and good high-frequency response. The reset pin capacitance is very low (less than 5 pF for Freescale HC08 MCU). There are also limits for the minimum resistor impedance since the maximum pull-down current is approximately 5 mA at 1 V (V_{OL}). Together with the low impedance voltage source of the external capacitor, it is necessary to ensure a minimum pull-up resistor value of 2 kΩ.

A diode to clamp the voltage of the reset pin is also recommended to prevent the voltage from exceeding the supply voltage and also to provide a faster discharge for the capacitor when the supply is removed.

Oscillators

Many MCUs incorporate an inverting amplifier for use with an external crystal or ceramic resonator in a Pierce oscillator configuration. The following discusses the minimum gain (transconductance) of the amplifier required to ensure oscillation with specific external components.

Figure 17 shows the typical standard Pierce oscillator configuration used on MCUs for crystals in the 1MHz to 20MHz frequency range. The circuit internal to the MCU is shown in simplified form as a NAND gate followed by an inverter. The NAND gate has two inputs; one is connected to the MCU pin called OSC1 and the other input is connected to the inverted internal STOP signal.

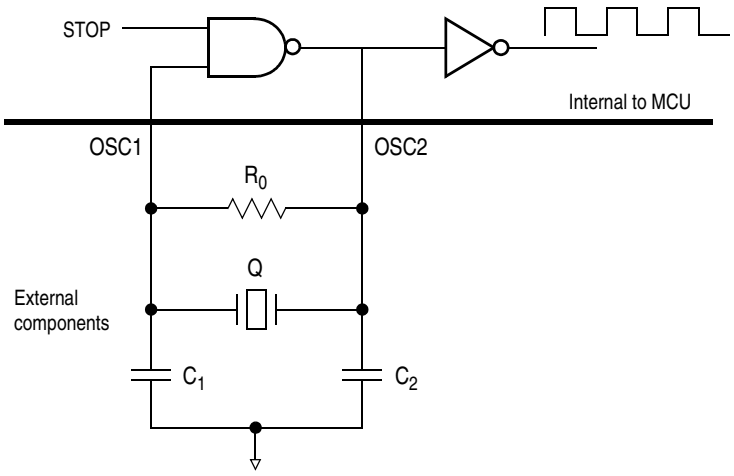

Figure 17. Standard Pierce Oscillator for 1MHz to 20MHz Operation

For the circuit to oscillate, there must be positive feedback and the closed-loop gain must be greater than unity. Resistor R_0 results in negative feedback which increases the open-loop gain requirement of the amplifier. R_0 is usually made as large as possible to minimize the feedback whilst still overcoming leakage currents at start-up. When using a crystal between 1 MHz and 20 MHz, R_0 should be in the range of 1 MΩ to 10 MΩ. For ceramic resonators, a R_0 of 1 MΩ is normally used.

The resonator Q and capacitors $C1$ and $C2$ form the resonant circuit. $C1$ and $C2$ represent the external capacitors and any stray capacitance in parallel. A crystal or ceramic resonator has the small signal equivalent circuit shown in Figure 18.

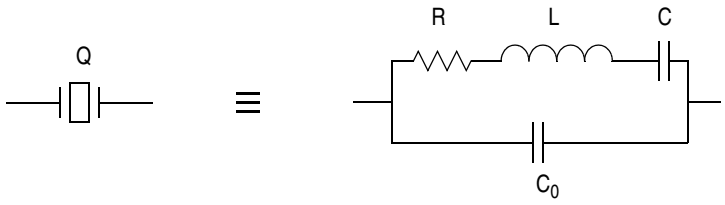

Figure 18. Crystal Equivalent Circuit

R is called the series resistance, L and C are called the motional or series inductance and capacitance, respectively. C_0 is the shunt capacitance, it represents the sum of the low-frequency parallel plate capacitance of the resonator and the stray capacitance of the crystal holder. Any additional stray capacitance between the OSC1 and OSC2 pins should be included into this value.

Values for R, L, C and C_0 for a particular crystal are specified in the crystal manufacturer's data sheet. In order to measure these values, the manufacturer must apply a signal to the crystal, i.e. the values are obtained at a particular level of power dissipation in the crystal. However, at the start-up of the oscillator, the only signal across the crystal is due to thermal (Johnson) noise, so the power dissipation in the crystal is extremely low. It is known that the effective value of R may increase as the power dissipated in the crystal decreases to low levels. The maximum value of R is therefore estimated by the crystal manufacturer.

Since the value of the R_0, $C1$, and $C2$ not only depends on the inverter characteristic of the MCU but also on the characteristic of the external crystal or ceramic resonator, the exact component configuration should be deduced from manufacturer's data sheets.

PART 3:
PRINTED CIRCUIT BOARD LAYOUT TECHNIQUES

In addition to component selection and circuit design, good printed circuit board (PCB) layout is an important factor in EMC performance. Since the PCB is an inherent part of the system, EMC enhancements by PCB layout does not add extra cost towards the finish product.

One point to note is that there are no fast and strict rules for PCB layout. There is no single rule that covers all PCB layouts. Most PCB layouts are restricted by board size and the number of copper layers. Some layout techniques may apply to one type of circuit but not another. Much of it will depend on the experience of the PCB layout engineer.

Nevertheless, there are some general rules. These are discussed in the following sections. These should be treated as general guidelines. One must remember that poor PCB layouts can cause more EMC problems than it can cure, and in many cases, adding filters and components cannot solve the problem. In the end, it may be better to do a complete re-layout of the board. Therefore, good PCB layout practice at the outset is the best cost saving method.

PCB Basic Characteristics

A PCB is constructed using a series of laminates, tracking and prepreg layers in a vertical stack. In multi-layer PCBs, most designers will place the signalling tracking on either outer layer for easier debugging of the board.

A track on the PCB has resistance, capacitance, and inductance.

- Resistance: the resistance of the track is determined by the weight of copper and cross-sectional area. For example, there are 0.49 mΩ/unit area in 1 oz. copper weight.
- Capacitance: the capacitance of the track is determined by the dielectric ($EoEr$), coverage area (A), and distance between track (h).
  The equation is $C = EoErA/h$, where Eo is the dielectric constant of free space (8.854 pF/m) and Er is the relative dielectric constant of the PCB substrate (4.7 for FR4 laminate).
- Inductance: the inductance of the track is evenly distributed in the track at approximately 1 nH/m.

For a 1 oz. copper track, 0.5 mm (20 mil) width, 20 mm (800 mil) long over ground plane on a 0.25 mm (10 mil) thick FR4 laminate would exhibit a resistance of 9.8 mΩ, an inductance of 20 nH and a capacitance coupling to ground of 1.66 pF.

Comparing the above values with component parasitics, these can be neglected, but the sum of all the tracks may exceed component parasitics. Therefore, the designer must take this into consideration.

The following are some general guidelines for PCB layout:

- Increase the separation between tracks to minimize crosstalk by capacitive coupling.
- Maximize the PCB capacitance by placing the power and ground in parallel.
- Place sensitive and high frequency tracks far away from high noise power tracks.
- Widen ground and power tracks to reduce the impedance of both power and ground lines.

Segmentation

Segmentation is the use of physical separation to reduce the coupling between different types of circuit, particularly by the power and ground tracks.

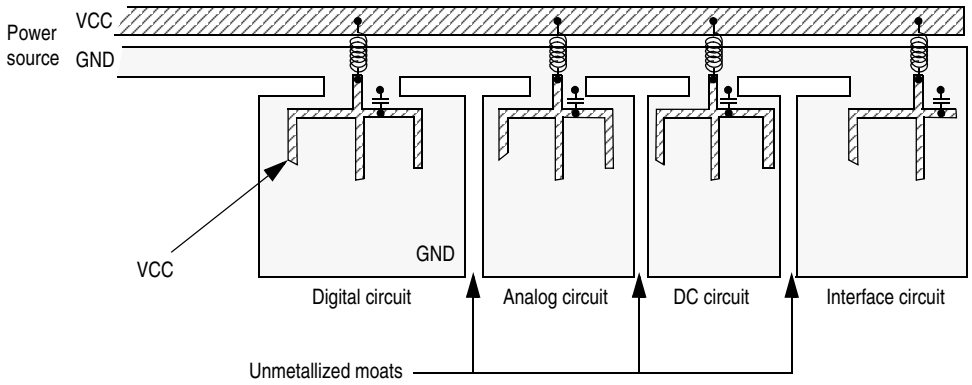

Figure 19. Separated Function Blocks

Figure 19 shows a typical example of separating four different circuits using the segmentation technique. In the ground plane, the unmetallized moat is used to isolate the four ground planes. The L and C provide filtering for each part of the board, coupling between different circuit power planes is reduced. High speed digital circuits need to be placed near the power supply inlet because of their higher transient power demand. The interface circuit may require ESD and transient suppression components and circuits. For the L and C, it is better to use different values of L and C filter components instead of one large L and C because they can provide different filtering characteristics for different circuits.

Decouple Local Supplies and ICs

Localized decoupling can reduce noise propagating along the supply rail. The use of large bypass capacitors connected at supply entry to the PCB will help as a low frequency ripple filter and potential reservoir for sudden power demands. In addition, decoupling capacitors should be connected between power and ground at each IC, as close as possible to the pins. This helps to filter out switching noises from the IC.

RF Current in Reference Plane

Whether with the reference ground plane on multi-layer PCBs or ground traces on single-layer PCBs, a current path is present from the load back to the power supply source. The lower the impedance of the return path the better the EMC performance of the PCB. Long return paths can create mutual coupling because of the RF current from load to source. Therefore, the return path should be as short as possible, the loop area as small as possible.

Trace Separation

Trace separation is used to minimize the crosstalk and noise coupling (by magnetic flux coupling) between adjacent traces on the same PCB layer.

The 3W rule states that all signals (clocks, video, audio, reset, etc.) must be separated between traces, edge-to-edge as shown Figure 20. To further minimize magnetic coupling, place reference grounds near critical signals to isolate other noise being coupled onto the signal lines.

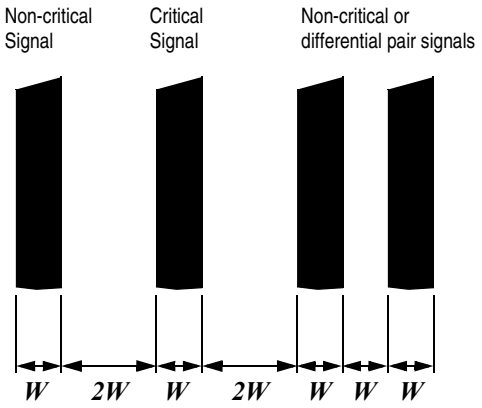

Figure 20. Trace Separation

Guard and Shunt Traces

In clock circuits, local decoupling capacitors are very important to reduce noise propagating along the supply rail. But the clock lines also need protection from other EMI sources, otherwise jittering clock signals will cause problems elsewhere in the circuit.

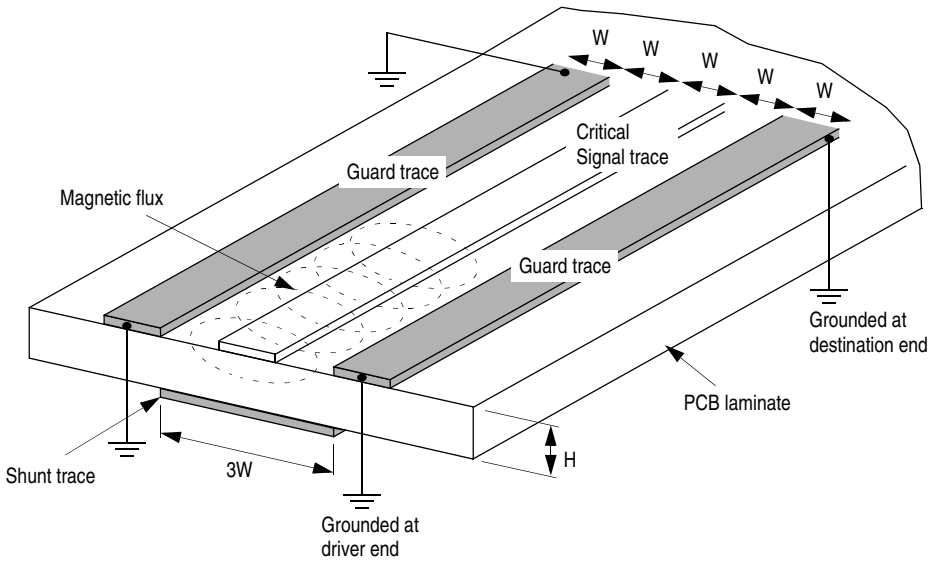

Figure 21. Shunt and Guard Traces

Shunt trace and guard trace are effective methods to isolate and protect critical signal traces such as the system clock from a noisy environment. In Figure 21, the shunt trace or the guard trace are placed along with the critical signal trace in the PCB. The guard not only isolate the magnetic flux coupling from other signal traces, but also isolate the critical signal from coupling to other traces.

The difference between the shunt trace and the guard trace is that the shunt trace does not need to be terminated (connected to ground), but the guard trace must be connected to ground at both ends. To further reduce the coupling, a number of vias to ground can be added at intervals on the guard trace on multi-layer PCBs.

Grounding Techniques

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

Ground track in single-layer PCBs

On a single-layer (single sided) PCB, the width of the ground track should be as wide as possible, at least 1.5mm (60mil). Since the star arrangement is impossible on single-layer PCBs, the use of jumpers and changes in ground track width should be kept to a minimum, as these cause change in track impedance and inductance.

Ground track in double-layer PCBs

On a double-layer (double sided) PCB, the ground grid/matrix arrangement is preferred for digital circuits because this arrangement can reduce ground impedance, ground loops, and signal return loops. As with the single-layer PCBs, the width of the ground and power tracks should be at least 1.5mm.

Another scheme is to have a ground plane on one side, the signal and power line on the other side. In this arrangement the ground return path and impedance will be further reduced and decoupling capacitors can be placed as close as possible between the IC supply line and the ground plane.

Guard ring

The guard ring is a grounding technique that can isolate the noisy environment (e.g. RF current) outside the ring, because there is no current flowing through the guard ring in normal operation (see Figure 22).

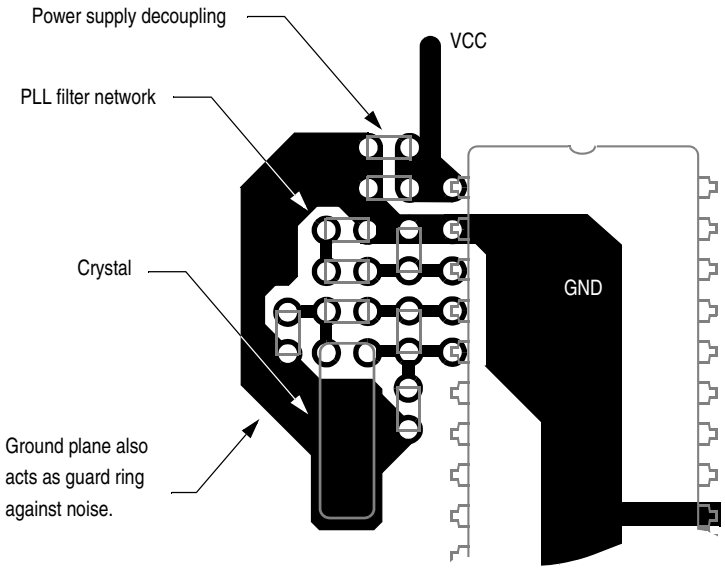

Figure 22. Guard Ring

PCB capacitor

On a multi-layer board, a PCB capacitor is created by the thin laminate separating the power and ground planes. On a single-layer board, this capacitive effect is also achieved by running the power and ground traces in parallel. The advantages of the PCB capacitor is that it has a very high frequency response and low series inductance that is evenly distributed along the plane or trace. In effect, it is an evenly distributed decoupling capacitor on the whole board. No single discrete component has these characteristics.

Fast circuit and slow circuits

High speed circuits should be placed closer to the ground plane while the slower circuits can be placed close to the power plane.

Ground copper fills

In some analog circuits, unused board areas are covered with a large ground plane such that it provides shielding and improve decoupling. But if the copper area is floating (i.e. not connected to ground), it may act as an antenna, and it will cause EMC problems.

Ground and power planes in multi-layer PCBs

In multi-layer PCBs, it is preferable to place the power and ground planes as close as possible on adjacent layers to create a large PCB capacitor over the board. The fastest and critical signals should be placed on the side which is adjacent to the ground plane, while non-critical signals placed near the power plane. Figure 23 shows the typical multi-layer board track arrangement.

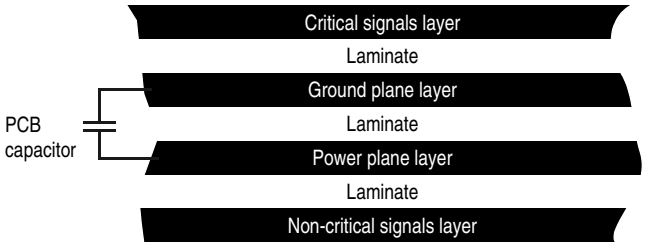

Figure 23. Tracking Arrangement on Multi-Layer PCBs

Multi-power requirements

When the circuit requires more than one power supply, the idea is to keep each power separated by a ground plane. But on a single-layer PCB, multi-ground planes are not possible. One solution is by running power and ground tracks for one supply separated from the others (see Figure 24). This still helps to avoid noise coupling from one power source to the other.

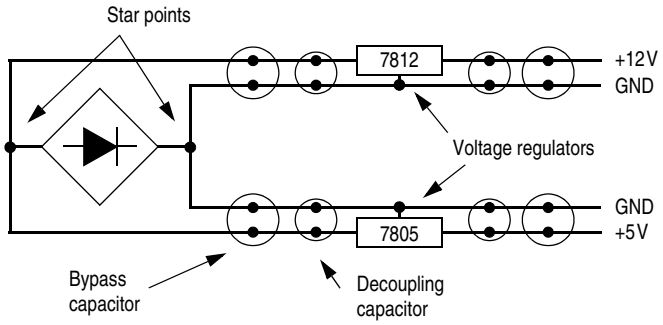

Figure 24. Multiple Power Sources

Tracking Layout Techniques

The following sections discuss some rules on PCB tracking.

Vias

Vias or via holes are commonly used for multi-layer PCBs. On high speed signals, a via introduces 1 to 4 nH of inductance and 0.3 to 0.8 pF of capacitance to the track. Hence, vias should be kept to an absolute minimum when laying high speed signal tracks. If layer changes are unavoidable on high-speed parallel lines (e.g. address and data lines), make sure the number of vias are the same on each signal line.

45° angled tracking

Similar to vias, right-angled track turns should be avoided because it can produce a field concentration at the inner edge. This field can cause noise that can be coupled to nearby tracks. Therefore, all orthogonal tracking should be 45° when making turns. Figure 25 is the general rule for 45° tracking.

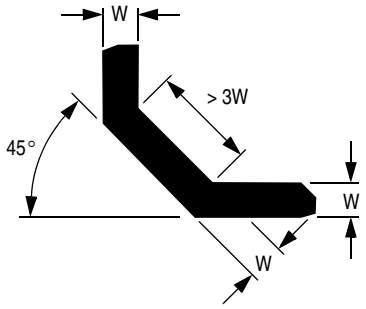

Figure 25. Angled Tracks

Stubs

Stubs produce reflections as well as the potential of adding wavelength divisible aerials to the circuit. Although a stub length may compute to be a non-quarter wavelength integer of any known signal in the system, incident radiation may resonate on a stub. Therefore, avoid producing stubs with tracks carrying high frequency and sensitive signals.

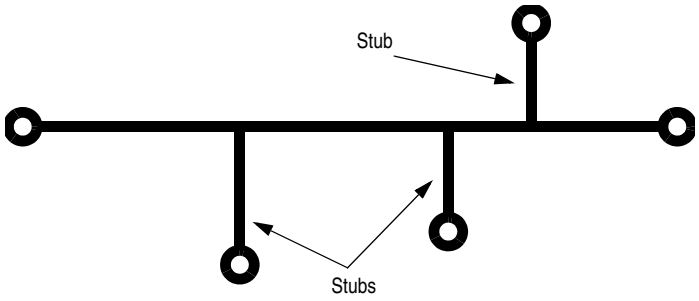

Figure 26. Stub Lines

Star signal arrangement

Although star arrangements are suitable for bonding ground rails from multiple PCBs, with a signal track this introduces multiple stubs. Therefore, the star arrangement should be avoided for high speed and sensitive signals.

Radiating signal arrangement

A radiating signal arrangement is usually the shortest tracking and causes minimum delay from source to all receivers, but this can also cause multiple reflections and radiated interference. Again, this should be avoided for high speed and sensitive signals.

Constant track width

The width of a signal track should be constant from driver to load. Varying track width creates changes in track impedance (resistance, inductance, and capacitance) and, consequently, can cause reflections and line impedance imbalances. It is better to keep a track thin rather than vary its width.

Hole and via concentrations

A concentration of via holes that pass through the power and ground planes produce a localized impedance difference near the holes. The area not only becomes a “hot spot” of signal activity, but the supply planes are high impedance at this point and less effective as RF sinks.

Split apertures

This is the same with hole and via concentrations, split apertures (i.e. long holes or wide vias) in power and ground planes create an area of non-uniformity within the planes and reduce their effectiveness as shields, as well as locally increasing the impedance of the power and ground planes.

Ground metallized patterns

All metallized patterns should be connected to ground, otherwise these large metal areas can act as radiating aerials.

Minimize loop areas

Keeping signal tracks and its ground return close together will help to minimize the ground loop, thus, avoiding a potential aerial loops. With high speed single-ended signals, sometimes the ground return may also have to be tracked alongside the signal if the signal does not track over a low impedance ground plane (see Figure 27).

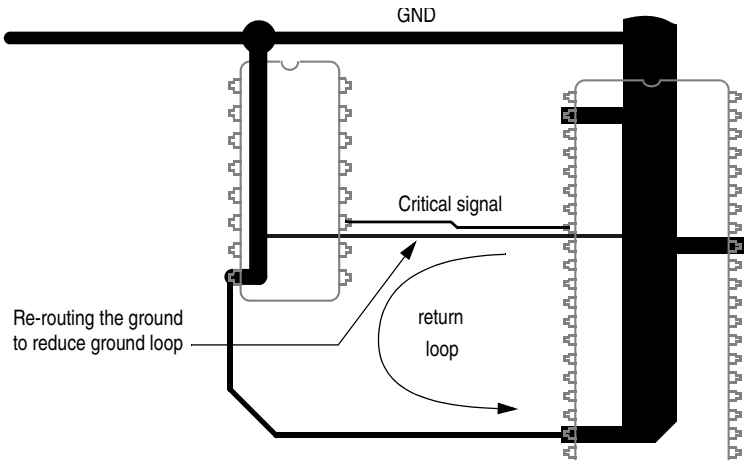

Figure 27. Ground Return Loops

PCB Example 1

Figure 28 shows some improvements on a typical printed circuit board used in a washing machine.

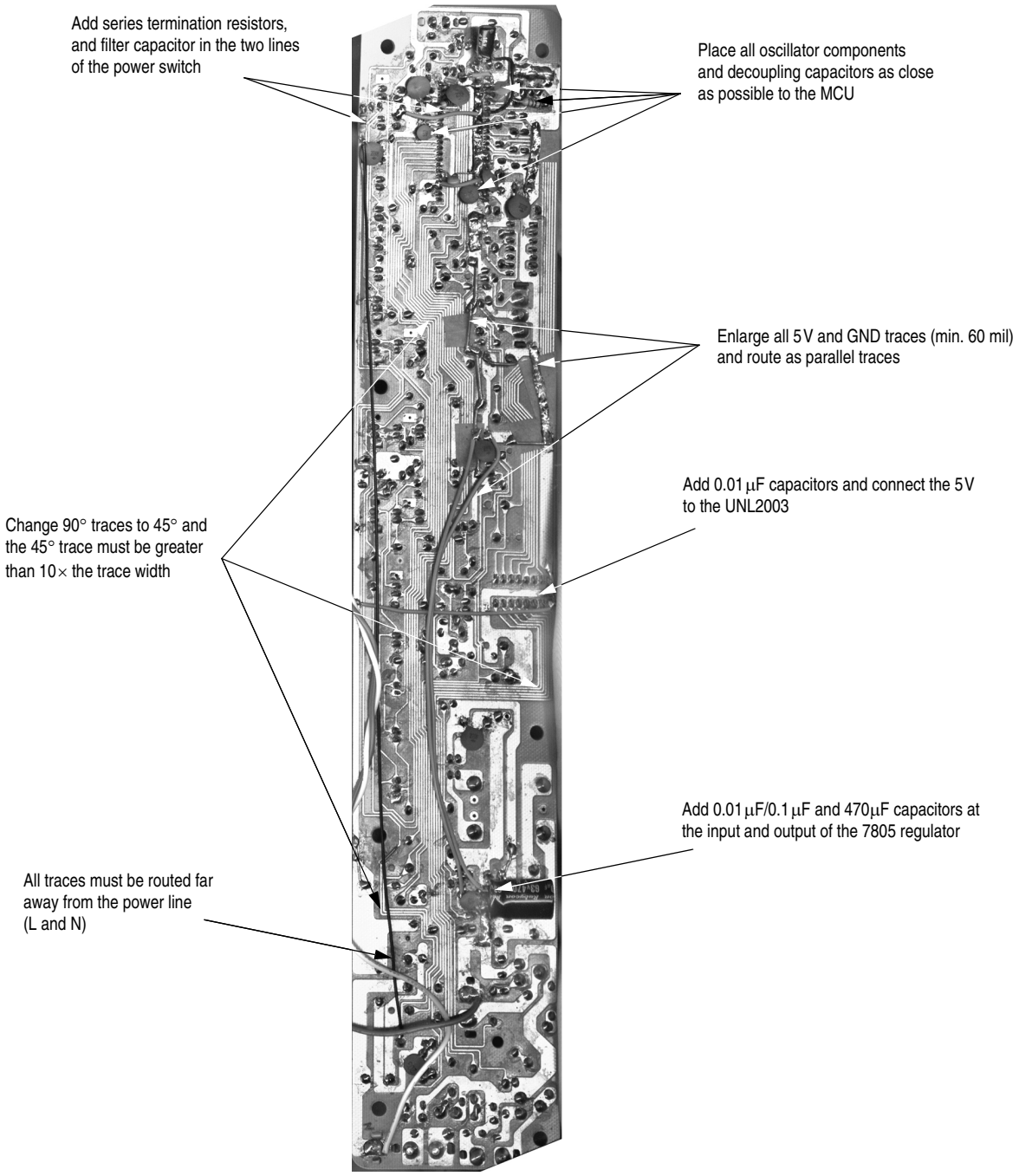

Figure 28. PCB Improvement — Example 1

PCB Example 2

Figure 29 shows some improvements on a typical printed circuit board used in an air conditioner.

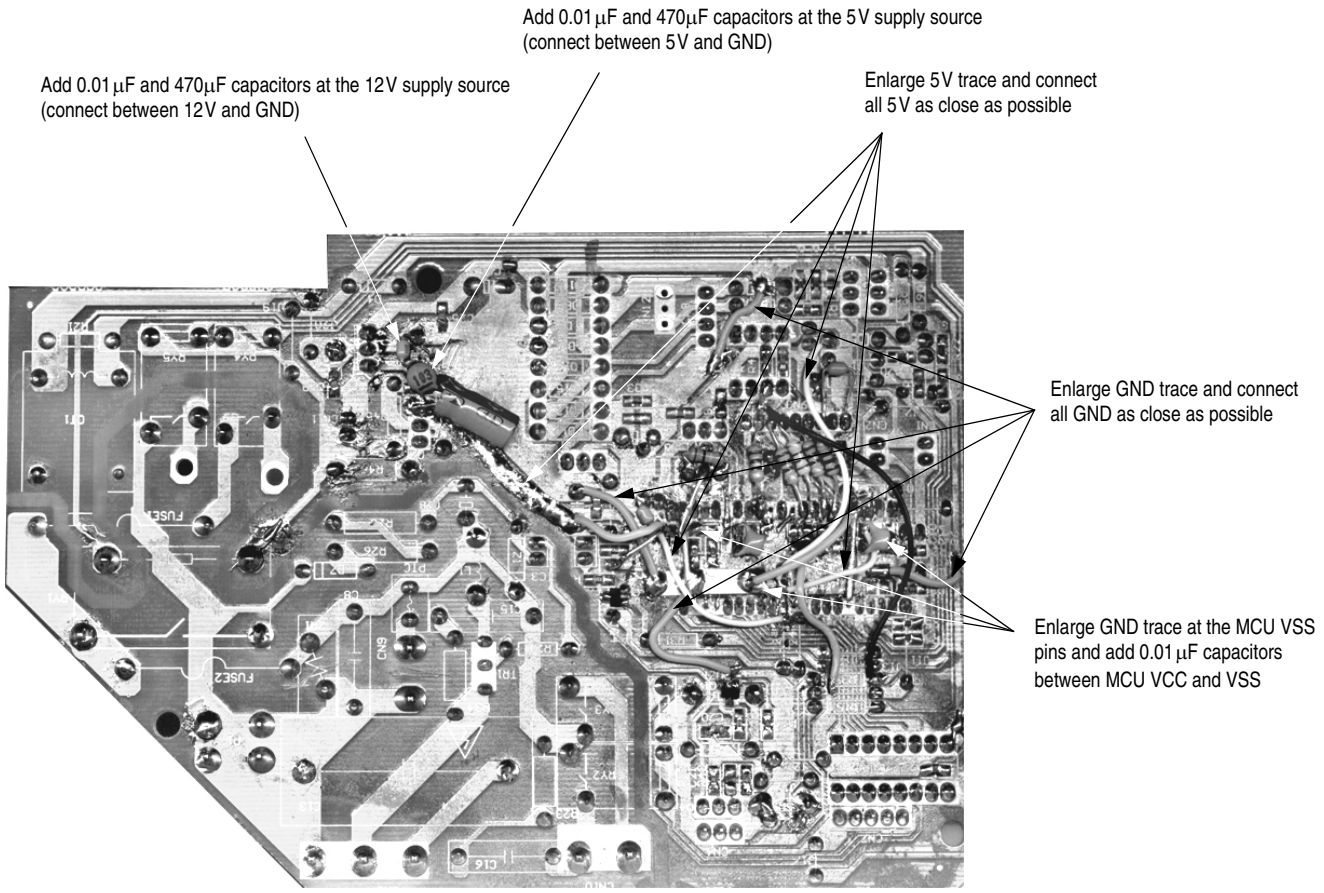

Figure 29. PCB Improvement — Example 2

APPENDIX A: GLOSSARY OF TERMS

Electromagnetic Compatibility (EMC)

The capability of electrical and electronic systems, equipment, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels or performance, without suffering or causing unacceptable degradation as a result of electromagnetic interference (ANSI C64.14-1992).

Electromagnetic Interference (EMI)

The lack of EMC, since the essence of interference is the lack of compatibility. EMI is the process by which disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths (or both). In common usage, the term refers particularly to RF signals. EMI can occur in the frequency range commonly identified as “anything greater than DC to daylight”.

Radiated Emissions

The component of RF energy that is transmitted through a medium as an electromagnetic field. RF energy is usually transmitted through free space; however, other modes of field transmissions may occur.

Conducted Emissions

The component of RF energy that is transmitted through a medium as an propagating wave, generally through a wire or interconnect cables.

Immunity

A relative measure of a device or a system’s ability to withstand EMI exposure while maintaining a predefined performance level.

Electrostatic Discharge (ESD)

A transfer of electric charge between bodies of different electrostatic potential in proximity to each other or through direct contact. This definition is observed as a high-voltage pulse that may cause damage or loss of functionality to susceptible devices. Although lightning differs in magnitude as high-voltage pulse, the term ESD is generally applied to events of lesser amperage and more specifically to events triggered by human beings.

Radiated Immunity

A product’s relative ability to withstand electromagnetic energy that arrives via free-space propagation.

Conducted Immunity

A product’s relative ability to withstand electromagnetic energy that penetrates it through external cables, power cords, I/O interconnects, or chassis. EMI may couple to a chassis, if interconnects are improperly implemented.

Susceptibility

A relative measure of a device or system’s propensity to be disrupted of damaged by EMI exposure to an incident field or signal. It is the lack of immunity.

APPENDIX B: IMMUNITY MEASUREMENT STANDARDS

Immunity to Electrostatic Discharge: IEC 1000-4-2

The purpose of this test is to verify the product's immunity against Electrostatic Discharge (ESD) generated by objects or persons coming into contact with, or in the vicinity of the device. Persons or objects can accumulate electrostatic charges which can reach to voltages above 15 kV. Experience has shown that many unexplained malfunctions and damages are likely to have been caused by ESD.

The equipment under test (EUT) is subjected to ESD events by applying the discharge from the ESD simulator to the surfaces of the EUT and in proximity to the EUT. The severity level of the discharges is specified in the product standard and the EMC test plan prepared by the manufacturer. The EUT is investigated for malfunction or disturbance to all its operating modes. The pass/fail criteria must be defined in the EMC test plan and are determined by the manufacturer of the product.

Immunity to Conducted Electrical Fast Transients (EFT/B): IEC 1000-4-4

The purpose of this test is to verify the EUT immunity to bursts of short duration fast rise time transients that may be generated by the switching of inductive loads or contactors. The fast rise times and repetitive nature of these test pulses results in the easy penetration of these spikes into the EUT circuitry and this may disturb the EUT operation. The transients are applied directly to the mains power and capacitively to signal lines. As with other immunity tests, the test plan should require the EUT to be monitored for pass/fail criteria while configured for normal operation.

Immunity to Radiated Electromagnetic Fields: IEC 1000-4-3

The purpose of this test is to verify the immunity of the product against electromagnetic fields generated by radio transmitters, transceivers, mobile GSM/AMPS cellular phones, and various industrial electromagnetic sources. Radiated electromagnetic fields can be coupled into the interface cables which provide a conductive path into the circuitry or they may be directly coupled onto the printed circuit wiring when the assembly is not shielded. When the amplitude of the RF field is sufficient, induced voltages and demodulated carriers can disrupt the operation of a device.

Performing the radiated immunity test

This test is usually the longest and most difficult to perform, requiring very expensive capital equipment and considerable expertise. As with other immunity testing, pass/fail criteria must be defined by the manufacturer and a written test plan submitted to the test house. The EUT must be arranged for normal operation and in the most sensitive mode, while subjecting it to radiated fields.

Normal operation must be established within the test chamber while exposing it to the leveled disturbance field as the frequency is swept over the required frequency range of 80 MHz to 1 GHz. Some radiated immunity standards commence at a frequency of 27 MHz.

Severity levels

This standard normally requires immunity levels of 1 V/m, 3 V/m or 10 V/m however equipment specifications may have there own requirements at particular problem (interference) frequencies. It is in the manufacturers interest for the product to have an adequate level of immunity to radiated fields.

Uniform field requirements

The new generic immunity standard EN50082-1:1997 calls up IEC/EN61000-4-3 which requires the establishment of a uniform test field over the area occupied by the test sample. This is performed in an anechoic chamber lined with ferrite absorber tiles, which serve to dampen reflections and resonances so that a uniform test field can be established within the chamber. This overcomes the deficiencies of conventional unlined chambers where reflections and field gradients can cause sudden and often unrepeatable test failures. (The semi-anechoic chambers are also ideal for accurate in-door precompliance “non ambient” radiated emission measurements.)

Semi-anechoic chamber construction

The semi-anechoic chambers must accommodate the RF absorber on its walls and ceiling. The mechanical and RF design specifications must accommodate the very heavy ferrite tiles lining the chamber surfaces. The ferrite tiles are mounted on a dielectric material and affixed to the chamber surfaces. In unlined chambers, reflections from the metallic surfaces cause resonances and standing waves which can produce peaks and troughs in the intensity of the test field. Field gradients of up to 20 to 40 dB are common in unlined chambers and this can induce sudden failure modes for what may appear to be a very low field at the test sample. Chamber resonance results in poor test repeatability and a high probability of “over testing”. (This may result in the over design of the product.) These serious deficiencies are eliminated by the field homogeneity requirements of the new immunity standard IEC1000-4-3.

Hardware and software requirements for field generation

High power broadband RF amplifiers are used over the frequency range of 26 MHz to 2 GHz to drive broadband transmitting antennas at a distance of 3 metres from the device under test. Fully automated tests and calibrations are best performed under software control to allow greater flexibility in the testing and full control of all key parameters such as sweep rate, frequency dwell time, modulation and field intensity. Software hooks allow synchronized monitoring and stimulus of the EUT functionality. Interactive functions are desirable so that real time changes in both the EMC test software and the EUT parameters can be performed during the actual test. This user access feature allows rapid logging of all test data for efficient evaluation and analysis of the EUT EMC performance.

Pyramidal absorbers

The traditional pyramidal (cones) absorbers are effective, however, the large pyramid dimensions leave an unacceptably small usable space within the chamber. The length of the pyramidal absorber should be in the order of 100 cm for a lower frequency of 80 MHz, while lengths of over two meters are required for operation at the lower frequency of 26 MHz. Clearly, the usable space inside the chamber is severely reduced. The pyramidal absorbers also have the disadvantage that they are fragile, easily damaged by bumping and also highly flammable. The use of these absorbers on the floor of the chamber is also impractical. Field strengths of over 200 V/m sustained for extended periods of time result in a high risk of fire due to the heating of the pyramidal absorber.

Ferrite tile absorbers

Ferrite tiles are space efficient, however, they add a considerable weight to the chamber roof, walls and doors and consequently, the mechanical structure of the chamber becomes significant. They operate effectively at low frequencies however they become relatively in-effective at frequencies above 1 GHz. Ferrite tiles are very compact (100 mm by 100 mm by 6 mm thick) and withstand field strengths of over 1,000 V/m without the risk of fire hazards.

Difficulties in radiated immunity testing

There are inherent difficulties in performing radiated susceptibility tests since the support equipment used to operate the EUT, provide stimulus signals and to monitor its performance must itself be immune to the susceptibility fields. This can often present difficulties, particularly when the support equipment is complex and requires many cables and interfaces that must connect to the EUT via penetrations through the shielded test chamber. All cables penetrating the test chamber must be shielded and/or filtered in order for them to be immune to the radiated test fields and to prevent the degradation of the shielding performance of the test chamber. Compromising the shielding performance of the test chamber will result in the unintended radiation of the test fields into the environment and this may cause interference problems to spectrum users. RF filtering of data or signal lines is not always possible if there are high numbers involved or when high speed data links are used. RF shielding of the test equipment and interface cables can be difficult to achieve, even when using shielded interface cables since the EUT configuration does not always end itself to the maintenance of an effective RF shield.

Personnel safety concerns — non-ionizing radiation

Electromagnetic fields within the test chamber may exceed the recommended safety limits for exposure of personnel so an operator cannot be in the test chamber to monitor the status or performance of the EUT. One solution is to use a remotely controlled EMI hardened closed circuit TV system.

Immunity to Conducted RF Disturbances: IEC 1000-4-6

The purpose of this standard is to verify the EUT immunity against conducted RF disturbances in the frequency range 9 kHz to 230 MHz. The EUT is functioned and monitored in accordance with the prepared test plan while the RF is injected onto the leads. All cables of the EUT can act as receptors of radiated RF energy which can then appear on the cables as voltages up to 10 Vrms. This test can be difficult to perform as there are a multitude of different networks and coupling units required.

Immunity to Powerline Surge Transients: IEC 1000-4-5

The purpose of this test is to verify the EUT immunity to high energy surges caused by over-voltage from switching, lightning and other similar transients. Many equipment specifications, in particular ITE equipment, already require compliance with this standard. This test can cause damage to the EUT so it is best not to perform it unless the EUT has effective transient suppression in-built.

Immunity-Household Appliances, Tools and Similar Equipment: EN55104

The purpose of this standard is to verify that appliances and similar devices have an adequate level of immunity to electromagnetic disturbances. This is a product family standard for immunity. ESD, EFT, radiated immunity, conducted RF, surges, voltage dips and variations are covered.

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