Systematic PCB Verification Approach:

1. **Parts completion check:**
   1. All major components included?
      1. Microcontroller/FPGA/SoC/Microprocessor/CPLD?
      2. Power supply/regulation?
      3. Sensors?
      4. User interface elements? (LCDs, buttons, switches, etc.)
      5. Actuator drivers and control? (Motor control? LED constant current drivers? Audio filters and amplifiers? Etc. etc. etc.)
   2. All support components included?
      1. Microcontroller system guidelines or minimum connection requirements followed?
      2. Application circuits and/or app notes for all major components followed?
      3. Support components proper package as well as value? (Power circuit support components designed to handle provided voltages and currents?)
   3. Other components included?
      1. Programming header?
      2. Reset tact switch?
      3. Power connector(s)?
      4. Mounting holes?
      5. Power indicator(s)?
      6. Heartbeat LED?
      7. Oscillator/clocking circuitry?
      8. Debugging LEDs/interfaces?
2. **PCB Footprint Verification Check:**
   1. All parts fit on 1:1 scale printout of PCB layout?
3. **Parts placement check:**
   1. Crystal close to microcontroller?
   2. Decoupling caps close to/under microcontroller?
   3. Connectors on board edges?
   4. Parts grouped by system and/or in way that minimizes trace lengths?
4. **Mechanical/Space Conflicts check:**
   1. Has x- and y- footprint space around electrical pins and pads of all parts been accounted for?
   2. Has z- height of all parts been accounted for?
   3. Has clearance been provided for the bolt heads of all mounting holes?
   4. Have connectors been placed on the outer edges of the board where appropriate? Are they overhanging the edges of the board where appropriate? Are they oriented in the correct direction?
   5. Are traces clear of all mounting and mechanical support holes?
5. **Routing completion check:**
   1. All traces routed? (Ratsnest command reads "nothing to do"?)
   2. Oscillator traces clear of interfering signals?
   3. Traces of appropriate widths to handle current being passed? (Including power traces?)
   4. Traces entering pads at 90-degree angles (or 45 degree angles, where appropriate)?
6. **Routing minimization check:**
   1. Traces have been minimized where possible?
   2. Octagonal layout mode has been utilized where possible?
   3. Right angles have been removed, accept where necessary?

    4. Acute angles have been eliminated from routes in designs?

7. **Via minimization check:**
    1. Vias have been eliminated to the extent reasonable?

8. **Signal plane check:**
    1. Signal planes have been included, to the extent reasonable?
    2. Analog ground (AGND), has been separated from the main ground net in accordance with microcontroller datasheets? (Alternatively, AGND should be separated from GND by a 0Ω resistor)
    3. Isolation on all signal planes has been set to at least 12 mils?

9. **Silkscreen check:**
    1. Silkscreen labels have been provided for all component IDs and connector signal names?
    2. Silkscreen labels have been appropriately placed near components, but not on top of pads and pins?
    3. Pin 1 of all ICs and other polarity-sensitive components (such as diodes) is clearly marked?
    4. Board silkscreen layer includes names of all team members?
    5. Board silkscreen layer includes a descriptive name to identify the board?
    6. Board silkscreen layer includes a revision number and/or last modified date?