FVF Based OTA

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Team: Analog Vibes

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1. Problem Statement & Motivation

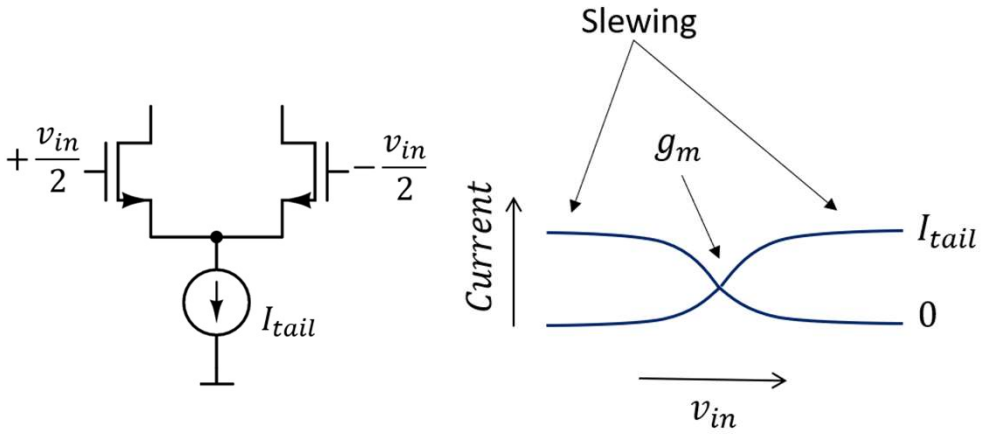
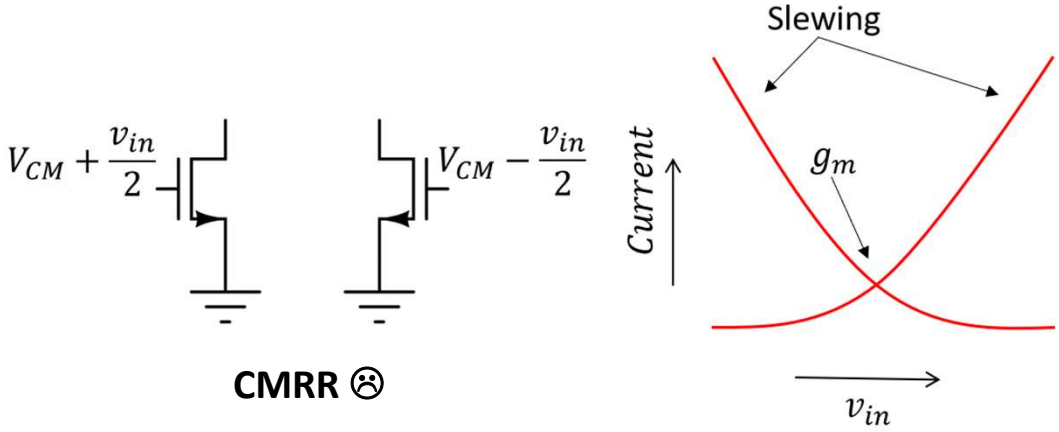


Figure 1: Slewing and Static Power Tradeoff



CMRR ☹

Figure 2: Breaking the Slewing and Static Power Tradeoff

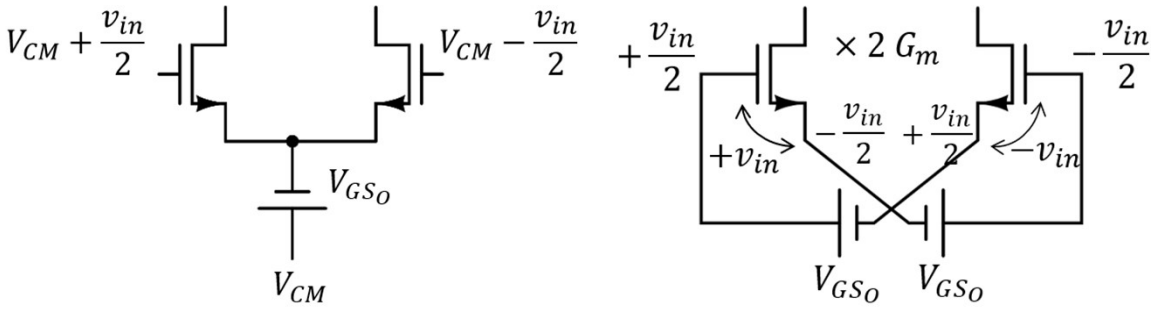


Figure 3: CMRR Reinstated ☺

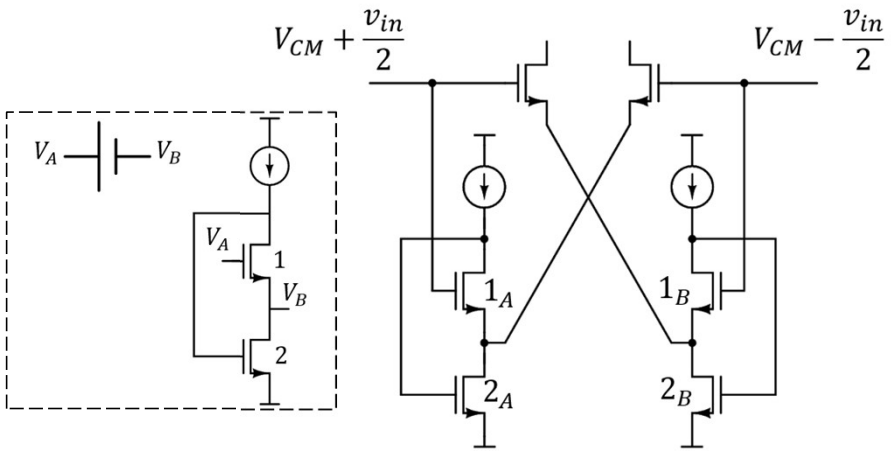
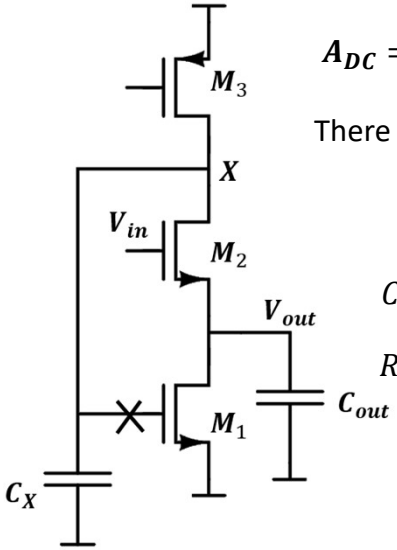


Figure 4: FVFs as Tail Voltage Source

2. FVF Based OTA: Overview & Sizing Constraints



$$A_{DC} = -g_{m1}R_X$$

There is also a RHP zero,

$$\omega_z = \frac{g_{m_1}}{C_{gd_1}}$$

$$C_{out} \approx C_L + C_{dd_1} + C_{ss_2}$$

$$R_{out} = r_{ds_1} || \frac{r_{ds_2} + r_{ds_3}}{1 + g_{m_2} r_{ds_2}} \approx \frac{\left(1 + \frac{r_{ds_3}}{r_{ds_2}}\right)}{g_{m_2}}$$

$$\omega_{p_{out}} = (R_{out} C_{out})^{-1}$$

$$C_X \approx C_{dd_3} + C_{dd_2} + C_{gs_1} + g_{m1} g_{ds_1} C_{gd_1} + C_p$$

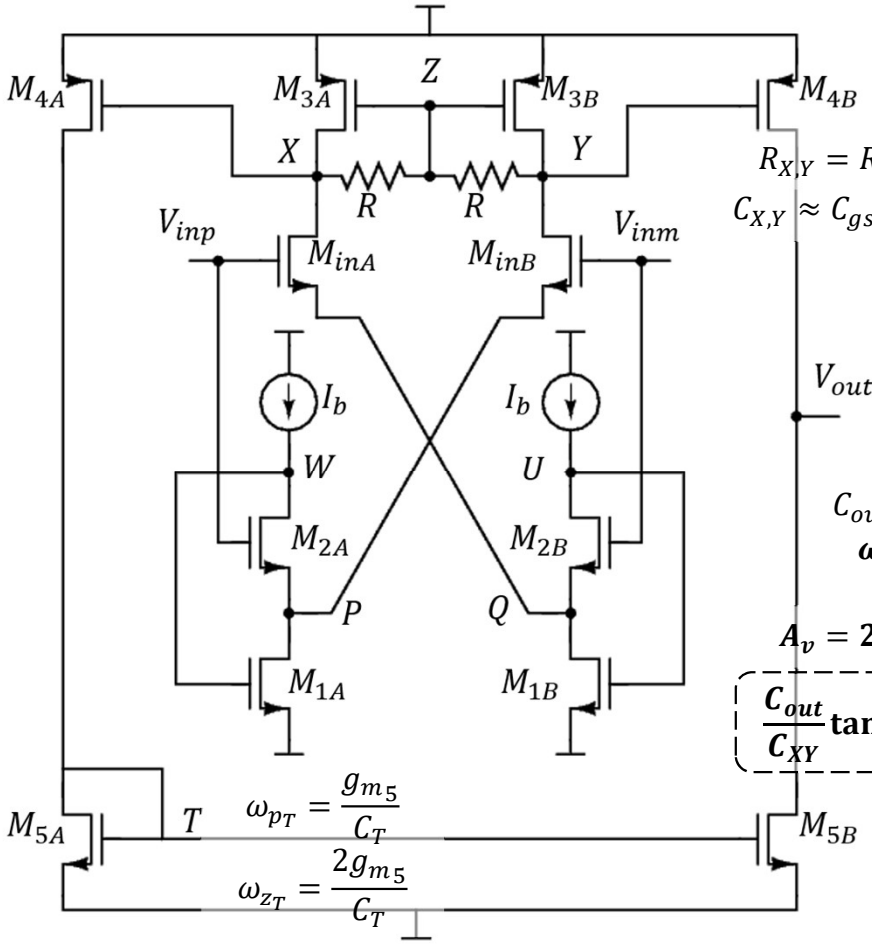
$$R_X = r_{ds_3} || (r_{ds_1} + r_{ds_2} + g_{m_2} r_{ds_2} r_{ds_1})$$

$$\omega_{p_x} = (R_X C_X)^{-1} \quad \text{(Dominant Pole)}$$

$$\Phi_M = 180 - \tan^{-1}\left(\frac{\omega_{ugf}}{\omega_{p_x}}\right) - \tan^{-1}\left(\frac{\omega_{ugf}}{\omega_{p_{out}}}\right) - \tan^{-1}\left(\frac{\omega_{ugf}}{\omega_z}\right)$$

90° 0°

$$\Rightarrow \frac{g_{m_1}}{g_{m_2}}\left(1 + \frac{r_{ds_3}}{r_{ds_2}}\right) = \frac{\tan(90 - \phi) \times C_X}{C_{out}}$$



$$R_{X,Y} = R \,||\, r_{ds_3} \,||\, r_{ds_{in}}$$

$$C_{X,Y} \approx C_{gs_4} + g_{m_4} r_{ds_4} C_{gd_4} + C_{dd_{in}}$$

$$\omega_{p_{XY}} = (R_{XY} C_{XY})^{-1}$$

$$\omega_{p_T} = \frac{g_{m_5}}{C_T}$$

$$\omega_{z_T} = \frac{2 g_{m_5}}{C_T}$$

V_{out}

$$R_{out} = r ds_4 || r_{ds_5}$$

$$C_{out} = C_L + C_{dd_4} + C_{dd_5}$$

$$\omega_{out} = (R_{out} C_{out})^{-1}$$

$$A_v = 2 g_{m_{in}} R_{XY} g_{m_4} R_{out}$$

$$\frac{C_{out}}{C_{XY}} \tan(90 - \Phi_M) = \frac{R_{XY}}{R_{out}}$$

3. Sizing Scripts using LUTs

Overview of Design Choices using Sizing Scripts

1. Choice of Optimal Gm/ID

(A good starting choice is @ max$\{\frac{g_m}{I_d} \times f_T\}$)

2. Choice of L for Gm/Gds for a given Gm/Id
3. Choice of Power Consumption
4. Stability Constraints
5. DC Biasing Constraints

Device Choices

1. PMOS: 1.8V LVT

(PMOS SVT was not chosen due to model inconsistencies)

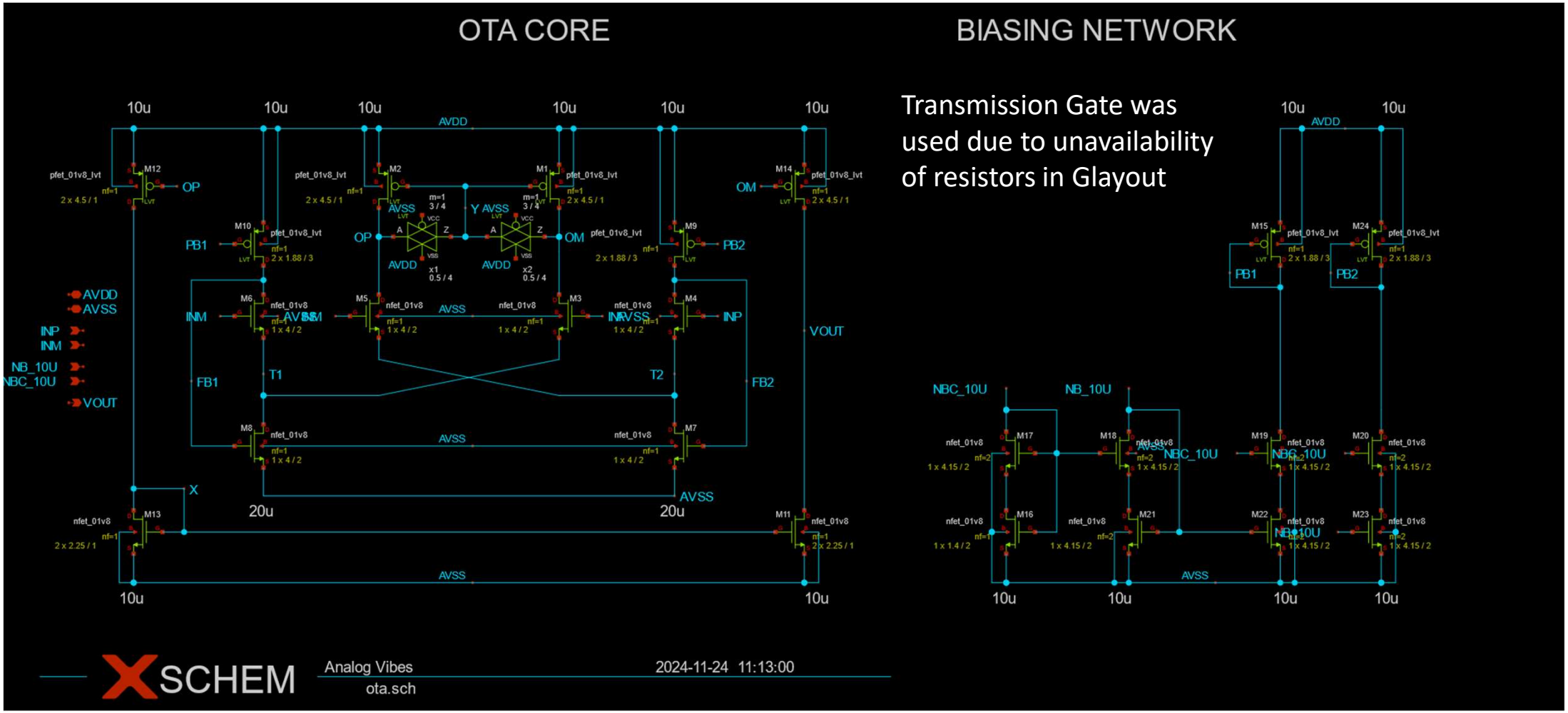
2. NMOS: 1.8V SVT

Blocks Sized Using Scripts

1. FVF
2. OTA
3. Low Voltage Current Mirror

(Few Transistors were oversized based on simulation results for Flicker Noise / Offset)

4. Schematic and Testbenches



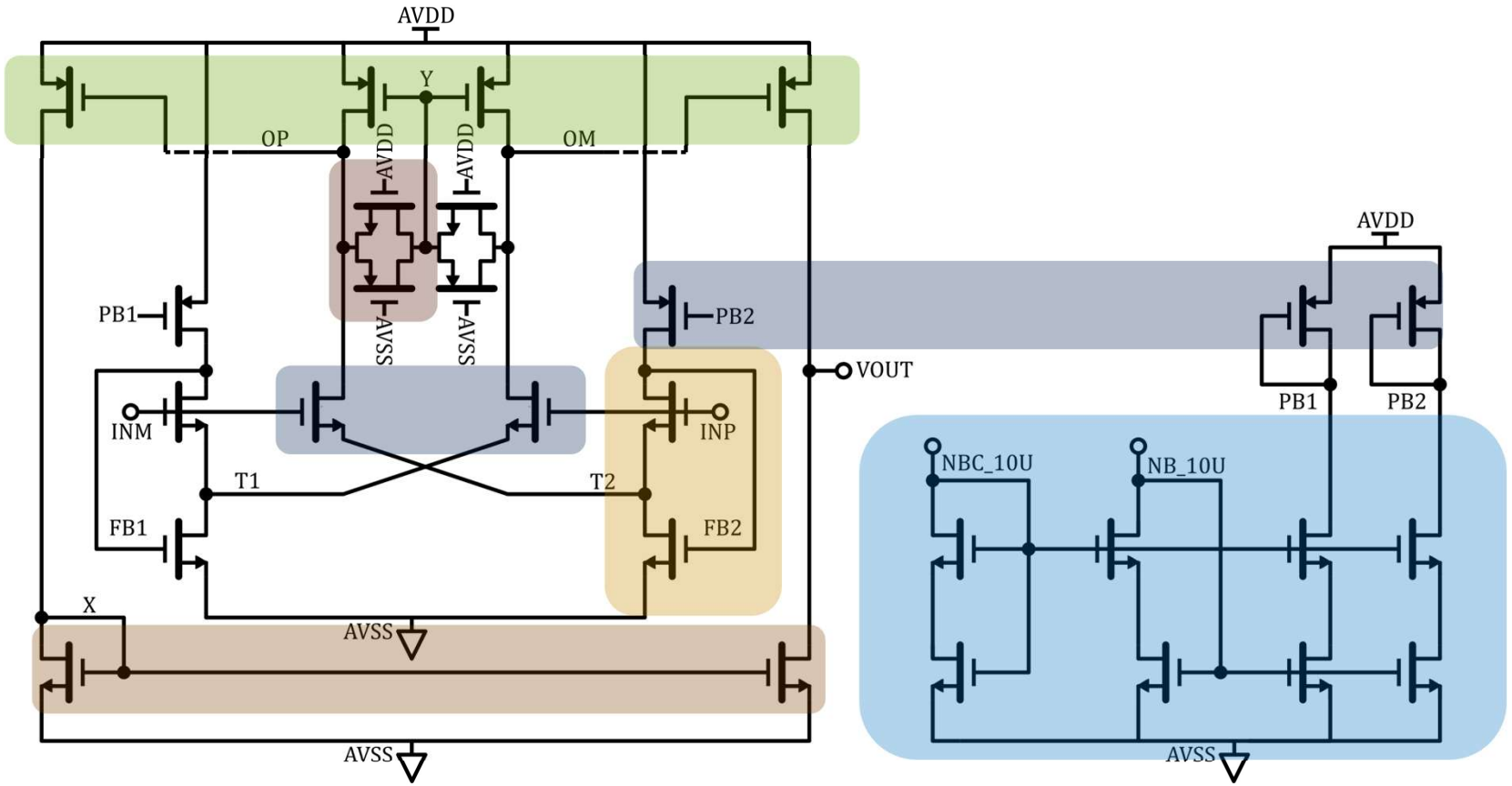
4. Schematic Testbenches and Simulation Results

Cross Corner PVT variations were automated using CACE
Load Cap used for OTA: $80pF$

Parameter	Tool	Result	Min Limit	Min Value	Typ Target	Typ Value	Max Limit	Max Value	Status
DC gain	ngspice	A0	any	40.062 dB	any	44.987 dB	any	52.226 dB	Pass ✅
Unity Gain Frequency	ngspice	UGF	any	417097.000 Hz	any	826089.000 Hz	any	2059780.000 Hz	Pass ✅
Phase Margin	ngspice	PM	any	86.774 °	any	89.349 °	any	90.115 °	Pass ✅
DC CMRR	ngspice	CMRR_DC	any	-84.205 dB	any	-55.444 dB	any	-41.906 dB	Pass ✅
DC PSRR	ngspice	PSRR_DC	any	-68.171 dB	any	-51.774 dB	any	-48.202 dB	Pass ✅
HD2 at 0.8V(p-p), 1kHz	ngspice	HD2	any	32.874 dB	any	47.843 dB	any	65.088 dB	Pass ✅
HD3 at 0.8V(p-p), 1kHz	ngspice	HD3	any	38.746 dB	any	53.906 dB	any	76.419 dB	Pass ✅
Noise:Vin(rms) (1kHz to 1MHz)	ngspice	vin_noi_rms	any	45.164 uVrms	any	57.088 uVrms	any	77.765 uVrms	Pass ✅
Rise Slew Rate	ngspice	rise_slew	any	3.273 V/us	any	4.498 V/us	any	7.482 V/us	Pass ✅
Fall Slew Rate	ngspice	fall_slew	any	2.147 V/us	any	3.240 V/us	any	5.228 V/us	Pass ✅
Total Static Power	ngspice	power_tot	any	169.306 uW	any	183.448 uW	any	198.997 uW	Pass ✅
Power - OTA Core	ngspice	power_ota_core	any	101.369 uW	any	111.447 uW	any	122.915 uW	Pass ✅
Power - OTA Bias	ngspice	power_ota_bias	any	67.924 uW	any	72.003 uW	any	76.082 uW	Pass ✅

Better Slew performance achieved ! (Compared to tail current source based)

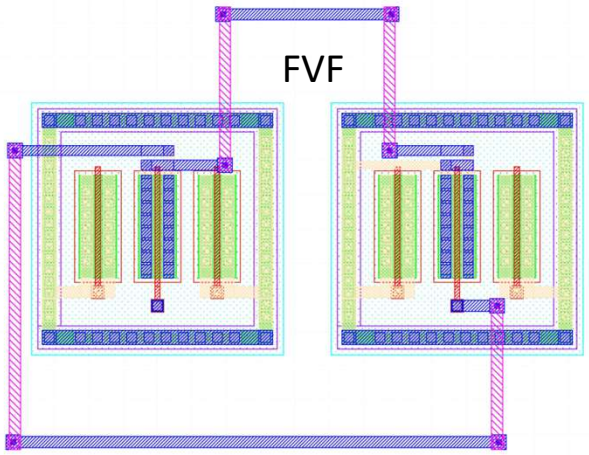
5. P-cell Breakup

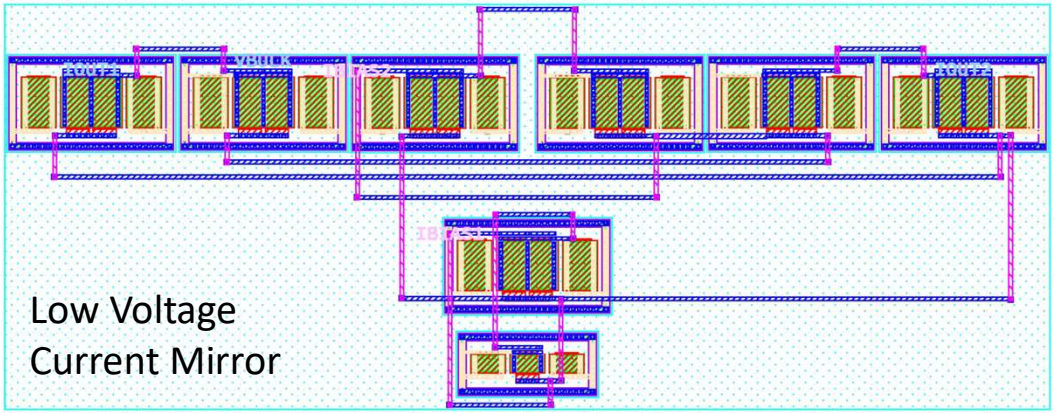


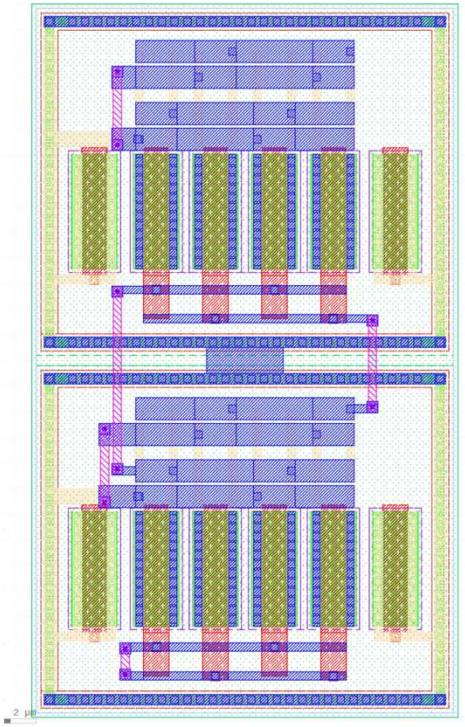
Pcell Breakup

1. FVF
2. Low Voltage Current Mirror
3. Input Pair
4. Current Mirror
5. Interdigitated fets

5. P-cell Breakup

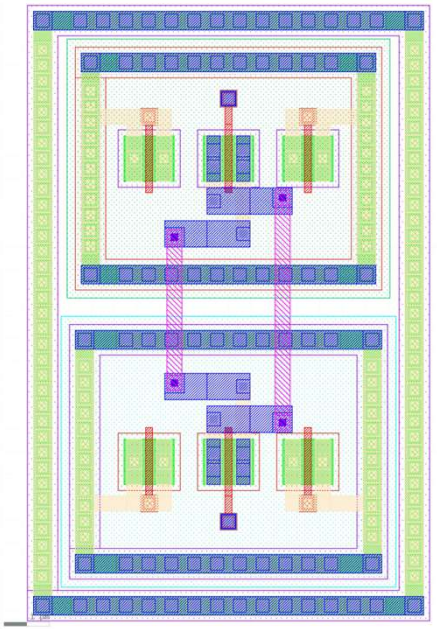




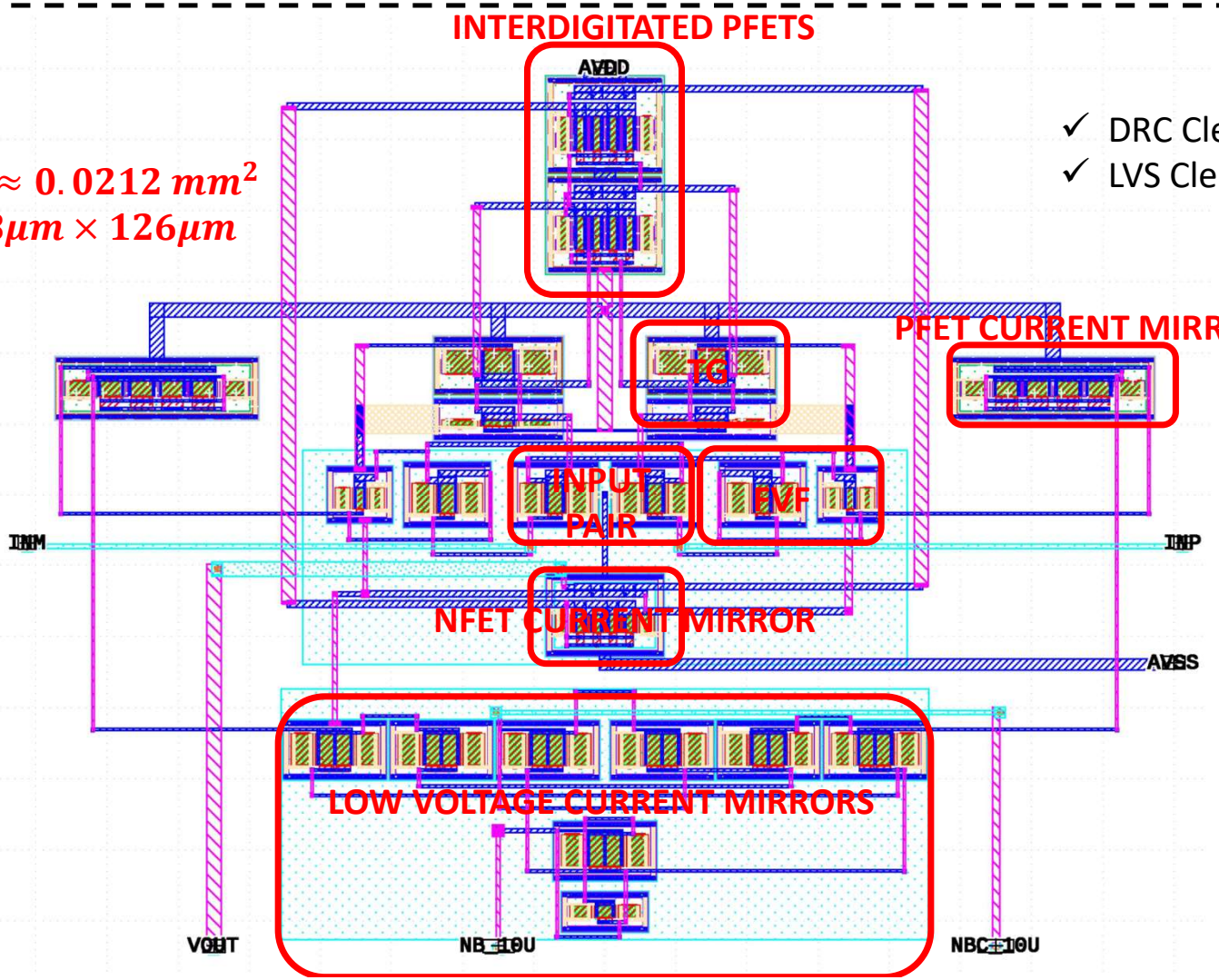


Interdigitated Pfets

Transmission Gate

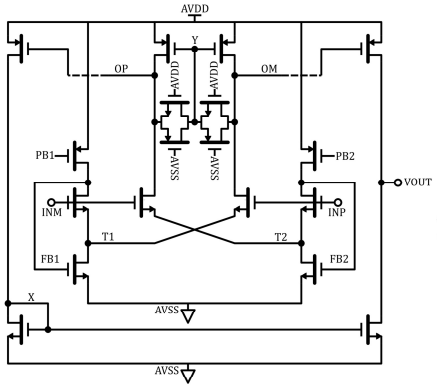


6. Placement & Routing: Final OTA

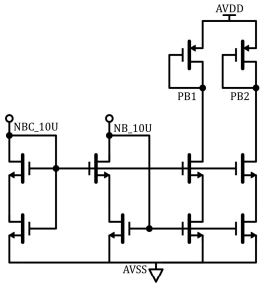


Area $\approx 0.0212\ mm^2$
$168\mu m \times 126\mu m$

- ✓ DRC Clean
- ✓ LVS Clean`



OTA CORE



BIASING NETWORK

7. Post Layout Simulation Results

PEX Performed Using Magic Terminal
Extracted Netlist used for cross corner simulations, automated with CACE

Parameter	Tool	Result	Min Limit	Min Value	Typ Target	Typ Value	Max Limit	Max Value	Status
DC gain	ngspice	A0	any	40.469 dB	any	46.984 dB	any	59.084 dB	Pass ✅
Unity Gain Frequency	ngspice	UGF	any	436845.000 Hz	any	1007410.000 Hz	any	4433840.000 Hz	Pass ✅
Phase Margin	ngspice	PM	any	76.171 °	any	88.659 °	any	90.022 °	Pass ✅
DC CMRR	ngspice	CMRR_DC	any	-75.288 dB	any	-54.392 dB	any	-40.354 dB	Pass ✅
DC PSRR	ngspice	PSRR_DC	any	-72.218 dB	any	-51.392 dB	any	-47.730 dB	Pass ✅
HD2 at 0.8V(p-p), 1kHz	ngspice	HD2	any	33.533 dB	any	49.020 dB	any	68.631 dB	Pass ✅
HD3 at 0.8V(p-p), 1kHz	ngspice	HD3	any	39.391 dB	any	55.518 dB	any	74.751 dB	Pass ✅
Noise:Vin(rms) (1kHz to 1MHz)	ngspice	vin_noi_rms	any	45.888 uVrms	any	56.984 uVrms	any	78.563 uVrms	Pass ✅
Rise Slew Rate	ngspice	rise_slew	any	3.494 V/us	any	5.030 V/us	any	8.066 V/us	Pass ✅
Fall Slew Rate	ngspice	fall_slew	any	2.195 V/us	any	3.368 V/us	any	5.424 V/us	Pass ✅
Total Static Power	ngspice	power_tot	any	169.622 uW	any	183.604 uW	any	198.993 uW	Pass ✅

Load Cap used for OTA: $80pF$
Better Slew performance achieved ! (Compared to tail current source based)

8. Conclusion & Comments

A FVF based OTA is successfully designed to achieve higher slew rate at lower Static Power consumption, without compromising with other parameters such as CMRR, PSRR, Linearity, Noise, etc.

Comments:

1. Issues faced while making generic p-cell
    i. C-route adds a single via (had to hardcode additional vias at few places)
    ii. DRC errors with certain parameters… need more time to make it generic
2. Issues while LVS and DRC using Glayout
    i. Works with Docker installation, but not with direct installation… (rpt files not found)
    ii. Gives the same error sometimes in docker environment as well…
3. Few of Extracted Results are better than schematic sims ?? (Can’t see extracted Resistor…)

8. Acknowledgement

Sincere thanks to Mehdi Saligane & Glayout Team, David Mitchell Bailey for much need technical support.
Grateful to Chipathon 2024 team for tutorials & lectures.

Open Source Tools/Frameworks Used:
Xschem, Ngspice, CACE, Glayout, Magic, Klayout, Pygmid, Netgen

9. References

1. R. G. Carvajal et al., "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52, no. 7, pp. 1276-1291, July 2005, doi: 10.1109/TCSI.2005.851387.
2. A. J. Lopez-Martin, S. Baswa, Jaime Ramirez-Angulo and R. G. Carvajal, "Low-Voltage Super class AB CMOS OTA cells with very high slew rate and power efficiency," in IEEE Journal of Solid-State Circuits, vol. 40, no. 5, pp. 1068-1077, May 2005, doi: 10.1109/JSSC.2005.845977.

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