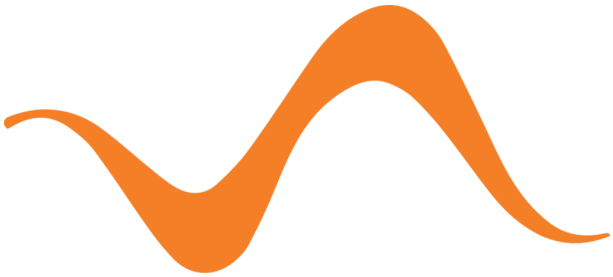

AC3E

Test Board 1.1.2
User Manual

Version 1.1.0

Overleaf

November 14, 2023

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1 Introduction

The Test Board Version 1.1.2 (Figure 1) is an evaluation board designed to test the integrated circuit for the Three Level Flying Capacitor Converter (3LFCC) project, version 1. The chip uses the Caravan Harness, and has the necessary outputs to test the converter, mapped to specific connectors and test points. This Test Board is designed to be used with the JoulesCope JS220 (with the front cover removed) to obtain the power measurements in the most accurate way possible.

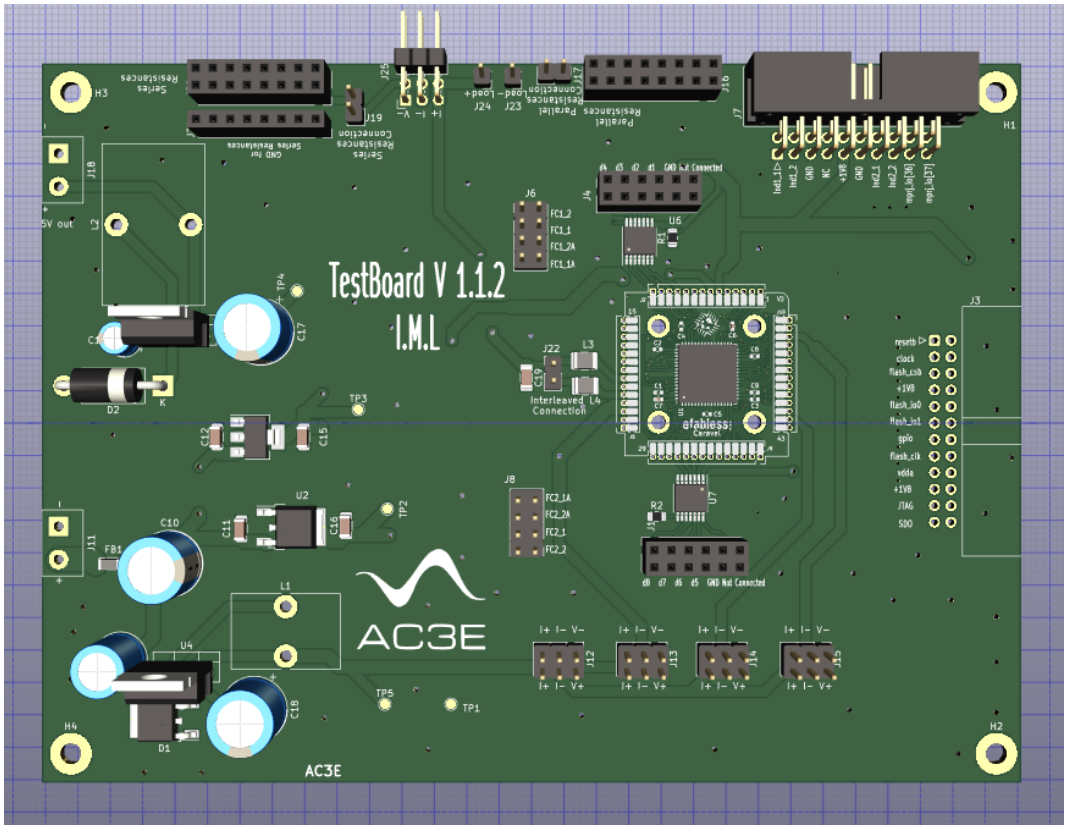

Figure 1: Test Board V 1.1.2

2 Observations

The version 1.1.2 of the board has some miss labeling and production errors (Figures 2 and 3) worth mentioning.

2.1 Miss labeling of ports and components

- Pins 11 and 12 of both J1 and J4 ports are labeled as not connected, in reality these pins correspond to an external 3V3 supply line for the level shifters that control the 3LFCC.

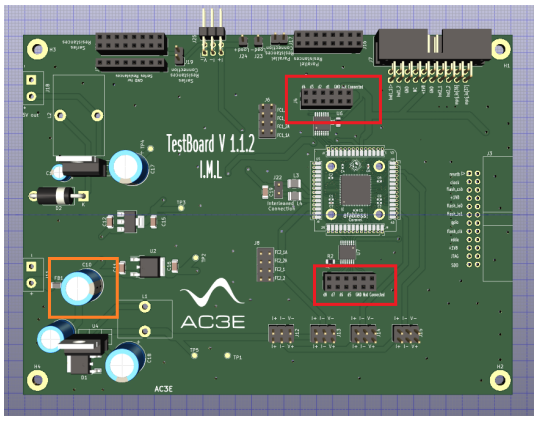

Figure 2: Ports J1 and J4 with miss labeled pins 11 and 12 (Red), C10 with additional plus sign (Orange).

- The capacitor C10 has two "plus" symbols for polarity. The convention of the others capacitors must be followed to ensure the correct polarity and good operation of the Test Board (just in case of replication of this board).

2.2 Production errors

- For the correct working of the two level shifters on the board, $1\mu F$ decoupling capacitors are needed between the supplies of the shifters (pins 1 and 14 of the shifters) and the ground plane. These capacitors footprints are absent from the PCB so additional work may be needed (manual scraping and soldering) to ensure the control signals integrity.
- The Test Board is designed to work with the Joulescope JS220. For this purpose 5 2x3 male header ports(J12, J13, J14, J15 and J25) are built in the PCB. Even though the ports are well labeled, if a direct connection is to be achieved between the Test Board and Joulescope, the headers need to be solder in the backside of the PCB.

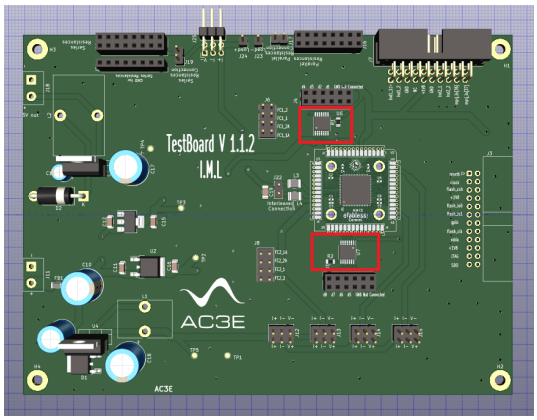

Figure 3: Level Shifters (Red) with missing $1\mu F$ decoupling capacitors.

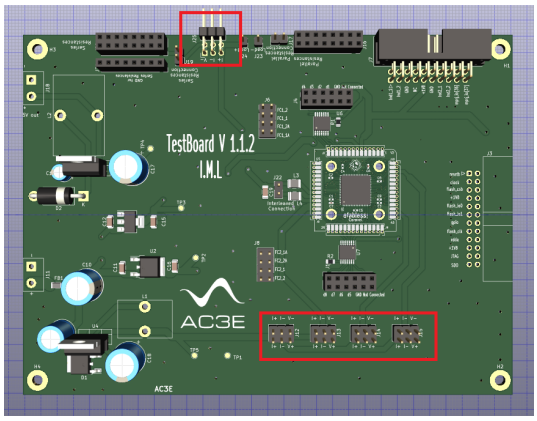

Figure 4: Ports (Red) that need to be mounted on the backside of the board for a direct connection with the Joulescope.

3 Power Supply

The Test Board 1.1.2 is designed to operate with a 9 V power supply in its input (Terminal Block J11) which has to be capable of an output of at least 6A (5A without the FPGA connected).

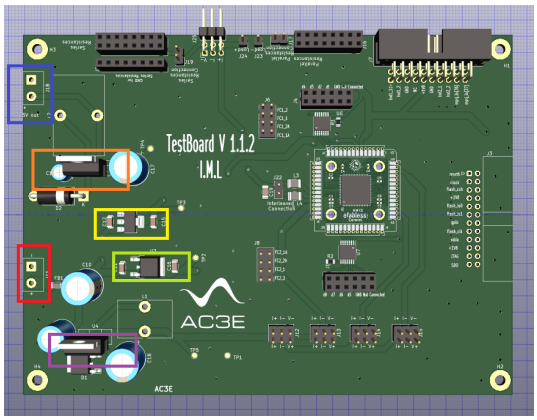

Figure 5: Test Board Power Supply input ports (Red), FPGA powering output (Blue) and converters for the 3LFCC Output (Purple), 5V logic (Green), 1.8V logic (Yellow) and FPGA powering (Orange).

In total, the Test Board has 4 different level converters to supply all the power needed to the components. It contains:

- 5V 1A converter routed to an output , designed to power an FPGA that is intended to control the 3LFCC.
- Two 5V converters to supply the logic and to power the 3LFCC.
- One 1.8 V converter to supply the low voltage logic for the IC.

4 Control Ports for the 3LFCC

For the control of the two 3LFCC branches, 8 PWM signals are needed, being D1-D4 (Port J4) and D5-D8 (Port J8) the ports for the task (Figure 6). These ports are meant to work with 3.3V PWM signals for the nmos and pmos transistors, then the signals are translated to 1.8V for the Caravan harness with the help of two level shifters (4 channels each).

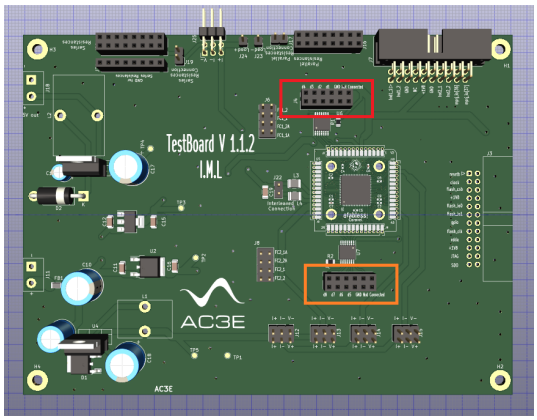

Figure 6: Ports for the control of the 3LFCC (D1-D4 Red, D5-D8 Orange).

5 Capacitors Voltage Measurement Ports

For the closed loop control of the 3LFCC branches, the voltage of the flying capacitors must be measured, for this J6 and J8 ports (Figure 7) are connected to the flying caps positive and negative points (differential measurement) through purely analog and also GPIO (configured as analog) outputs of the Caravan.

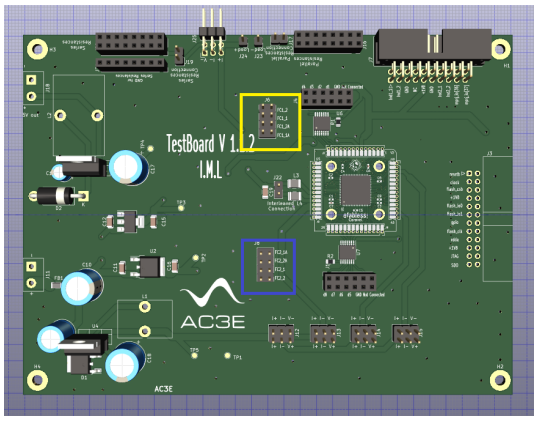

Figure 7: Ports for the control of the 3LFCC (Flying Cap 1 Yellow, Flying Cap 2 Blue).

6 Joulescope JS220

For the power measurements, four Joulescope ports for "in-between measurements" exist in the board. One port for the consumption of all the power

electronics of the converter (VHO, VLS1, VLS2), one for each of them alone. Additionally a fifth connector for the output.

If no Joulescope is used in any of the in between measurements ports (J12, J13, 14 or J15), the I+ and I- pins of that port need to be shorted .

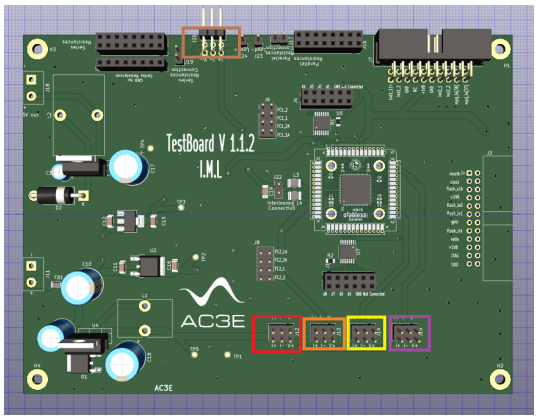

Figure 8: Ports for the JouleScope connection to measure the consumption of: VHO(Orange), VLS2(Yellow), VLS1(Purple), or oll of them (Red), and the load (Brown).

7 Interleaved Mode

The 3LFCC has two identical branches that can be used independently or in an interleaved configuration. For the latest one, the pins of the J22 port (Figure 9) need to be shorted (just one branch of the 3LFCC (Output 1) is routed to the Load connectors).

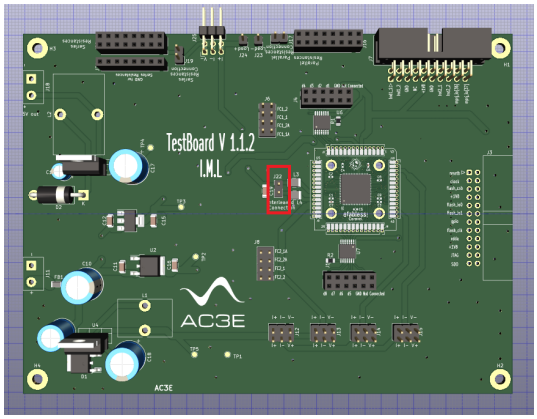

Figure 9: Port for the interleaved mode (Red).

8 Load Connections

The Test Board 1.1.2 has multiple configurations for Load connections. The main two types of connections is with or without the Joulescope connected for current and power measure in the load.

8.1 No Joulescope connected

With No Joulescope connected, there are different types of connection to be made:

8.1.1 External load

The pin headers J24 Load+ and J23 Load- are intended to be use for the connection of an external load.

8.1.2 Series On Board load

The pin sockets of port J20 are intended for a series resistances connection of typical breadboard resistances. The following image shows the internal routing of the connectors.

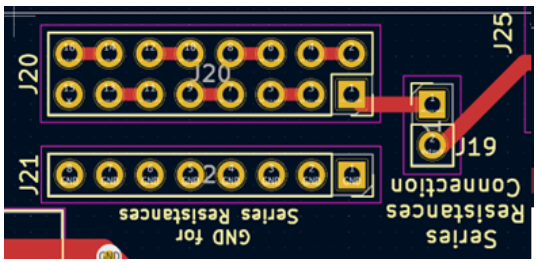

Figure 10: Routing of the J20 port for series resistances

It's important to short circuit the I+ and I- connections of port J29, since the joulescope its not present to complete the circuit, as well as the connections of J19 port.

The Resistances must be connected with one end in each of the two long rows of the 2x8 port in order to work as a "series resistances matrix". For the last resistance in the connection the end that wont have another resistance connected should be connected to gorund in the J21 port to complete the circuit.

8.1.3 Parallel On Board load

The pin sockets of port J16 are intended for a parallel resistances connection of typical breadboard resistances. The following image shows the internal routing of the connectors.

Figure 11: Routing of the J16 port for parallel resistances

It's important to connect the Load+ header with the J17 header that is more close to the j16 port in order to connect the parallel matrix to the output of the 3LFCC. In this case is easier to figure how the matrix works. One row is connected to the output and one to ground so it does not matter where the resistances are connected as long as they complete the circuit.

8.2 Joulescope connected

8.2.1 External load

If the Joluescope needs to be used with an external load, the positive side of the load needs to be connected to pin 1 of J19 port while the negative end is connected to Load-(gnd).

8.2.2 Series On Board load

For the series connection with onboard loads, pins 1 and 2 of port j19 need to be shorted and the J20 port be used as descripted above.

8.2.3 Parallel On Board load

For the parallel connection with Joulescope, pin 1 of J19 port needs to be connected to pin 1 of J17 port and the J16 port be used as descripted above.

9 Control of the Test Board with an FPGA

The 3LFCC is designed to work with PWM modulation, for this, J4 and J1 ports have dedicated pins meant to be connected to output pins of an FPGA to control the pulses.

9.1 FPGA Connection

To use an already setup file (Bitstream), it is necessary to program the FPGA, with the corresponding software.

In the case of the Test Board V1.1.2, the chosen FPGA is the Nexys 7, and the Vivado software is needed to program it.

9.1.1 Already setup Bitstream (Plug and play)

To upload a Bitstream to the FPGA is necesary to create a new project and set it up for the xc7a100tcsg324-1 (this model is used for the nexys 7 FPGA, other models may need another configuration). No source file needs to be created.

Once in the project, the FPGA needs to be connected through the usb port. Next open the Hardware Manager, at the bottom left, and program device. Look for the Bitstream and upload it.

After the bitstream is uploaded DONT DISCONNECT THE FPGA from the power source.

The provided test program lets the user change the duty cycle (80 different levels) and dead times in base clock cycles (base clock of 800MHz), with a PWM frequency of 1MHz, mapping the signals to [2:1] pins in the JD and JC ports of the FPGA.

The PWM duty cycle is control by the first 7 switches (SW[6:0]) of the FPGA in binary code. The dead times are also controlled by the switches in binary (SW[10:7]).

9.1.2 Advanced testing

A I/O of the Test Board

Most, but not all, of the Caravan pins are mapped out to connectors in the board. There are also 5 connections for the use of the Joulescope JS220 and 2 types of matrices to connect resistances directly for onboard testing. The description of each port and pin are detailed in Tables 1 and 2.

Port	pin	Detail	Port	pin	Detail
J1	1,2	D8	J7	1,2	$Ind1_1$
	3,4	D7		3,4	$Ind1_2$
	5,6	D6		5,6	GND
	7,8	D5		7,8	NC
	9,1	GND		9,1	1V8
	11,12	3V3(meant to be powered by FPGA)		11,12	GND
				13,14	$Ind2_1$
J3	1,2	Reset		15,16	$Ind2_2$
	3,4	clock		17,18	$mprj_io[36]$
	5,6	$flash_csb$		10,2	$mprj_io[37]$
	7,8	1V8	J8	1	$FC2_1A$
	9,1	$flash_io0$		3	$FC2_2A$
				5	$FC2_1$
	11,12	$flash_io1$		7	$FC2_2$
	13,14	gpio		2,4,6,8	GND
	15,16	$flash_clk$	J11	1	9V input -
	17,18	vdda		2	9V input+
	10,2	1V8	J12		Joulescope VHO, VLS1, VLS2
	21,22	JTAG			
	23,24	SDO	J13		Joulescope VH0
					(3LFCC Power)
J4	1,2	D4			
	3,4	D3	J14		Joulescope VLS2
	5,6	D2			(3LFCC Level Shifter 2)
	7,8	D1			
	9,1	GND	J15		Joulescope VLS1
	11,12	3V3(meant to be powered by FPGA)			(3LFCC Level Shifter 1)
J6	2	$FC1_2$	J16		Onboard parallel resistances connection
	4	$FC1_1$			
	6	$FC1_2A$	J17		Onboard parallel resistances connection
	8	$FC1_1A$			
	1,3,5,7	GND	J18	1	5V output -
				2	5V output +

Table 1: I/O of the Test Board (Ports J1-J18)

Port	pin	Detail
J19		Onboard series resistances connection
J20		Onboard series resistances connection
J21		Onboard series resistances connection
J22	1	3LFCC output 1
	2	3LFCC output 2
J23		Load-(GND)
J24		Load+(3LFCC Output1)
J25		Joulescope (Load Measurement)

Table 2: I/O of the Test Board (Ports J19-J25)

B FPGA specifications

The Nexys 7 complete spec list can be found here.

The principal reason for the use of these model is the clock wizard ip and the PLL capabilities of the FPGA. The core concept of the 3LFCC demands the use of ultra high frequency PWM control, nowadays comercial high frequency PWM means a 2MHz control at best. With the use of the PLL plus the clock wizard allows the generation of a 800MHz base clock, wich is used to generate a digital PWM with 80 levels of Duty Cycle at 10 MHz of frequency.