The files present in [these](https://drive.google.com/drive/folders/13AKop2yQgPxuOZjezuhXVDJ7BkxZb8ba?usp=drive_link) folder correspond to the necessary files for the testing the 3LFCC through the output ports of the FPGA. The Bitstream is able to produce a 10MHz (adjusted to 1MHz by code) PWM signal to control the 3LFCC Chip through the PMOD pins.

Dead times are built into the program and accessible through the switches[10:7] on the FPGA.

The Duty Cycle is also accessible through the switches[6:0] on the FPGA. (max value in decimals is 79, in binary 0100 1111).

The code has two protection systems. Firstly if the input makes the Duty Cycle less than 0 or bigger than the period, the Duty Cycle is set to 100%. Secondly if the Dead times are set to be less than 1 or bigger than the period, they are set to 6 clock pulses (0110).

PMOD connection:

For the working of one branch of the two 3LFCCs the pins JC[2:1] and JD[2:1] are meant to output the control signals:

JD[1] = PMOS D1

JD[2]= NMOS D4

JC[1]= PMOS D2

JC[2]= NMOS D3