The files present in [these](https://drive.google.com/drive/folders/1WXOPbPir3Bz6BNUKljxI3BF03IS7iPCq?usp=drive_link) folder correspond to the necessary files(just the LFCC\_Test.bit to work, the folder is the complete project) for testing of the 3LFCC through the output ports of the FPGA. The Bitstream is able to produce a 10MHz PWM signal to control the 3LFCC Chip through the PMOD pins.

Dead times are built into the program and are set to 7 clock cycles. The Duty Cycle is accessible through the switches[2:0] on the FPGA (One Hot configuration 001 = 25%, 010=50%, 100=75%). There is also a delta variable that makes the PWM asymmetric between pwmout1 and pwmout2. Delta is accessible also through the switches[5:3].

The default Duty Cycle is 50%.

PMOD connection:

For the working of one branch of the two 3LFCCs the pins JC[2:1] and JD[2:1] are meant to output the control signals:

JD[1] = PMOS D1

JD[2]= NMOS D4

JC[1]= PMOS D2

JC[2]= NMOS D3