Microelectronic Systems

Labs and Projects Rules

March 2, 2022

General Rules

G.1 Only groups with three people are allowed.

G.2 You are from a previous year, you have made all the labs and you want to join a new group to improve your evaluation. You can, but keep in mind that *you loose all the evaluations* from the previous year and you have to re-submit all the labs.

G.3 Lab grading scale is from A to D, where A is the highest mark and D is the lowest.

G.4 Late submissions are evaluated as D. For more detail, please read the next section.

G.5 Cheating situation on lab submissions will be evaluated as D.

G.6 Please comment on the VHDL code in both labs and DLXs, it will be part of the overall evaluation.

G.7 There will be **four** DLX discussions per academic year: end of June, end of July, end of September, end of October.

G.8 The DLX discussion is one-time. Once you are ready for the discussion you can book a time slot on the doodle that will be provided on the *Portale della Didattica*. Cheating and plagiarism on DLX projects lead to a null grade.

Lab Submission Rules

To be evaluated you must upload a zip file through the student web page, *Elaborati* section. This file must respect **STRICTLY** the following rules. Non-organized folder and submission after the deadline **WON'T be accepted and evaluated**.

L.1 The root folder (containing all the sub-directories) should be zipped. So, the file must have the extension ".zip".

L.2 The name of the zipped folder must be:

- `grXX_labYY.zip`, where `XX` represents your group number, `YY` represents the lab number. Both of them must have two digits. Example, if you are group 2 and you are submitting the lab 5 the file name must be → `gr02_lab05.zip`).

L.3 The root folder must have the same name of the archive (`grXX_labYY`) and inside create one sub-folder for each exercise.
Example of folder hierarchy within the .zip file:

```
grXX_labYY.zip
├── ex1.1.1
│   └── sim
│       ├── all necessary VHDL files to simulate the design
│       └── waveforms (if required in the lab instructions)
├── ex1.2.1
│   └── sim
│       ├── all necessary VHDL files to simulate the design
│       └── waveforms (if required in the lab instructions)
├── ex2.1.1
│   └── syn
│       ├── all necessary VHDL files to synthesize your design
│       ├── all reports (see lab instructions)
│       ├── post-synthesis netlist (if required in the lab instructions)
│       └── synthesis scripts
└── etc...
```

L.4 Remember to put all the component files and the test-benches needed to simulate the architecture or run the synthesis.

L.5 In each exercise folder put only the **NECESSARY** files. (e.g.: `gr01_lab01/ex1.1/sim` will contain only the VHDL files related to `ex1,1`, and nothing more). Please remember to delete all the `WORK` folders generated by the tools and all useless files.

L.6 When the **VHDL netlist** is required, you must submit all the VHDL files of your design (testbench included) necessary to simulate your design.

L.7 When the **waveforms** are required, you must submit the simulation waveforms printed on a pdf file (use the File→Print postscript in Modelsim and select the time window you are interested in). The printed waveforms must be readable.

L.8 When the **synthesis script** is required, it means that you should provide the script with all the commands required to synthesize your architecture and reproduce your results.

L.9 When the **post-synthesis** netlist is required, you must submit the VHDL netlist after synthesis generated by the Synopsys.

L.10 If you need to give us some extra information, just add a "`readme.txt`" file into the root folder.

L.11 If some specific report is requested (power, timing etc.) add a "`report`" folder containing all the outputs of your synthesis.

DLX Discussion Rules

D.1 **Plan your time** in order to be able to conclude in one of the **four** sessions (see **G.7**). The DLX is optional, therefore is up to you to organize your work. No exceptions will be made.

D.2 Remember to book a time slot on the doodle that will be published on the *Portale della Didattica* just before the sessions (see **G.7**).

D.3 Remember to submit (on the web-portal) the report and all files (`VHDL, scripts, reports...`), 1 week before the discussion. The deadline will be published on the web-portal.

D.4 Bring your own laptop with you.

D.5 Be ready to demonstrate the logic correctness of your architecture. You will be asked to run simulations.

D.6 The files of the project you present during the oral exam must correspond to uploaded ones.

D.7 Each member of the group will discuss the project together, however, each evaluation will be managed individually.