AJAY KUMAR GARG ENGINEERING COLLEGE, GHAZIABAD

Department of CSE

Pre-University Test

Course: B. Tech.
Session: 2025-26

Semester: III
Section: CSE1,2,3 CS1,2,3 IT1,2,3 CSIT1,2 CSE-DS, AIML. CSE-AIML1,2

Subject: Comp. Org. Arch.
Max Marks: 70
Sub. Code: BCS-302
Time: 3 hrs.

OBE Remarks:

Q.No.	1	2	3	4	5	6	7	8	92	10	11	12	13	14	15	16	17
CO No.	1	1	3	3	3	4	5	1	2	5	4	3	3	4	4	5	5
Bloom's Level	4	2	2	4	4	2	4	3	3	3	4	2	3	4	2	3	4
Weightage CO3: 16					Weightage CO4: 16										Weightage CO5: 16		

Note: Answer **all** the sections.

Section-A

A. Attempt **all** the parts. **(7 X 2 =14)**

1. Distinguish between computer architecture and organization through an example illustrating computer system design.
2. Identify different types of addressing modes and state their significance in instruction design.
3. Summarize the main cycles of a CPU and their coordination during instruction execution.
4. Examine the key features that differentiate RISC and CISC processors.
5. Analyze the structural and functional differences between 2D and 2.5D memory organization.
6. Describe the role of cache memory in reducing memory latency in modern processors.
7. Compare memory-mapped I/O and isolated I/O with respect to addressing mechanism and control signal requirements.

Section-B

B. Attempt **Any three. (Q. No. 12 is Compulsory)** **(3X 7=21)**

8. Illustrate the mechanism of data transfer among registers, buses, and memory units within a digital system.
9. Using Booth's algorithm, perform multiplication of (–9) × (+6) and trace the contents of all registers after each step.
10. Demonstrate the sequence of signals in destination-initiated handshaking and explain timing overlap.
11. Evaluate the role of Translation Lookaside Buffer (TLB) in virtual memory systems and analyze its impact on effective memory access time.

12. Construct a hardwired control unit and compare it with a microprogrammed control unit.

Section-C

C. Attempt **all** the parts. **(5 X 7 = 35)**

13. Attempt any one.

a) Design a pipeline structure for a 4-stage instruction execution and analyze the Speedup.

b) Explain how an interrupt cycle assists a microprogram in managing subroutine call and return sequences.

14. Attempt any one.

a) Analyze the steps involved in virtual memory address translation using paging

b) Compare FIFO and LRU page replacement algorithms for the reference string: 1,2,3,4,1,2,5,1,2,3,4,5.

15. Attempt any one.

a) Design the address structure for a 2-way set-associative cache mapping between 128 KB main memory and 4 KB cache with 256-byte blocks.

b) Evaluate the role of auxiliary memory in the memory hierarchy with examples.

16. Attempt any one.

a) Explain a DMA-based data transfer scheme and illustrate what is cycle stealing.

b) Examine the sequence of operations in interrupt-driven I/O transfer and discuss its advantages over programmed I/O.

17. Attempt any one.

a) Design a bus system incorporating a priority interrupt mechanism using daisy chaining and parallel priority methods.

b) Analyze the role of strobe control and handshaking in asynchronous data transfer.

Faculty Sign **HoD Sign**