Roll No. | | | | | | | | | | | | |

AKGEC/IQAC/QP/09

AJAY KUMAR GARG ENGINEERING COLLEGE, GHAZIABAD
DEPARTMENT OF INFORMATION TECHNOLOGY
Sessional Test

Program: B.Tech
Session: 2025-26
Semester: 3rd
Section: CSE-1,2,3,CS-1,2,CSE- AIML-1,2,CSE-DS,AIML,IT-1,2,3CSIT-1,2
Subject: COMPUTER ORGANISATION & ARCHITECTURE
Subject Code: BCS-302
Max. Marks: 50
Time: 2 Hours

OBE Remarks:

Q.No	1	2	3	4	5	6	7	8	9	10	11	12
CO No.	CO1	CO1	CO2	CO2	CO3	CO1	CO1	CO2	CO2	CO3	CO1	CO2
Bloom's Level* (L1 to L6)	3	2	3	3	1	2	3	2	3	3	3	3
Weightage CO1: 21.5			**Weightage CO2: 21.5**								**Weightage CO3: 7**	

**Bloom's Level: L1: Remember, L2: Understand, L3: Apply, L4: Analyze, L5: Evaluate, L6: Create*

Note: Answer **all** the sections with all the questions

Section-A (2*5=10)

1. Draw the diagram of the basic functional units of computer.
2. Explain different types of Buses.
3. Design a 4-bit Parallel adder.
4. Design 3*2 array multiplier using parallel adder.
5. List various micro-operations.

Section-B (5*5=25)

6. Define the term BUS arbitration? Why is it needed? How can bus arbitration be implemented in Centralized Scheme?
7. A 2 word instruction at address 400 and 401 is a load to accumulator. This instruction within address field 300, PC has the value 400 for fetching this instruction, the content of register R1 is 200 and index register is 100.Find out the Effective addresses of Direct mode, Indirect mode, Register direct, Register Indirect, Index mode and relative mode.
8. Discuss the motivation behind CLA. Design 4-bit Carry Look-ahead Adder.
9. Represent the number $(-253.125)_{10}$ in IEEE FPN in single and Double precision format.
10. Evaluate the expression **X= A-B+C*D /E+F*G** Using one and zero address Instruction format.

Section-C (7.5*2=15)

11. A digital computer has a common bus system for **5 registers of 6 bits each**. If the bus is constructed with multiplexers, draw a schematic diagram, and find following.
    - i. How many selection inputs are there in each multiplexer?
    - ii. What sizes of multiplexers are needed?
    - iii. How many multiplexers are there in the bus?

12. Draw the flowchart of Booth Algorithm. Show the systemic multiplication process of **(-14) X (-12)** using Booth's algorithm.

Faculty Sign **HOD Sign**