Homework 3

Computer Architecture: Fall 2012

Problem 1

a) **[10 points]** Briefly describe fine-grained and coarse-grained multithreading techniques and their advantages and disadvantages? Which one can be used for simultaneous multithreading?

b) **[10 points]** What are the design challenges of achieving simultaneous multithreading?

c) **[10 points]** Consider a simple MIPS-like processor running at 2 GHz with a CPI of 1.9. It has an L1 and a L2 cache system, where miss rates are 4% and 10% respectively. If the miss penalty for L1 and L2 are 5 ns and 50 ns respectively, find the performance of the processor in millions-of-instruction-per-second.

Problem 2 [20 points]

Assume a sequence of memory requests where the block addresses are: A, B, C, A, B, C, A, B, C, A, B, C. Assume that there are only 2 blocks in cache i.e., cache can hold only two of these blocks at a time.

a) Simulate LRU replacement policy for the above sequence.

	A	B	C	A	B	C	A	B	C	A	B	C
Block 1												
Block 2												

b) Simulate the optimal (OPT) replacement policy for the above sequence. Is it possible to implement OPT? If yes, discuss its implementation; otherwise design and simulate any implementable replacement policy that can provide better performance than the LRU replacement trace in a).

	A	B	C	A	B	C	A	B	C	A	B	C
Block 1												
Block 2												

Problem 3

a) **[10 points]** We need to design a 16 KB cache with block size (line size) of 4 words, and word size 2 bytes. Determine the tag array size for three cache implementations (direct-mapped, 4-way set associative and fully associative) on a computer that has 32–bit physical address and the cache is addressed by physical address.

b) **[10 points]** You have a processor with an ideal CPI without memory stalls for each instruction type as follows: ALU=1, Load/Store=1.5, Branch=2, Jump=1. Consider an application, which has an instruction mix of 50% ALU and logical operations, 25% load and store, 15% branch and 10% jump instructions. Assume a 4-way set associative 1-level separate data and instruction cache with a miss rate of 10% (0.10) for data accesses and miss rate of 5%

(0.05) for instructions, and a miss penalty of 20 cycles for both instruction and data caches (assume a cache hit takes 1 cycle). What is the effective CPU time (or effective CPI with memory stalls) and the average memory access time for this application with this cache organization? Please refer to Appendix B where a number of cache performance equations are discussed.

Problem 4 [30 points]

Cache access involves address translation, cache tag comparison, and cache data array access. Assume in particular processor architecture, the virtual and physical addresses have 48 and 40 bits respectively. The page size is 8 KB and the cache block size is 64 bytes. Assume that the TLB can record the recent 2K virtual to physical page address translation implemented with 4-way set-associative design. The L1 cache size is 32KB with 8-way set associative design. You need to fill the number of bits inside the brackets "( )" in the diagram below. Note that the "Total size" in the diagram represents the total size of the entire tag or data array.