Homework 1

You are not allowed to take or give help in completing this assignment.

1. Assume that you are the product manager for XXX processor. The chip has an area of 263 mm2, with a defect rate of 0.025 defects per cm2 and N=11.5. The die of each chip is occupied by four identical cores (70% total area) and a shared L3 cache (30% total area). For simplicity, we assumed here that each chip has only four cores and an L3 cache (no other components).

该芯片面积为263 mm2，缺陷率为0.025/cm2，N=11.5。每个芯片的裸片由四个相同的内核（总面积的 70%）和一个共享的 L3 缓存（总面积的 30%）占据。为简单起见，我们在这里假设每个芯片只有四个内核和一个 L3 缓存（没有其他组件）。

* 1. **[5 Point]** What is the yield of the die?

晶片的成本？

* 1. **[5 Point]** Some researchers proposed that the number of defects in a die can be modeled by [Geometric distribution](http://en.wikipedia.org/wiki/Geometric_distribution). Suppose we can use the yield as the probability that there is no defect on a die, what is the value of parameter *p* in Geometric distribution here?

一些研究人员提出，可以通过几何分布来模拟模具中的缺陷数量。 假设我们可以使用良率作为裸片上没有缺陷的概率，那么几何分布中参数 p 的值是多少？

**Note:** Geometric distribution means the probability that there are exactly *k* defects (*k* being a non-negative [integer](file:///C:\wiki\Integer), k = 0, 1, 2, ...) is equal to

几何分布意味着恰好有 k 个缺陷（k 是非负整数，k = 0, 1, 2, ...）的概率等于



where,

k is the number of occurrences of defects

*p* is a positive [real number](file:///C:\wiki\Real_number),

在哪里，

k 是缺陷出现的次数

p 是一个正实数，

* 1. **[15 Points]** In a defected chip, assume defects are independent and uniformly distributed within the die area. What is the probability that all defects in a DEFECTED die occur in the same core? (In other words, there is no defect on all other three cores and the L3 cache.) Please notice that there can be more than one detect on a die.

在有缺陷的芯片中，假设缺陷是独立的并且均匀分布在裸片区域内。 DEFECTED die 中的所有缺陷都发生在同一个核心中的概率是多少？ （换句话说，所有其他三个内核和 L3 缓存都没有缺陷。）请注意，一个芯片上可能有多个检测。

* 1. **[5 Point]** If there is only one defected core in a chip with defect-free L3, we can still sell it by shutting down the defected core. Suppose you can sell the perfectly working (defect-free) chip for $259.99 each. Also assume that you need $179 to manufacture and test each chip. What is the minimum sale price for your chips with 3 working cores (the defective core is shutdown) to make break even (no profit, no loss)?

如果 L3 无缺陷的芯片中只有一个有缺陷的内核，我们仍然可以通过关闭有缺陷的内核来出售它。 假设您可以以每个 259.99 美元的价格出售完美工作（无缺陷）的芯片。 还假设您需要 179 美元来制造和测试每个芯片。 你的芯片有 3 个工作核心（有缺陷的核心被关闭）以实现盈亏平衡（没有利润，没有亏损）的最低销售价格是多少？

1. **[40 points]** Assume that values of variables A, B, C and D reside in memory. Write the code sequence for

假设变量 A、B、C 和 D 的值驻留在内存中。 编写代码序列为

D = B\*(A+B-C) + A\*D

for four instruction-set architectures: i) Stack, ii) Accumulator, iii) Register-memory and iv) Register-register (Load-Store). (These four architectures are shown in Figure A.1 on page A-4 of the Appendix A). *Please* *do not perform any scheduling or other optimizations of the above code sequence!*

对于四种指令集架构：i）堆栈，ii）累加器，iii）寄存器存储器和 iv）寄存器寄存器（加载存储）。 （这四种架构显示在附录 A 第 A-4 页的图 A.1 中）。 请不要对上述代码序列进行任何调度或其他优化！

1. ARM instruction set offers an instruction to Load multiple registers.

ARM 指令集提供了加载多个寄存器的指令。

LDMIA R1,{R2,R7} will perform the following two operations:

将执行以下两个操作：

R2 = memory[R1], R7 = memory[R1+4];

In other words, we can replace

LOAD R2,0(R1)

LOAD R7,4(R1)

ADD R5, R7, R2

STORE R5, 4(R6)

**by**

LDMIA R1,{R2,R7}

ADD R5, R7, R2

STORE R5, 4(R6)

There are two different formats of LDMIA available: LDMIA R1,{R2,R7} and LDMIA R1,{R2-R7}. The first three can load 2 registers. The second format can load all registers in the range, i.e. LDMIA R1,{R2-R7} will perform the following operations:

R2 = memory[R1], R3 = memory[R1+4]; R4 = memory[R1+8], R5 = memory[R1+12]; R6 = memory[R1+16], R7 = memory[R1+20];

1. **[15 Points]** LDMIA is not currently supported by MIPS instruction set. Suppose all instructions are still 32 bits. Since this is an R-Type instruction, there are 6 bits reserved for opcode. Can you design the binary format (encoding) for this LDMIA instruction if we want to add it to MIPS? Please notice that your encoding should support instructions like LDMIA R1,{R2,R7} and LDMIA R1,{R2-R7}.

MIPS 指令集目前不支持 LDMIA。 假设所有指令仍然是 32 位。 由于这是一条 R-Type 指令，因此为操作码保留了 6 位。 如果我们想将 LDMIA 指令添加到 MIPS 中，你能设计它的二进制格式（编码）吗？ 请注意，您的编码应支持 LDMIA R1,{R2,R7} 和 LDMIA R1,{R2-R7} 等指令。

1. **[15 Points]** Assume that the new instruction will cause the clock cycle to increase by 2.5%. Assume that 26% of dynamic instructions are loads. The new instruction affects only the clock speed and not the CPI. If only 20% of load instructions can be eliminated by the new instructions, will the overall performance change? Indicate the change (e.g., if improved, by how much etc.?).

假设新指令会使时钟周期增加 2.5%。 假设 26% 的动态指令是负载。 新指令仅影响时钟速度而不影响 CPI。 如果新指令只能消除 20% 的加载指令，整体性能是否会发生变化？ 指出变化（例如，如果改进，改进了多少等？）。