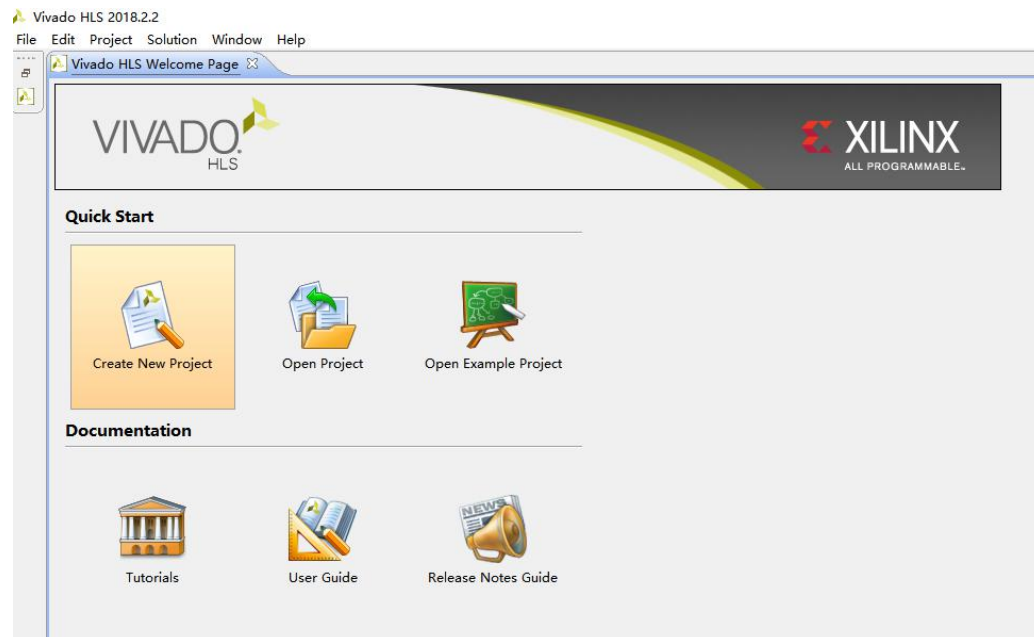


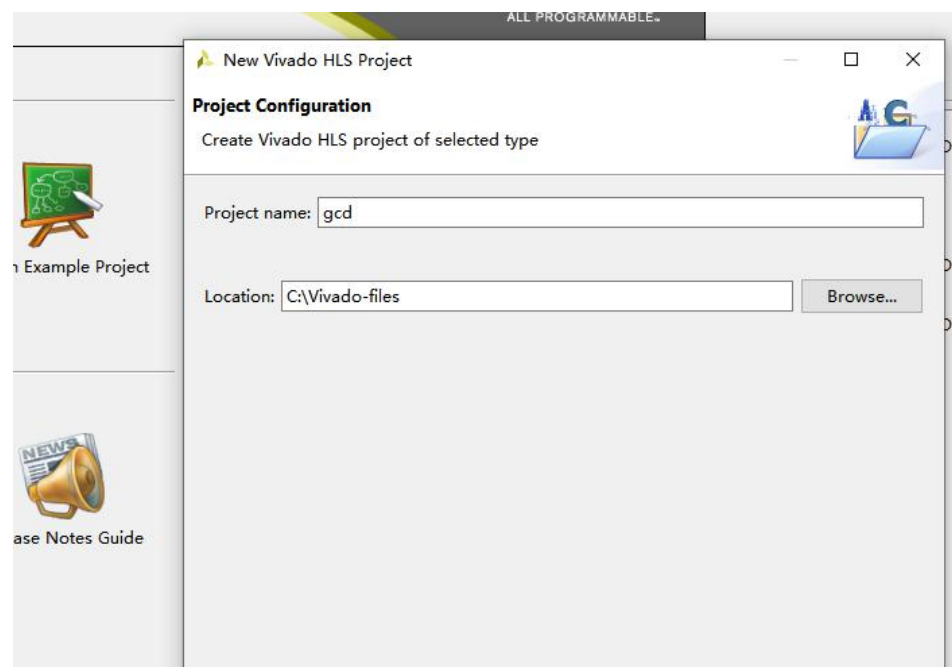
Vivado HLS 工程建立操作步骤及硬件性能获取方法

2022 年 4 月 7 日星期四

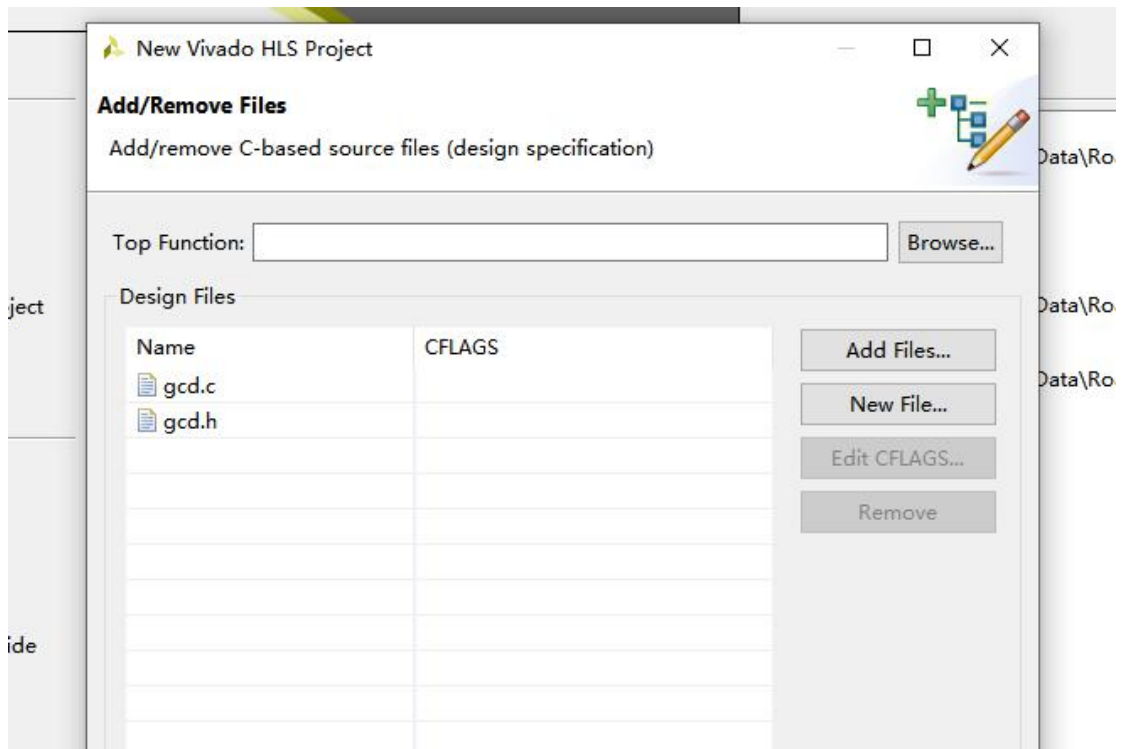
1、 打开 Vivado HLS 工具，选择 Create New Project



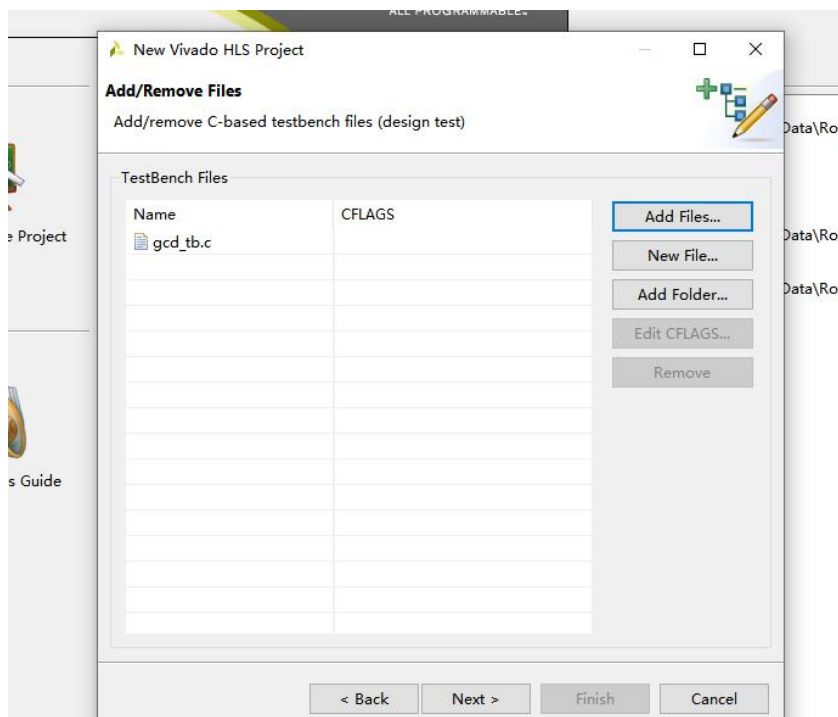
2、 在 Project Configuration 中添加 Project name gcd 和 Location，用来保存 Project GCD。按下 next 出现添加 top Function 和.h 与.c 文件。



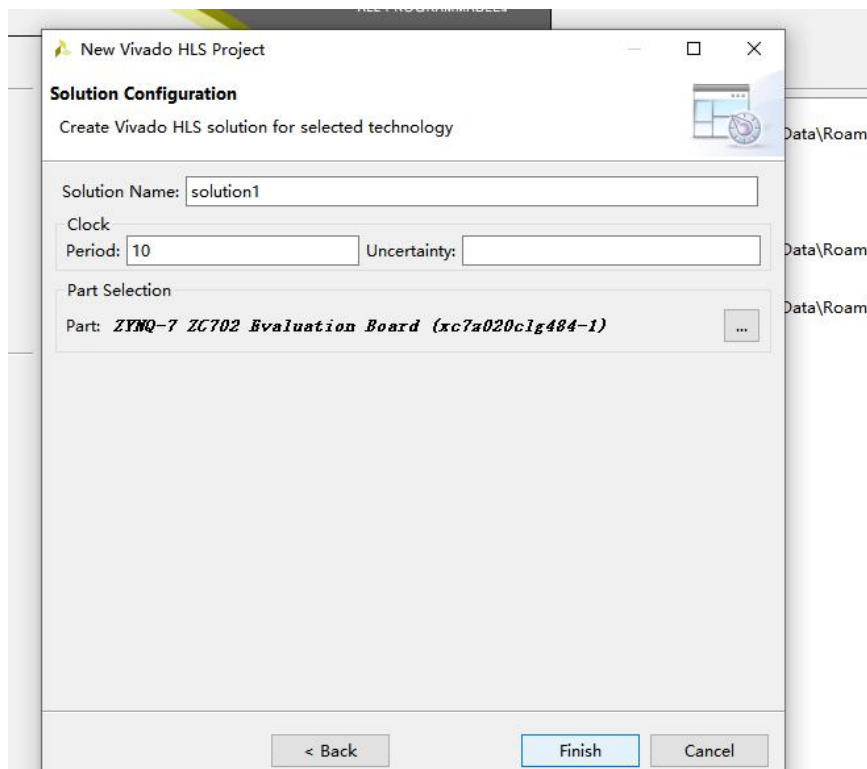
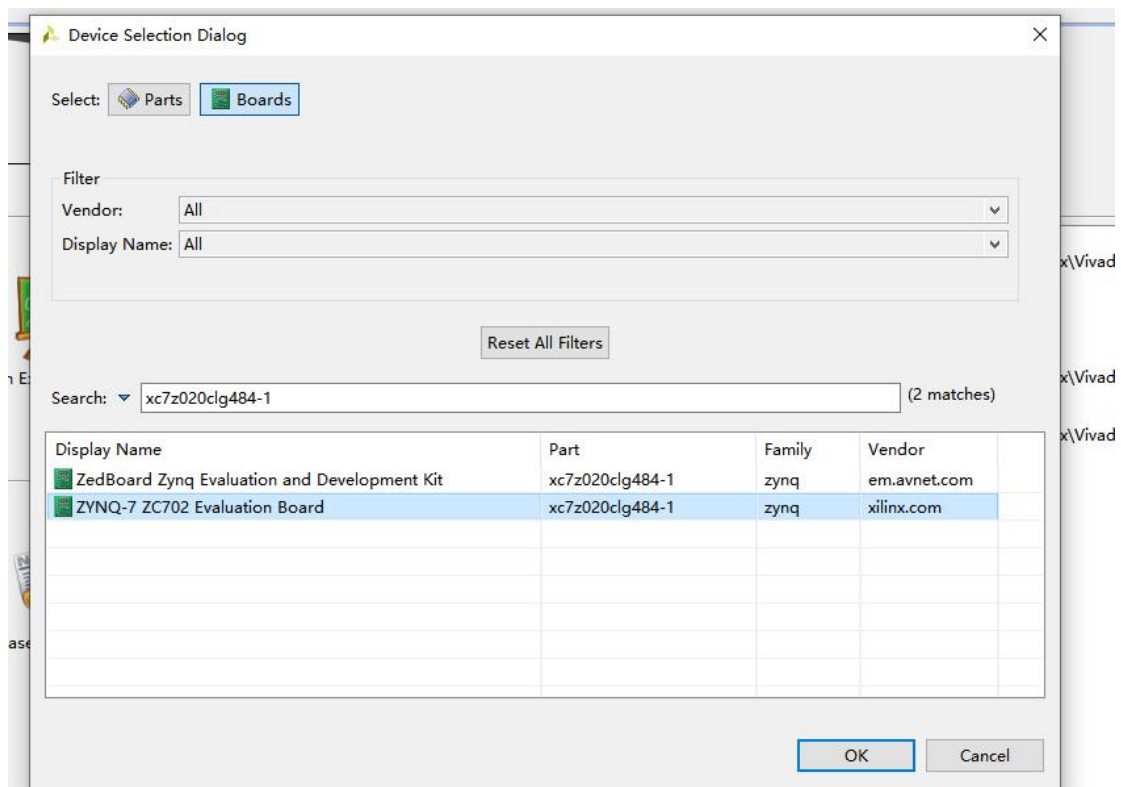
3、 Add/Remove files 界面: 在 Top function 中通过 Browse 选定 gcd, 通过 Add files 加上 gcd.c 和 gcd.h 两个文件。然后按 next, 进入添加测试文件。



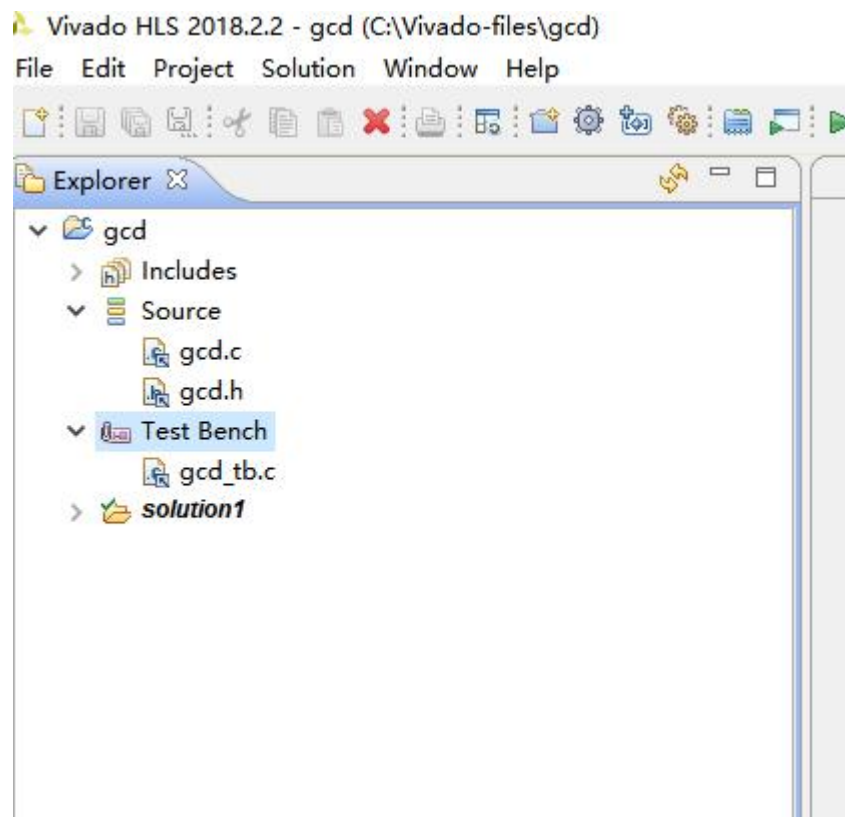
4、 Add 测试文件 gcd_tb.c，然后按下 Finish，进入选择 Board 界面。



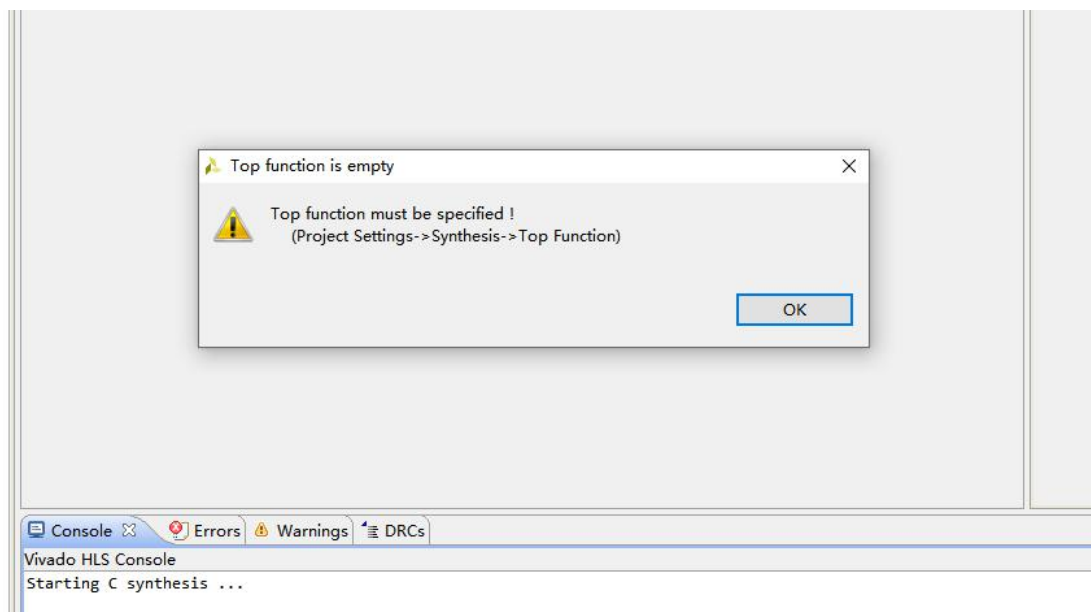
5、 选择 Board 界面，选择开发板，按下 OK 键，进入显示开发板选择界面，按下 Finish 进入 Explorer 界面

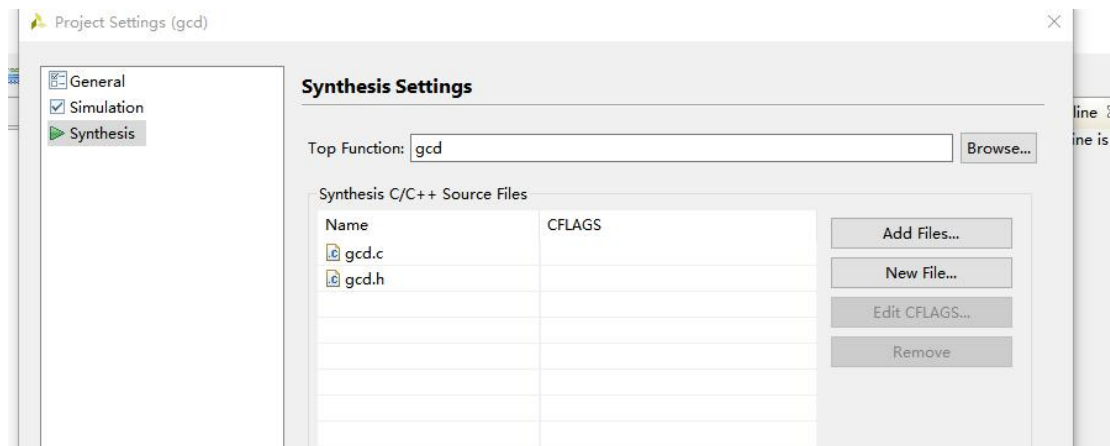


6、 Explorer 界面可以看到 GCD 目录下的 Source 子目录和 Test Bench 子目录，以及各自目录下的文件 gcd.c、gcd.h 和 gcd_tb.c。

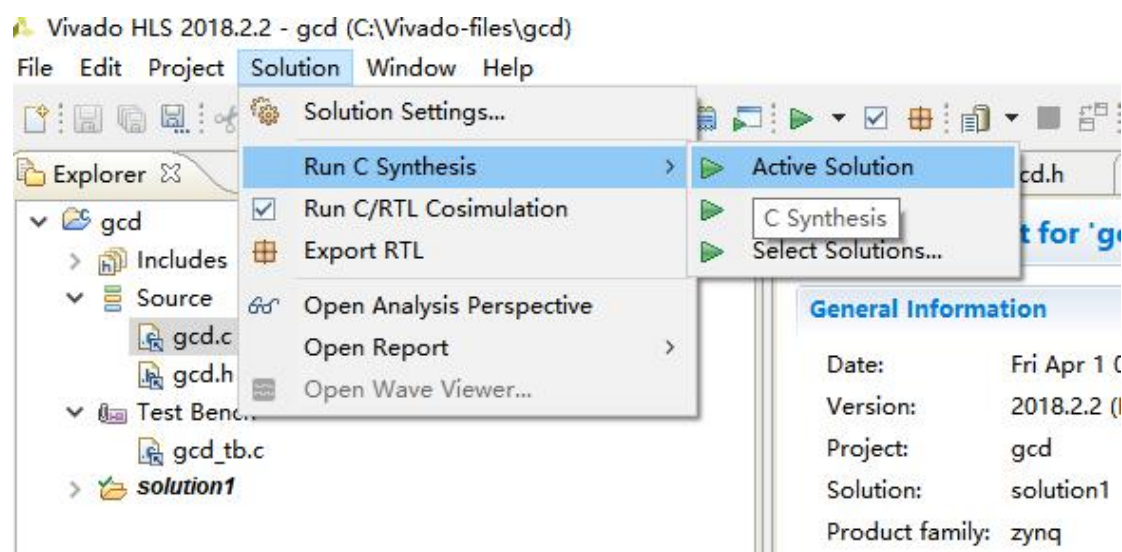


7、开始运行 C synthesis---由于在选择 top function 时没有选择，因而这时要补上，按下 OK 键。在 Explorer 选 Project Settings-Synthesis-Top Function，进入到了 Add/Remove Files 界面，通过 Browse 选择 gcd，这就设置了 Top Function，选择 OK 键。若在前面 3 中设置好了 Top Function，就可以省略这一步了。

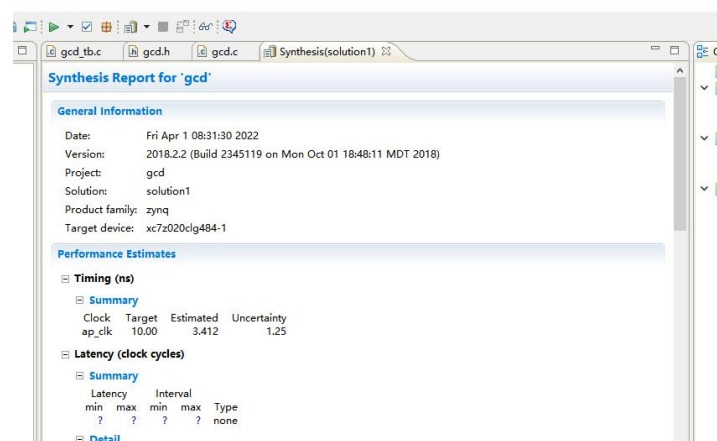




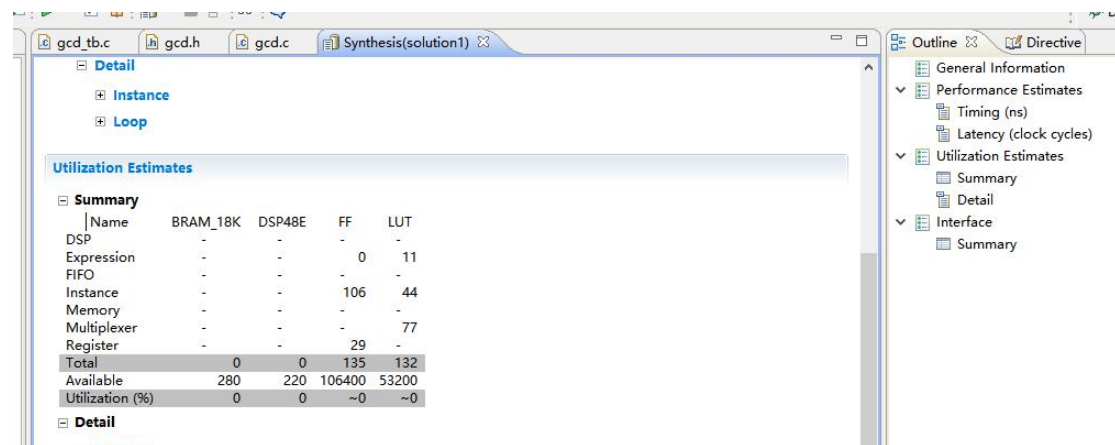
8、T 在 Explorer 界面选 Solution 栏, 选 Run C Synthesis-Active Solution, 对 GCD 进行合成了。



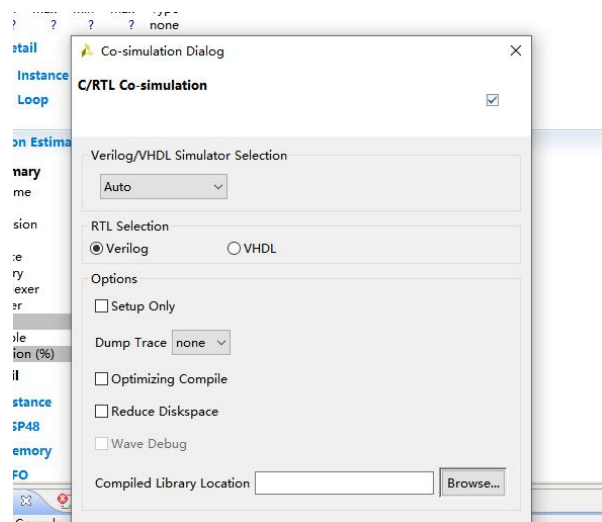
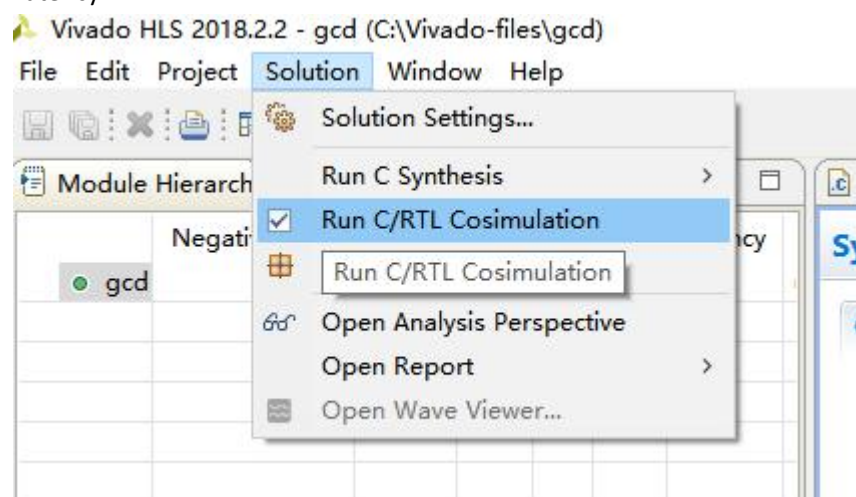
9、Synthesis Report for GCD 从中可以看到生成时间和开发板型号, 以及时间 Summary , 但没有 Latency 和 Interval。



10、在 Explorer 中选最右边框，点击 Utilization Estimates，可以看到查找表 LUT 等数。



11、在 Explorer 中 Solution 栏选 Run C/RTL Cosimulation，在 Co-Simulation Dialog 中选 verilog，按下 OK 键，运行开始，运行结束后给出 Cosimulation Report for GCD，从这报告中可以获得 Latency。



Cosimulation Report for 'gcd'

Result

RTL	Status	Latency			Interval		
		min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	49	49	49	NA	NA	NA

Export the report(.html) using the [Export Wizard](#)

Vivado HLS Console

```
## set tb_n_group [add_wave_group n(wire) -into $tbcinputgroup]
## add_wave /apatb_gcd_top/n -into $tb_n_group -radix hex
## set tb_m_group [add_wave_group m(wire) -into $tbcinputgroup]
## add_wave /apatb_gcd_top/m -into $tb_m_group -radix hex
## save_wave_config gcd.wcfg
## run all
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @ "Simulation Time"
// RTL Simulation : 0 / 1 [n/a] @ "125000"
// RTL Simulation : 1 / 1 [n/a] @ "635000"
$finish called at time : 675 ns : File "C:/Vivado-files/gcd/solution1/sim/verilog/gcd.autotb.v" Line 323
## quit
INFO: [Common 17-206] Exiting xsim at Sat Apr 2 10:08:47 2022...
INFO: [COSIM 212-316] Starting C post checking ...
result=4
```

12、打开 gcd_tb.c 调整测试用例中的参数 200 为 2000，计算 2000 与 148 的最大公约数，可以得到 Latency 值---49，执行时间为 675ns。

Cosimulation Report for 'gcd'

Result

RTL	Status	Latency			Interval		
		min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	49	49	49	NA	NA	NA

Export the report(.html) using the [Export Wizard](#)

Vivado HLS Console

```
## add_wave /apatb_gcd_top/ap_return -into $tb_return_group -radix hex
## set tbcinputgroup [add_wave_group "C Inputs" -into $testbenchgroup]
## set tb_n_group [add_wave_group n(wire) -into $tbcinputgroup]
## add_wave /apatb_gcd_top/n -into $tb_n_group -radix hex
## set tb_m_group [add_wave_group m(wire) -into $tbcinputgroup]
## add_wave /apatb_gcd_top/m -into $tb_m_group -radix hex
## save_wave_config gcd.wcfg
## run all
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @ "Simulation Time"
// RTL Simulation : 0 / 1 [n/a] @ "125000"
// RTL Simulation : 1 / 1 [n/a] @ "635000"
$finish called at time : 675 ns : File "C:/Vivado-files/gcd/solution1/sim/verilog/gcd.autotb.v" Line 323
## quit
INFO: [Common 17-206] Exiting xsim at Sat Apr 2 15:31:57 2022
```

13、再次调整 gcd_tb.c 中参数为 2000 和 114，得到 Latency 为 73，执行时间为 915。

The screenshot displays the Vivado HLS interface. The top tab is 'Simulation(solution1)'. The main window shows the 'Cosimulation Report for 'gcd'' with a 'Result' section containing a table of latency and interval data.

RTL	Status	Latency			Interval		
		min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	73	73	73	NA	NA	NA

Below the table, it says: 'Export the report(html) using the [Export Wizard](#)'.

The bottom panel shows the 'Vivado HLS Console' with the following output:

```
#####  
// Inter-Transaction Progress: Completed Transaction / Total Transaction  
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%  
//  
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @ "Simulation Time"  
#####  
// RTL Simulation : 0 / 1 [n/a] @ "125000"  
// RTL Simulation : 1 / 1 [n/a] @ "875000"  
#####  
$finish called at time : 915 ns : File "C:/Vivado-files/gcd/solution1/sim/verilog/gcd.autotb.v" Line 323  
## quit  
INFO: [Common 17-206] Exiting xsim at Sat Apr 2 15:26:58 2022...  
INFO: [COSIM 212-316] Starting C post checking ...  
result=2  
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***  
INFO: [COSIM 212-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will.  
Finished C/RTL cosimulation.
```