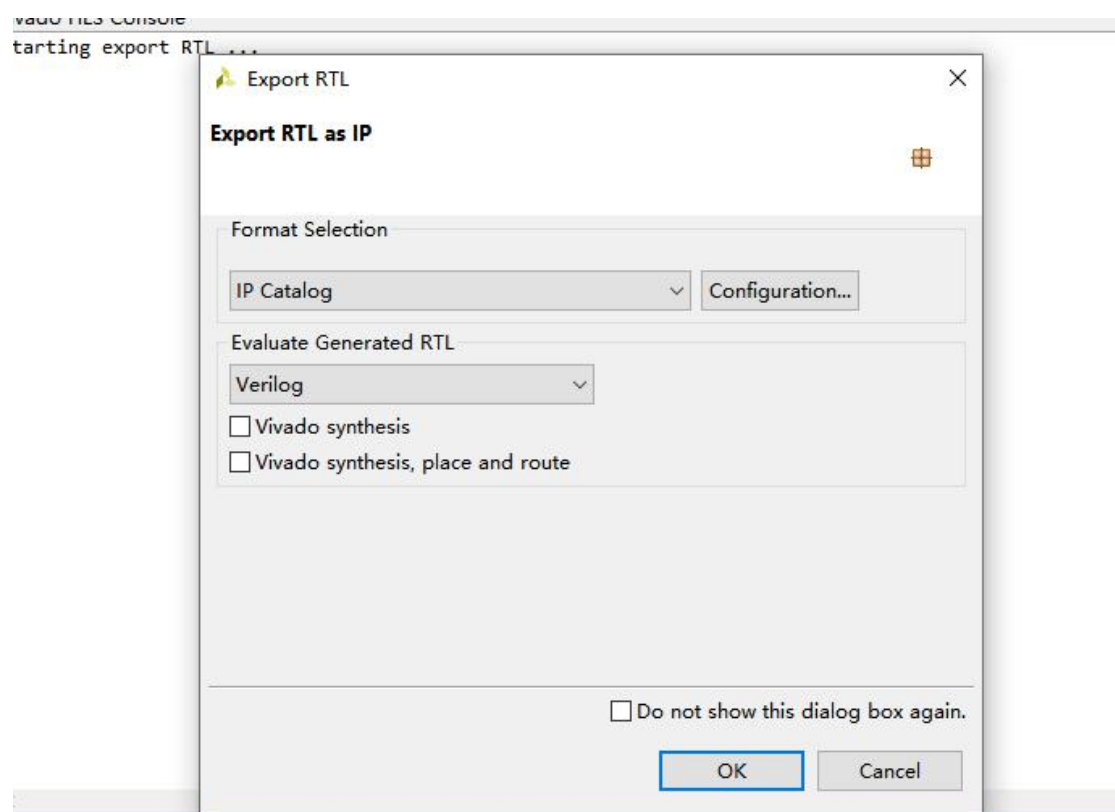
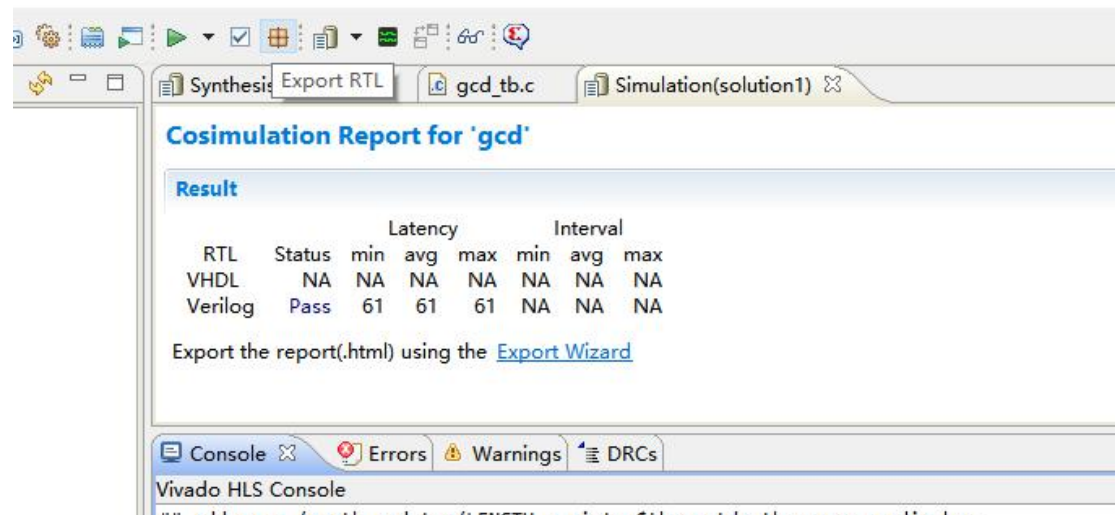


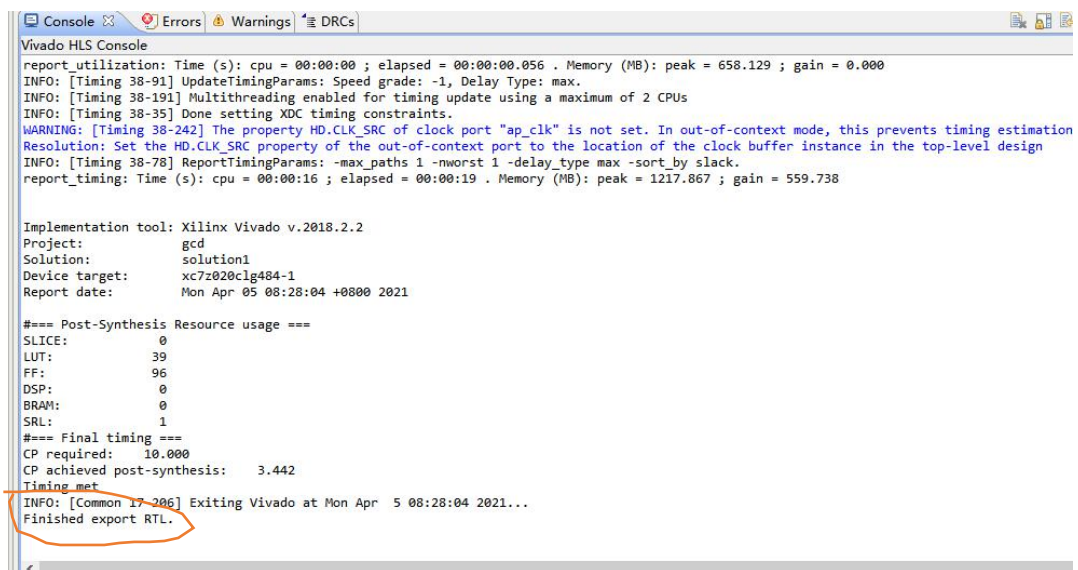
IP 核图形化生成步骤

2022 年 4 月 5 日

以 GCD 为例

1、在 vivado HLS 平台上生成 IP 核，需要注意的是将电脑时间改成 2021 年，否则会报错，不能生成。先运行 Export RTL。





```

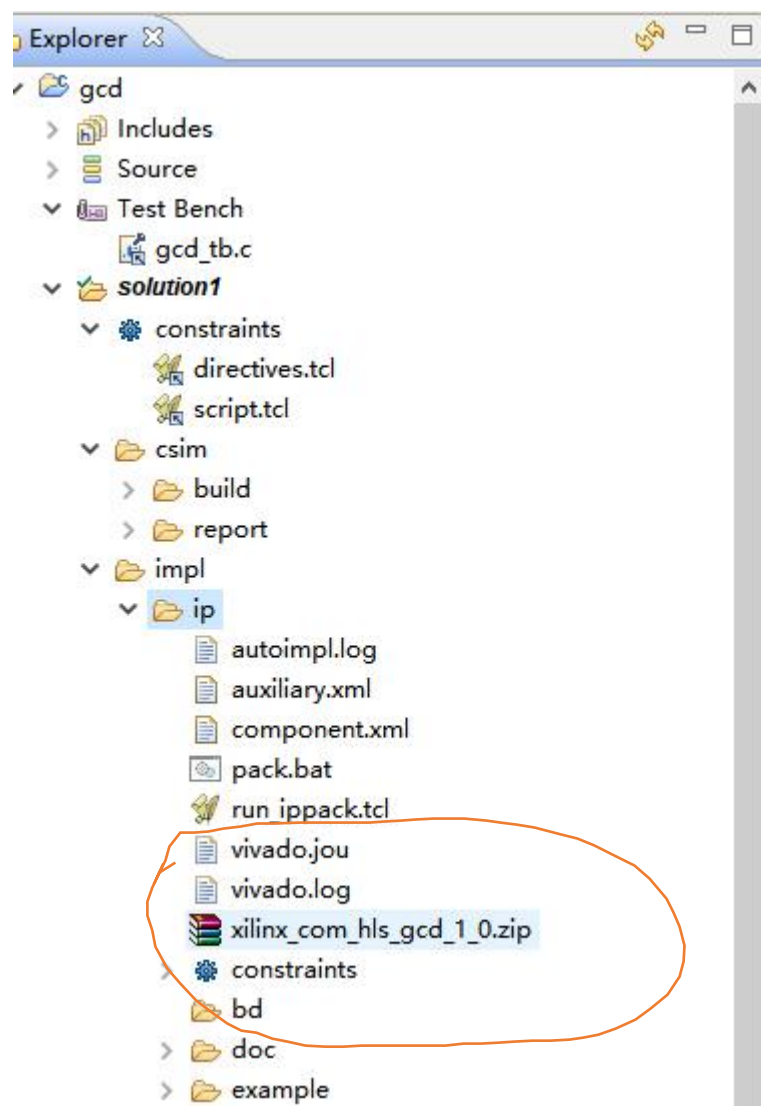
Vivado HLS Console
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.056 . Memory (MB): peak = 658.129 ; gain = 0.000
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
INFO: [Timing 38-35] Done setting XDC timing constraints.
WARNING: [Timing 38-242] The property HD.CLK_SRC of clock port "ap_clk" is not set. In out-of-context mode, this prevents timing estimation
Resolution: Set the HD.CLK_SRC property of the out-of-context port to the location of the clock buffer instance in the top-level design
INFO: [Timing 38-78] ReportTimingParams: -max_paths 1 -nworst 1 -delay_type max -sort_by slack.
report_timing: Time (s): cpu = 00:00:16 ; elapsed = 00:00:19 . Memory (MB): peak = 1217.867 ; gain = 559.738

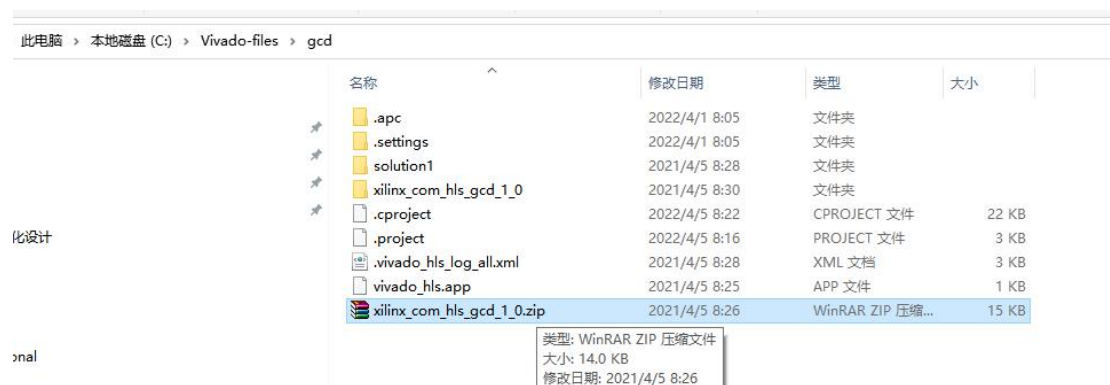
Implementation tool: Xilinx Vivado v.2018.2.2
Project: gcd
Solution: solution1
Device target: xc7z020clg484-1
Report date: Mon Apr 05 08:28:04 +0800 2021

==== Post-Synthesis Resource usage ====
SLICE: 0
LUT: 39
FF: 96
DSP: 0
BRAM: 0
SRL: 1
==== Final timing ====
CP required: 10.000
CP achieved post-synthesis: 3.442
Timing met
INFO: [Common 17-206] Exiting Vivado at Mon Apr 5 08:28:04 2021...
Finished export RTL.

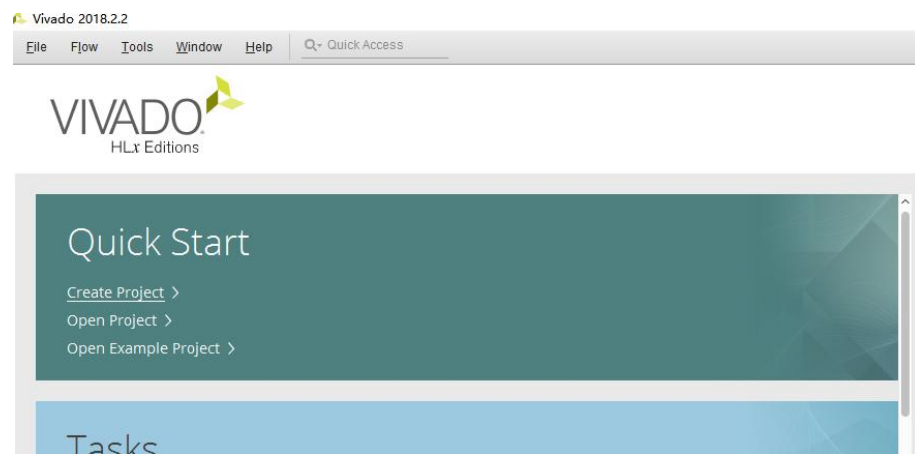
```

2、下载 IP，放在 c:vivado-files/gcd 文件夹下，然后解压获得含 IP 的子文件夹，保存 IP 核文件，这个文件夹在后面生成图形化 IP 核时添加 Sources 时使用。

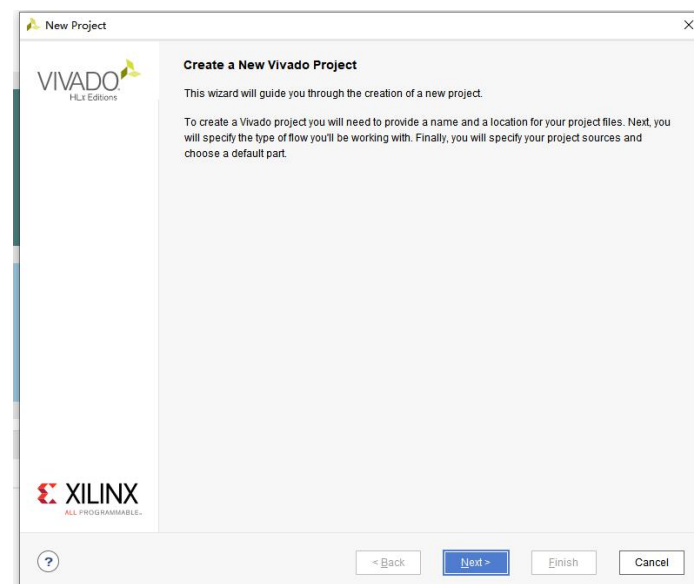




3、打开 Vivado 工具，Create New Project: Project_7



Create a new Vivado Project



定义 Project 名称 Project_7 和路径 C:/vivado-files

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at: C:/vivado-files/project_7

添加 Project 类型

New Project

Project Type

Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time

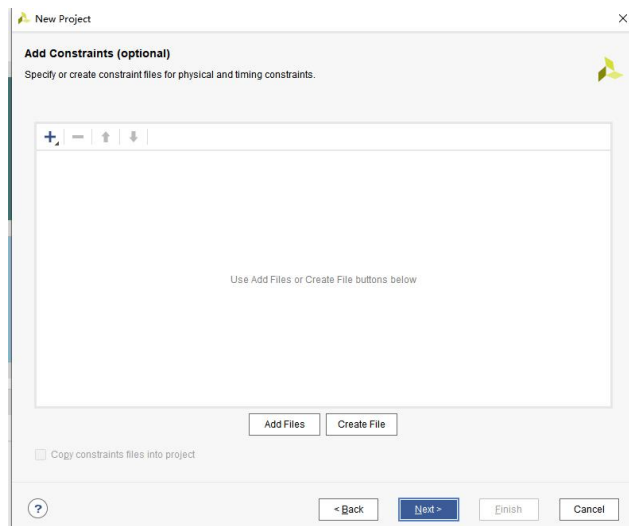
☐ **Post-synthesis Project**. You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

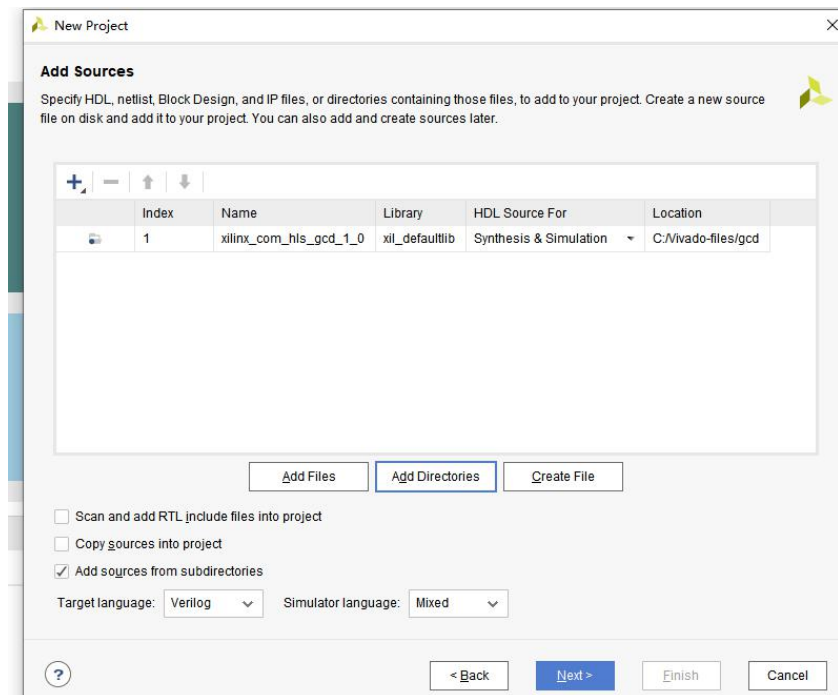
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

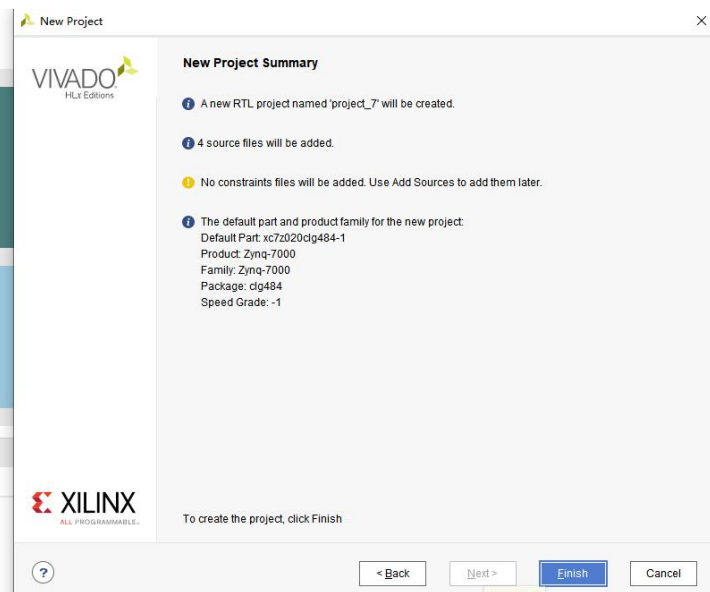
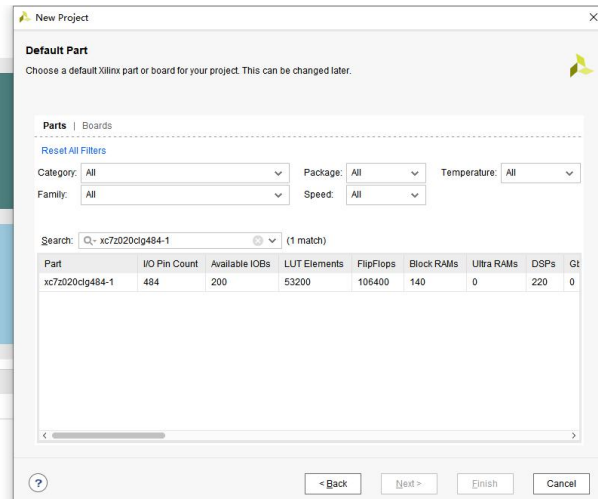
添加 Constraints (可以不加)



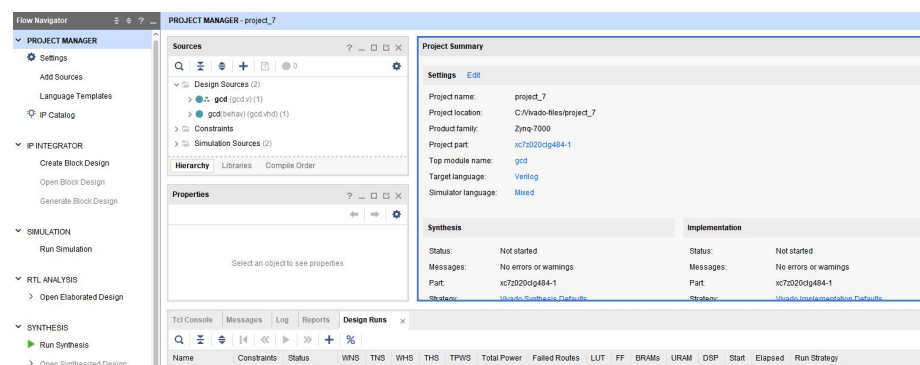
添加 Sources: 选路径---IP 解压后的文件夹 xilinx_com_hls_gcd_1_0。



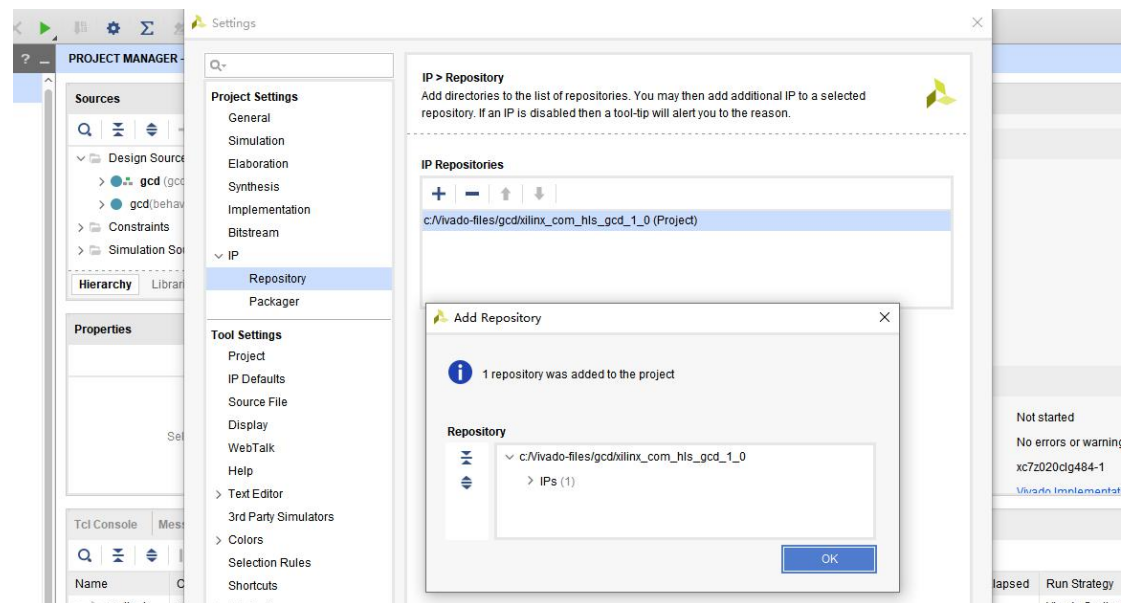
添加硬件板子: Part---xc7z020c1g484-1, 查找和选定。完成了 Project_7 的建立, 按 Finish 键后, 得到 Project_7 的信息汇总。



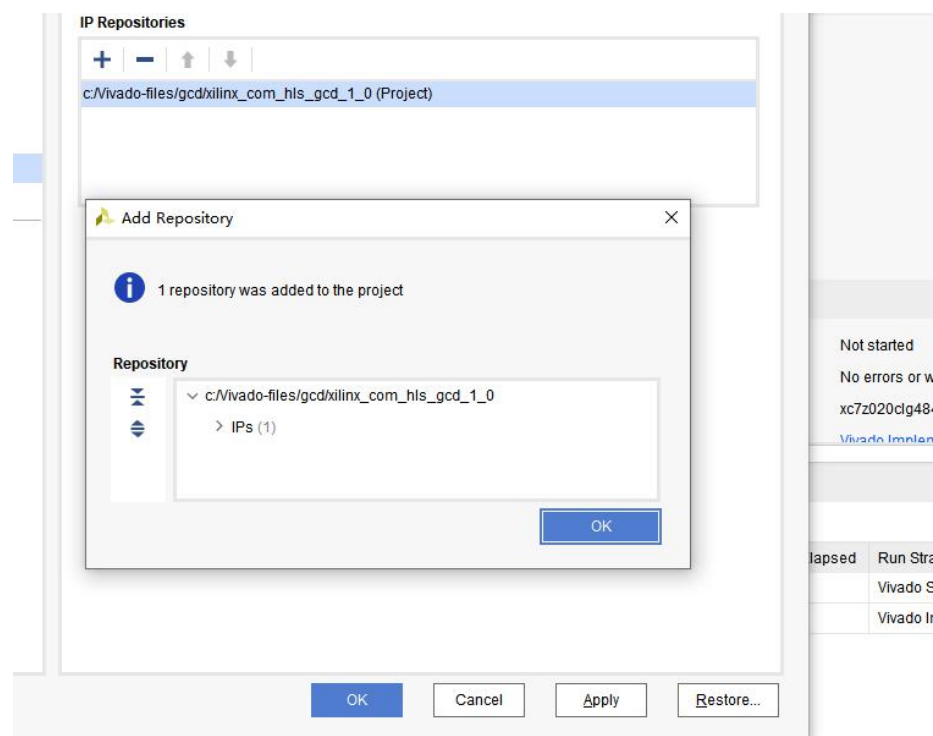
4、工程管理---Project Manager



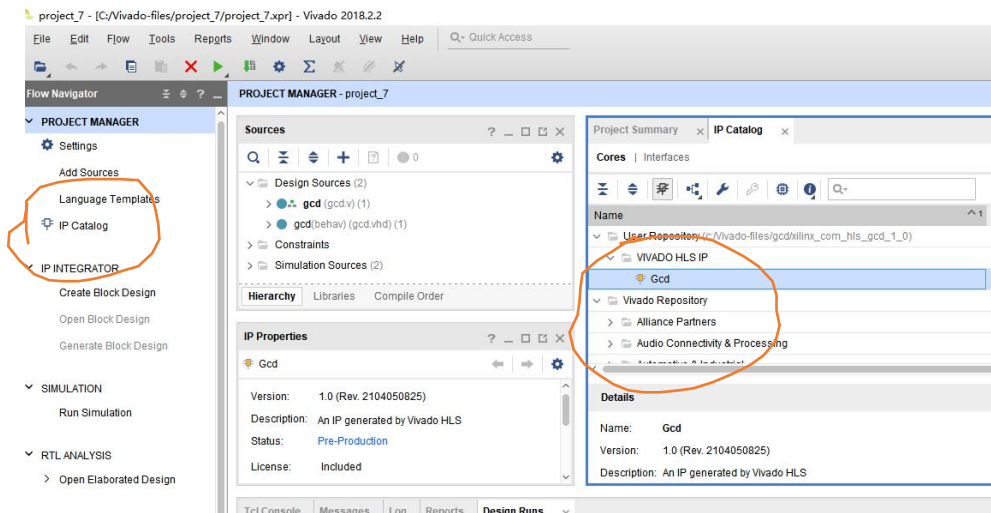
5、在 Project Manager 环境下打开 Setting 进行 IP Repository 添加，会自动选择路径，确认就行。



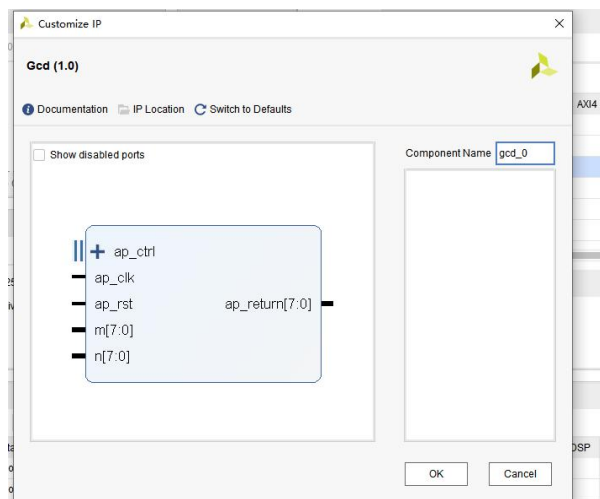
按下 OK 键后，再按 Apply 键，添加成功。



6、打开 IP Catalog, 选择 User Repository 目录下 VIVADO HLS IP, 可以看到 Gcd。



7、双击 Gcd 就可以生成 gcd 图形 IP 核



完成图形化 IP 核生成。

8、图形化 IP 核输出：按下 ok 键得到下面的图，再按下 Generate 键完成 Out-of-Content Model 生成

