A	General	AA	Card Punch
B	Source & Dest Code	BB	Teleprinter
C	Clock	CC	Inter Unit wiring
D	Chain	DD	Power Supplies
E	Sequence Unit MK II	EE	Current Instruction Store
F	Sequence Reg MK I	FF	Monitor Test Equipment.
G	Sequence Regs MK II	GG	Editing
H	Interpreter MK I	HH	Ventilating System
J	Interpreter MK II	JJ	Valve Tester
K	Time Selector	KK	Hg Delay Line Test Equipment
L	Line Selector + Reg		
M	Source + Dest Selector		
N	Input Units		
	Reader		
	Control		
	Register		
P	Constant Generator		
Q	Arithmetic Organ		
R	Multiplier Seq Unit		
S	Hg Delay Line Memory		
T	Magnetic Drum		
U	Output Reg + Control		
V	Start Unit		
W	Trigger Unit		
X	Header		
Y	Control Desk		
Z	Tape Punch		

SECTION F

SEQUENCE REGISTER MK I

Circuits

Input: D17155

Register: C22572

Output: C22571

1 The Register consists of 10 flip-flops into which the digits of a number may be read, added or counted.

2 The diodes V17-V25 connect the flip-flops so that they form a normal binary adder register, i.e. when V9 for example changes from 1 to 0 a negative pulse (or carry) is transmitted to V10 causing that valve to change sign. A change of V9 from 0 to 1 has no effect on V10.

3 Digits may be counted into the register via D3 and D4 from the 2 gate formed by V16. e.g. if the number 0101110111 is counted in, the contents of the register will be increased by 7.

4 Unit pulse may also be added into the register via D3 and D4 and terminal P2-2.

5 The diodes D1, D2, D33, D34 etc. enable a number to be added into the register. i.e. if V9 for example is registering either a 1 or a 0 then a negative pulse on terminal 9 will change V9 to a 0 or 1. If the former change takes place a carry will be propogated in the normal manner.

6 When destination $\rightarrow$S is selected a clear pulse is sent to the register. This pulse is formed from the differentiated front of P4-25, an amplifier V13-a and the normally conducting, tube V13(b).

7 Read out from the register is conventional through 2 gates with chain pulses and a three gate V26a, V28a and V29b with destination and clock pulses.

8 V30b is an inhibitor to prevent read out during the P2-6 interval as otherwise there would be interference with the Interpreter read out. The diode D1 prevents the anode of V29(b) going negative during the inhibition period.

SECTION H

INTERPRETER MK I

Circuit Drawings

Input: C22587

Register: C22588

Output: C22586

1 The Interpreter register contains 20 flip-flops into and out of which numbers may be read in a conventional manner.

2 Circuit drawing B22588 shows extra circuits for the K+ operation (diodes D1 - D40, V23, V22 etc.) which however are not used. This operation has been eliminated until Mk II is installed.

3 Read In chassis voltage measurements.

(a) Bias line on gates = 17·5 V.

(b) Bias on amplifiers = -33 V.

(c) Amplitude of Input pulses

P1	-	56 V
P2-3	-	58 V
P5	-	58 V

(d) V33 cathode

Main pulse	-	44 V
Breakthrough	-	5 V

(e) V45 plate

Pulse	-	34 V
Breakthrough	-	7 V

V45 has unequal grid base voltages. Chain is +19 V, other pulses + 11 volts. Very little improvement is made by equalizing these.

(f) Output pulse from Read In on V30 plate -21 volts.

4 Interpreter Register voltage measurements.

(a) Biases on flip-flops should be ≏ -20 volts without P3 plug in and -15 volts with it in. + ve bias is +3 to +4 volts.

(b) V21 Bias = -58 V

g1	k1	g2	k2
-65	-57	-82	-65.

(c) V22

+16	+33	-68	-60.

(d) Flip-flop V1 H.T. = 205

-19, +125, 0; 2·8, 62, 0.

(e) Bias on diodes at end of 5K = +7V.

(f) Amplitude of P2-7 = 80 V

V22 cath = 52 V 40 µsecs long

V21 cath = 56 V 20 µsecs long

(g) Plate voltages at flip-flops. P14.

A	22	F	35
B	28	G	29
C	33	H	26
D	29	J	30
E	22	K	34.

5 Interpreter Read Out chassis voltage measurements.

(a) Bias on grids of Chain 2 gates.

Chain = +20 volts.

A	19	F	28
B	23	G	24
C	26	H	22
D	24	J	24
E	19	K	27

(b) Output pulse amplitudes on P7 & P6 = 60 V.

(c) V29 cathode 29 V

V30 grid 30 V

screen 90 V

anode 62 V

D1 cathode 130 V.

SECTION J

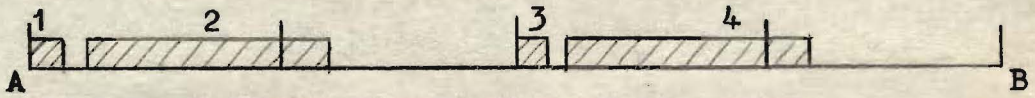
INTERPRETER MK II

Circuit: SKE5183

Logical Schematic: SKE5182.

1 The Interpreter was redesigned because of the necessity of incorporating the K+ transfer described under the notes on destinations (No. 27). The use of a Hg delay line and the standard adder circuit simplifies read in, adding and read out.

2 The operation cycle is as follows:



A is the start of the 4 major cycle period.

(a) During minor cycle 1 the Interpreter is cleared unless the previous instruction is K+ (P4-22).

Flip-flop V19 remembers the previous instruction if it included the destination K+ and inhibits the P2-1 clearing pulse via V4b.

(b) During the major cycle 2 the current command is added from the memory to the contents of the Interpreter

The two gate D2, D3 feeds into the adder.

(c) During the same major cycle (2) the lower half of the command is also read into the static register V34 to V52.

(d) During minor cycle 3 read out from the Interpreter occurs. P2-6 gates out the contents of the Hg delay line onto trunk P7. The static register is connected directly to the source and destination selectors.

(e) During the major cycle 4 any digits on the P5 trunk are <u>read</u> into the Hg line register.

SECTION B

SOURCE AND DESTINATION CODE & FUNCTION

SOURCE CODE

Code	Plug No.	Symbol		Symbol for printing out program	Ref. Note
00000	4	M	Mercury Line Memory	M	
00001	3	I	Input	I	1
00010	20	N1	Constant Register	NA	2
00011	19	N2	"	NB	2
00100	12	A	A Register	A	3
00101	11	p20.A or s.A	"	SA	6
00110	28	½A	"	HA	11
00111	27	2A	"	TA	10
01000	8	p1.A or 1.A	"	LA	7
01001	7	cA	"	CA	5
01010	24	Z.A	"	ZA	8
01011	23	B	B Register	B	3
01100	16	R	Round Off	R	9
01101	15	rB	B Register	RB	12
01110	32	C	C Register	C	3
01111	31	p20.C or s.C	"	SC	6
10000	2	rC	"	RC	12
10001	1	Dm	D Register	D	4
10010	18	p20.Dm or s.Dm	"	SD	6
10011	17	rDm	"	RD	12
10100	10	Z	Zero	Z	14
10101	9	H1	H Register	HL	13
10110	26	Hu	"	HU	13

Code	Plug No.	Symbol		Symbol for printing out program	Ref. Note
10111	25	S	Sequence Register	S	15
11000	6	p11		PE	2
11001	5	p1		PL	2
11010	22	K	Interpreter	K	15
11011	21	M1	Magnetic Drum Store	MA	16
11100	14	M2	"	MB	16
11101	13	M3	"	MC	16
11110	30	M4	"	MC	16
11111	29	p20		PS	2
			DESTINATION CODE		
00000	4	M	Mercury Line Memory	M	
00001	3		Unused		
00010	20	Ot	Output Printer	OT	17
00011	19	Op	Output Punch	OP	18
00100	12	A	A Register	A	19
00101	11	+A	"	PA	21
00110	28	-A	"	SA	21
00111	27	.A	"	CA	28
01000	8	vA	"	DA	29
01001	7	A	"	NA	30
01010	24	P	Hooter	P	34
01011	23	B	B Register	B	19
01100	16	xB	Multiply	XB	31
01101	15	L	Shift Product Left	L	32
01110	32	C	C Register	C	19

Code	Plug No.	Symbol		Symbol for printing out program	Ref. Note
01111	31	+C	C Register	PC	21
10000	2	-C	"	SC	21
10001	1	Dm	D Register	D	20
10010	18	+Dm	"	PD	22
10011	17	-Dm	"	SD	22
10100	10	Z	Zero	Z or Hyper-symbol	33
10101	9	H1	H Register	HL	23
10110	26	Hu	"	HU	23
10111	25	S	Sequence Register	S	24
11000	6	cS	"	CS	25
11001	5	+S	"	PS	26
11010	22	+K	Interpreter	PK	27
11011	21	M1	Magnetic Drum Store	MA	35
11100	14	M2	"	MB	35
11101	13	M3	"	MC	35
11110	30	M4	"	MD	35
11111	29	T	Stop Sequence Unit	T	36

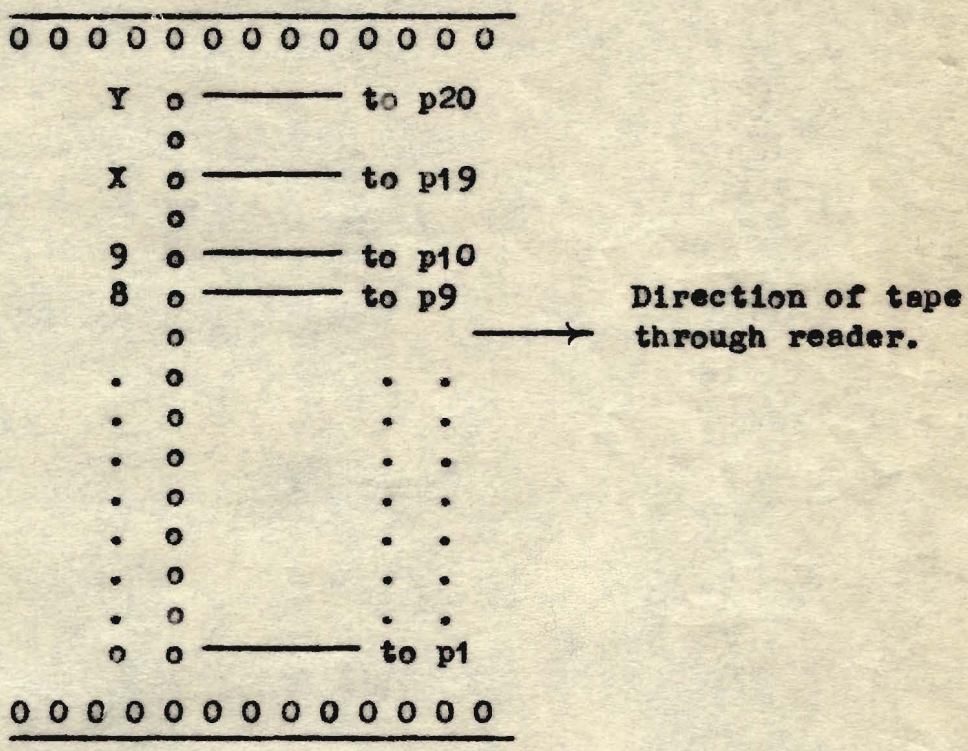
SOURCE FUNCTION

Reference Notes

1 <u>I Input Register</u>

The 20 digit register may be set up by means of switches on the control panel or pulses from the 12 hole tape reader.

The tape reader transfers the information from the tape to the digit positions p1 - p10, p19, p20 as shown below.



2 <u>N1, N2, p20, p11, p1</u>

These digits are derived from the constant generator chassis. N1 and N2 are each 20 digit registers which may be hand set by means of switches on the control panel.

p20, p11, p1 are single digit sources which read out unit digits in the time position indicated by the subscript.

3 <u>A, B, C</u>

Read out the contents of the A, B C registers respectively.

4 <u>Dm</u>

Read out the contents of the minor cycle of 20 digits in

D register located in time position "m".

5 <u>cA</u>

Reads out the contents of the A register and leaves A cleared to zero.

6 <u>sA, sC, sD</u>

Read out in time position p20 the digit located in the time position p20 of the registers A, C, D respectively.

7 <u>p1A</u>

Reads out in time position p1 the p1 digit of A.

8 <u>ΣA</u>

Reads out a unit digit in the p1 time position if the contents of A is not zero, otherwise a zero is read out.

9 <u>R</u>

Reads out in time position p1 the p20 digit of the contents of B.

10 <u>2A</u>

Read out the contents of the A register multiplied by 2. This also applies to positive and negative numbers but implies that the original contents of A must have a modulus less than ½.

11 <u>½A</u>

Read out the contents of the A register divided by 2. This applies whether the number is positive or negative.

12 <u>rB, rC, rD</u>

Reads out the contents of the B, C, D registers shifted one position to the right. The p1 digit in the original number is lost and the p20 digit in the new number is always zero.

13 <u>H1, Hu</u>

Reads out the contents of the 10 digit register in the time position p1 - p10, p11 - p20 respectively.

14 <u>Z</u>

Reads out zero.

15 <u>S, K</u>

Reads out in time positions p11 - p20 the ten digit content, p11 - p20, of the register.

16 <u>M1, M2, M3, M4</u>

The suffix refers to the section of the magnetic store which has a total capacity of 4096 words.

DESTINATION FUNCTION

17 <u>Ot</u>*

Read into the output register in time positions p1 - p5 or p11 - p15 and print the corresponding character.

18 <u>Op</u>*

Read into the output register in time positions p1 - p10, p19, p20 and punch onto tape.

19 <u>A, B, C</u>

Read into register A, B, or C respectively.

20 <u>Dm</u>

Read into the minor cycle of the D register located in time position "m".

21 <u>+A, +C, -A, -C</u>

Add to or subtract from the contents of the A, C registers resp. Any overcarry is lost.

---

* Refer Output Register Schematic attached (p).

22 <u>+Dm, -Dm</u>

Add to or subtract from the contents of the minor cycle in the D register located in time position "m". The overcarry is inhibited and lost.

23 <u>Hl, Hu</u>

Read into the H register the digits of the entering number which are in time positions p1 - p10, p11 - p20 resp.

24 <u>S</u>

Read into the Sequence Register the digits of the entering number which are in time positions p11- p20. The normal "add one" pulse is inhibited.

25 <u>cS</u>

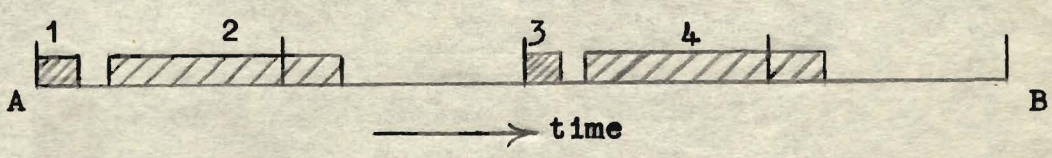
Count into the Sequence Register the number of digits entering e.g. if the entering number is 0001011100001101 then the Sequence Register will change to n + 8 where n was the number of the instruction which called for the destination cS. The extra "one" is due to the normal "add one" pulse which is not inhibited.

26 <u>+S</u>

Add to the contents of the sequence register the digits of the entering number which are in time positions p11 - p20. e.g. if the entering number is 00000, 00110, 00001, 11001 then the Sequence Register will change to n + 7 where n was the number of the instruction which called for the destination +S. The extra "one" is due to the normal "add one" pulse which is not inhibited.

27 <u>+K</u>

Read into the Interpreter Register and modify the following cycle so that the next command is added to the number held in the Interpreter following the K+ transfer. This means that the normal clearing pulse to the interpreter, which occurs at the beginning of the cycle, is inhibited.



(a) During minor cycle 1 the Interpreter is cleared unless the previous instruction is cleared unless the previous instruction is K+.

(b) During the major cycle 2 the current command is added from the Memory to the contents of the Interpreter.

(c) During minor cycle 3 read out from the Interpreter.

(d) During the major cycle 4 read into the Interpreter if the destination is K+.

28 <u>.A</u>

Replace the contents of register A by the digit by digit product of its contents and the entering digits (i.e. conjunction). i.e. the contents of the register and the entering number are compared digit by digit as the digits enter and the final contents are determined according to the following

Register A	Entering digit	Final digit
0	0	0
0	1	0
1	0	0
1	1	1

29 <u>vA</u>

Replace the contents of register A by the digit by digit logical sum of its contents and the entering digits (i.e. disjunction).

The rule in this case is as follows:-

Register A	Entering digit	Final digit
0	0	0
0	1	1
1	0	1
1	1	1

30 <u>~A</u>

Replace the contents of register A, digit by digit, by a unit digit whenever the digit in register A differs from the corresponding digit of the entering number.

Register A	Entering digit	Final digit
0	0	0
0	1	1
1	0	1
1	1	0

31 <u>XB</u>

Read into Register B, from the product of the content of B and register C (modulo 2) and add to the original content of register A, retaining the lowest 19 digits of the product in B with a zero in the p1 position of B.

[(A) = a, (B) = b, (C) = c, prod. = $x + 2^{-19} y$; a,b,c,x, 20 digit fractions; y, 19 digit fraction. (A)' = a + x, (B)' = 2y, (C)' = c] .

32 L

Only if a unit in the p20 position is received, shift the contents of registers A and B, considered in series, one place to the left. The digit in the p20 position of B shifts to the p1 position of A and the digit in the p20 position of A shifts to the p1 position of B.

33 Z

This is a null destination, having no effect on computer contents except for c(A)—— Z. Normally used only for marking hyper-commands and so Z destination commands are printed in hyper-symbols.

34 P

Any digit sent to P produces an audible click in a loudspeaker.

35 M1, M2, M3, M4

Read into the magnetic drum store. The suffix refers to the section of the store which has a total capacity of 4096 words. This is effective only if drum writing power is switched on.

36 T

Any pulse or pulses sent to T stop the sequence unit at the end of the current cycle.

SECTION C

CLOCK UNIT

Circuit: B17800

Block Schematic: Refer RPR117 Fig. 5.

1. DIVIDERS AND PULSE FORMING CIRCUITS

The screen-grid and cathode of V1 act as an oscillator tube operating at approximately 300 kc/s. The output is fed via a transformer and phase shift network to two pulse forming circuits. These produce C pulses displaced by an amount fixed by the adjustment of the phase shift network in series with the lead to V28.

The grid of V16 is driven negative and produces a pulse at the plate of V16 of a width depending on the values of L and C. (Fig. 1(a)). This pulse is amplified and fed finally via a group of paralleled cathode followers to terminal P1. These pp' pulses are fed throughout the computer via a coaxial cable which is terminated in a non-inductive 75 ohm resistor. The amplitude of the pulses may be adjusted by means of an amplitude control potentiometer (V19).

The pp pulse forming network is similar. These pulses are fed into a blocking oscillator divider chain V5-V13 which divides in the ratios 5, 4, 2, 4, 2 to form pulses of p and c frequencies.

The L, C circuits in the cathodes of V5 and V7 are adjusted to assist in the stability of these dividers.* Fig. 2(c) shows the waveform on the cathode. Maximum discrimination is obtained when the blocking oscillator fires in the trough of the cathode oscillation.

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* See Vol.19 M.I.T. R.L. Series.

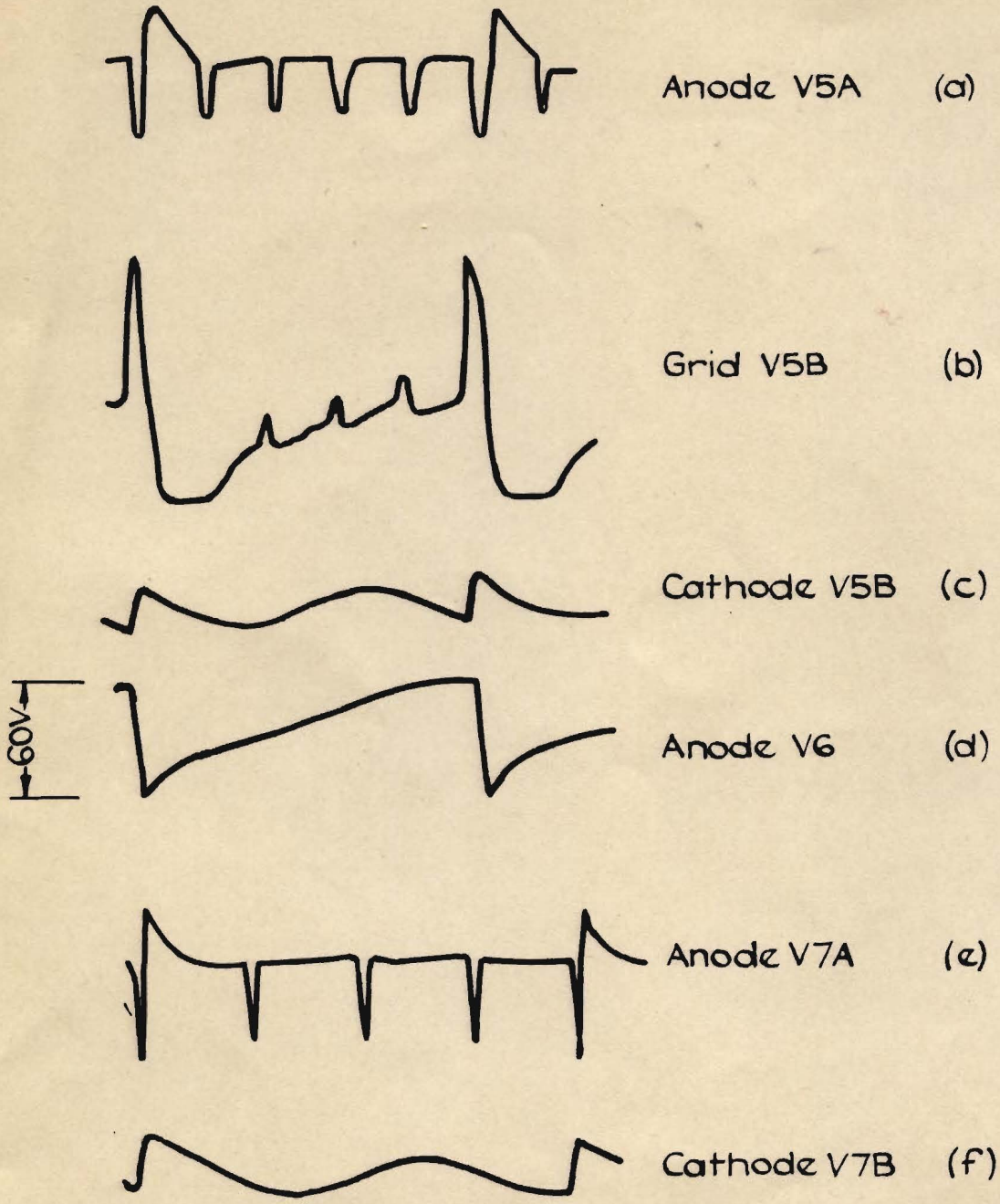

Anode V5A (a)
Grid V5B (b)
Cathode V5B (c)
60V
Anode V6 (d)
Anode V7A (e)
Cathode V7B (f)

FIG. 2 (a – f)

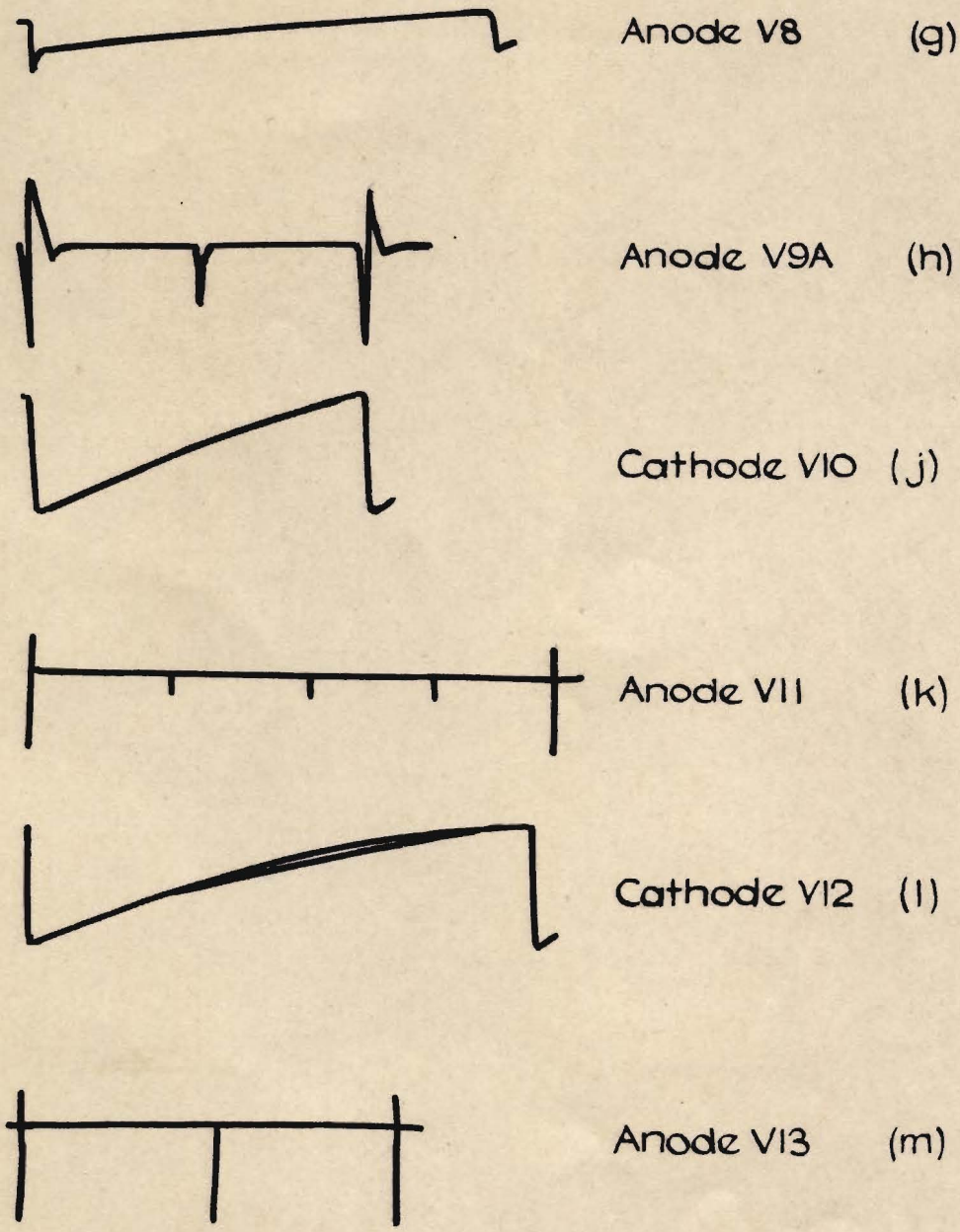


FIG. 2 (g-m)

R.P.L. 99

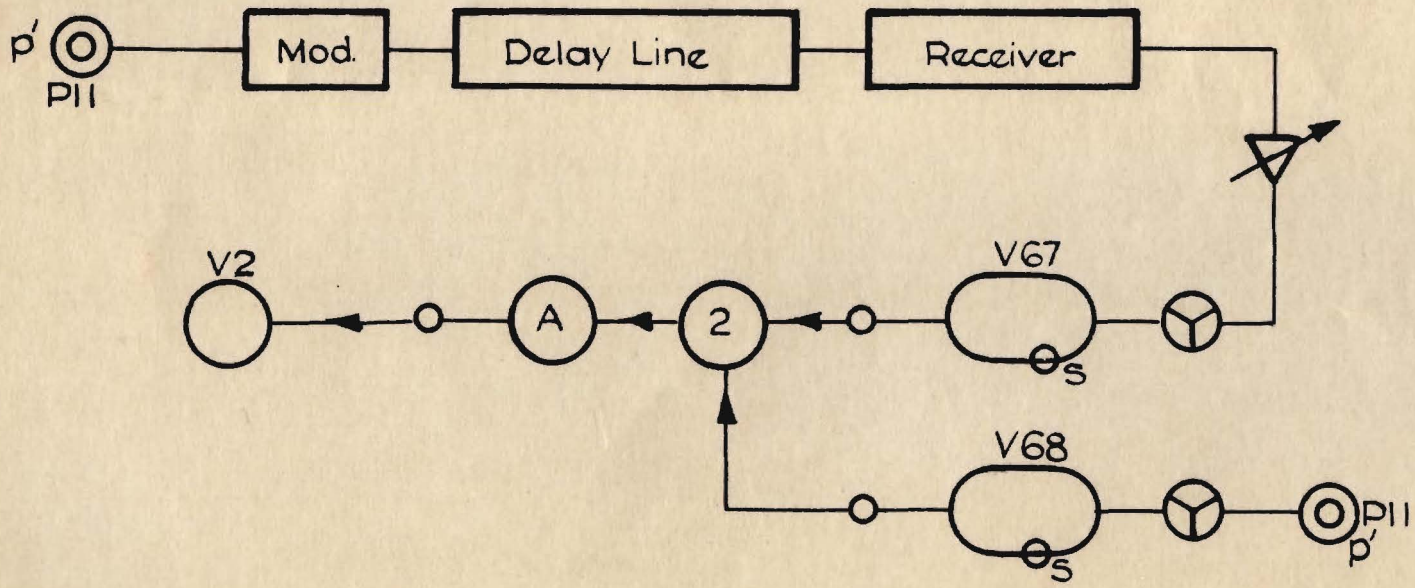


FIG. 3

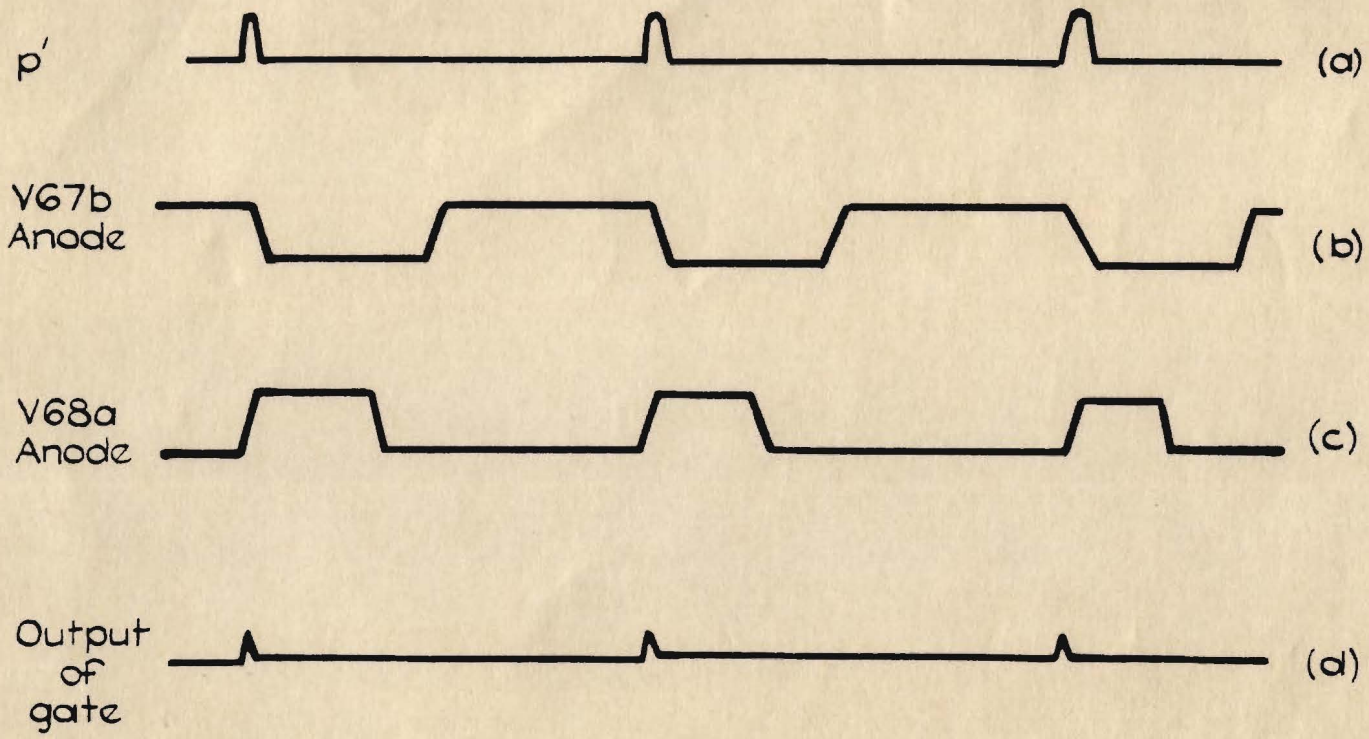


FIG. 4

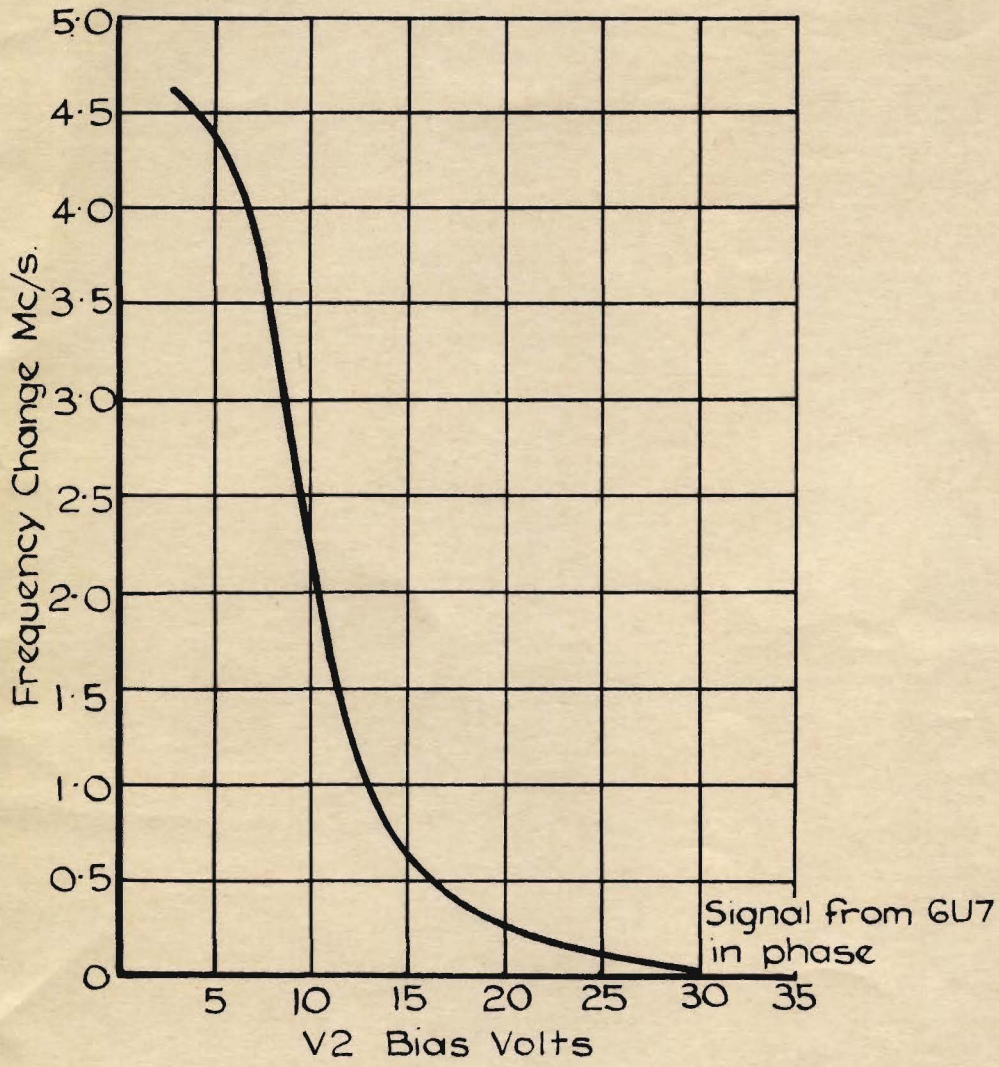

5·0
4·5
4·0
3·5
3·0
2·5
2·0
1·5
1·0
0·5
0
Frequency Change Mc/s.
5
10
15
20
25
30
35
V2 Bias Volts
Signal from 6U7
in phase

FIG. 5

RPL 99

SECTION D

CHAIN UNIT

Circuit: C22574, C22577

Block Schematic: Fig. 7, RPR117.

The Chain Unit generates a set of 20 pulse trains which are used for feeding digit pulses into and out of store registers, inhibiting carry pulses etc. Referring to the Block schematic the p pulses set up the flip-flops so that all except the first one are in the "off" position. The pp pulse which occurs at the time of the p pulse is inhibited in order to prevent interference with the setting up function. The pp pulses which then occur between the p pulses are applied to one of the common cathode lines and result in the flip-flops being "on" in turn for approximately 2 μsecs.

As an example suppose that V1 is in the "on" position, i.e. the plate to which the terminal 1 is connected is up while the plates connected to the other terminals are down. When the next pp pulse arrives, the conducting side of V1 will be cut off and a positive pulse will be sent to V2 via the 30 pf condenser. V1 and V2 will then flip over while all the other flip-flops will remain as before. The process is repeated and continues down the chain until the next p pulse starts the cycle again.

The two common cathode lines should be at approximately the same base potential - measured with the CRO, under normal operating conditions.

The diode D1 speeds up the re-setting of V20 which is brought about by the clearing pulse and not by a pulse on the cathode line as occurs for all the other flip-flops.

V23(b) holds V24 anode at earth potential.

VOLTAGE MEASUREMENTS

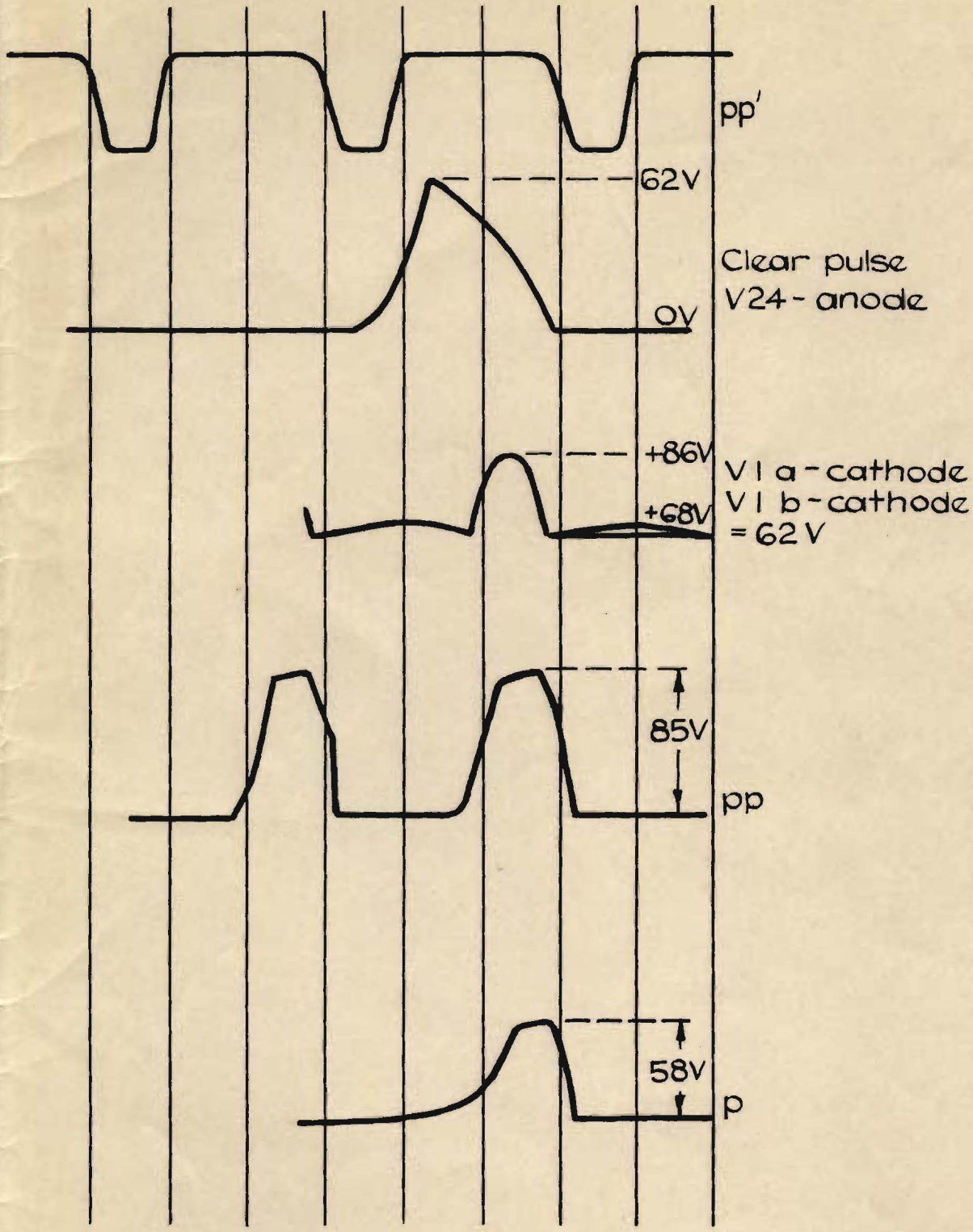
Measurements taken with Unit operating. 26/10/54

Nominal 210 - 206

Nominal -60V - -62

VOLTS

V1(a) cathode	base level	- 68
V1(b) cathode	"	- 62



CHAIN UNIT WAVEFORMS

SECTION E

SEQUENCE UNIT MK II

Circuit: B21238

Block Schematic: C21354

Waveforms: C21221

1. Normal Operation
2. Start and Stop Inputs
3. Speed-up Operation
4. Testing
5. Voltage Measurements
6. Delay Line Adjustments
7. Output Amplitudes.

1. NORMAL OPERATION

1.1 Two modes of operation are possible viz. "NORMAL" and "SPEED-UP". The NORMAL operation will be considered first. In this case P13-2 is disconnected from the Time Selector Unit. The output waveforms are shown in Fig. SU-1.

1.2 To start the Sequence Unit RY1 is closed. The first C pulse triggers V11 which opens the 4 gate G1 and allows the next C pulse via D47 to produce P2-7 via amplifier V36 and V44.

The output pulse from V36 triggers the flip-flop V13 which closes the 4 gate G1 for 3½ major cycles. The next C pulse starts the operation again thus one P2-7 pulse is produced every 4 major cycles.

V13 .... Fig. SU-1(a)

P2-7 .... Fig. SU-1(b), Photograph 16

(a) When the S.U. start switch is initially in the off position the flip-flop V12 is set-up. This flip-flop remains set-up when the switch is changed to "on" and D46 then allows the 4 gate G1 to be opened as above.

(b) V13 is a self-setting flip-flop but for the speed-up operation is restored by a pulse via D18.

1.3 The output pulse from V36 also triggers the flip-flop V14. This flip-flop is restored by the next p pulse via D21. The output of V14, P2-1, is thus of one minor cycle duration.

P2-1 .... Fig. SU-1(c)

Start of P2-1 .... Photograph 24

Finish of P2-1 .... Photograph 25

(a) The p pulses appearing at the output of V4(a) are delayed from the clock p pulses. In addition the p pulse occurring

at the time of a C pulse is inhibited, V2(b), so that it does not interfere with the triggering of V14.

p pulses at V3 cathode .... Photographs 36, 39

1.4 At the end of the P2-1 period the output of V14 is differentiated and the pulse so formed fed into a delay circuit via V5(a). Via diodes D3, D4 and cathode follower V5(b) a pulse is formed coincident with a delayed p pulse. This pulse after inversion in V6(a) triggers the flip-flop V15.

P2-3 .... Fig. SU-1(d)

Trigger at V6(a) grid .... Photograph 42

Trigger at V6(a) plate .... Photograph 43

(a) The delay circuit operates as follows:-

The output from V14(a) plate is differentiated and the positive pulse obtained at the end of the P2-1 period is applied to V5(a) grid. This pulse discharges C1 through D3. C1 is normally charged to +60 V by p pulses fed through D4. C1 remains discharged until the next p pulse which occurs one minor cycle later. The voltage at D3 plate or V5 cathode is thus a negative pulse of one minor cycle length. This pulse is differentiated and the pulse formed from the back edge triggers V15.

1.5 The output of V15 is P2-3. P2-3 is applied to the 2 gate G2 which allows the next C pulse to trigger V16. The operation of V16 is the same as V14 i.e. the output is of one minor cycle duration. A trigger pulse for V17 is produced one minor cycle after the end of the V16 output and this pulse also restores V15 which has therefore an output of length one major cycle.

Output of V15 .... Fig. SU-1(d)

Output of V16 .... Fig. SU-1(e)

1.6 The above sequence of a minor cycle followed by a major cycle is continued through the flip-flops V17, V18, V19 and V20 to produce the waveforms shown in Figs. SU-1(f) to SU-1(j). These are used to produce the remainder of the waveforms required as shown in Figs. SU-1(k) to (p).

2. START AND STOP INPUTS

2.1 There is provision for stopping and restarting the sequence unit by means of pulses and also for inhibiting the add-one pulse P2-2.

2.2 A STOP pulse appearing at P19 restores the flip-flop V12 thus closing the gate G1 and stopping the sequence unit at the end of the current 4 major cycles.

2.3 A START pulse applied at P83 triggers the flip-flop V12 thus opening the gate G1 and allowing the next C pulse to restart the sequence unit.

(a) Provision is made in another unit to ensure that the start pulse cannot occur at the same time as a C pulse. A near coincidence of C and a start pulse could result in incorrect operation.

2.4 A STOP - ADD ONE pulse applied to P84 is used to inhibit the trigger pulse to V19. This results in no output from the sequence unit after the end of P2-6 and hence the inhibition of P2-2.

(a) This operation is required in connection with reading from the drum, tape reading, printing and punching.

3. SPEED-UP OPERATION

3.1 For the SPEED-UP operation a pulse from the Time Selector is fed to P13-2.

P13-2 .... Fig. SU-2(1)

3.2 A pulse on P13-2 restores V15 before the end of the normal 1 major cycle period as shown in Figs. SU-2(d) and (1). The P13-2 pulse also triggers V17 via a gate G3. This gate is closed after V15 is restored and prevents retriggering of V17 during the second half of the operation.

3.3 The triggering of V17 opens the gate G4 and allows V18 to be triggered by the next C pulse.

3.4 If a second pulse is received at P13-2, the flip-flop V19 is restored, Fig. SU-2(h). V13 is also restored ready to start the sequence again.

3.5 Fig. SU-2 shows the operation with speed-up occurring twice in the full cycle followed by a normal operation. In the last cycle shown the P13-2 pulse is coincident with a C pulse. The pulse restores V19 and V13 but does not shorten the operating time as V13 is not triggered again until after a further major cycle.

Effective speeding up does not occur for the last 3 time positions of the major cycle intervals.

4. TESTING

4.1 For initial tests it is preferable to remove the speed-up pulse (by means of switch on Time Selector Unit) and also break the connection A-A. The operation of the chain of flip-flops V11 - V20 may then be checked in turn by noting the outputs at the P2 terminals or at the flip-flop plates

when these are not connected to output terminals. Since each flip-flop depends upon the preceding one for its trigger pulse a fault may be easily localised.

4.2 Routine tests should include the following:-

(a) Check natural length of flip-flop V13 i.e. with link A-A broken. The length must be >3 and <4 major cycles and is adjusted initially to $\simeq 3\frac{1}{2}$ major cycles.

(b) Check cathode voltages at the 4 gate G1 i.e. cathodes of diodes D44, 45, 46 and 47. These should be equal to within ± 2 volts say.

(c) Check D.C. voltages from dividers i.e. 120 V, 60 V, 20 V and -20 V.

(d) Check D.C. levels at grids of 6V6GT output cathode followers. These were set initially to 0 V.

(e) Check flip-flop voltages and trigger pulses.

(f) Check delay line adjustments according to details given in section F.

5. VOLTAGE MEASUREMENTS

The following readings were taken 6/5/52, using R.P. Electronic Voltmeter (R.C.A. design).

D.C. Supplies Nominal Volts	R.P. Meter	Sub-standard Meter
+ 210 V	+ 213 V	+ 213 V
- 60 V	- 61 V	- 61 V
- 100 V	- 102 V	- 100 V
- 20 V	- 20 V	
+ 20 V	+ 20 V	
+ 60 V	+ 62 V	
+ 100 V	+ 100 V	

Tube No	Grid Volts	Cathode Volts	Remarks
D44		42	G1 gate. D44 cathode is normally up. Check reading is obtained with grid of V13(b) connected to -60 V.
D45		39	
D46		44	
D47		38	
V32	6	21	These grids should be 0 ± 5 volts.
V33	6	26	
V38	-6	18	
V39	-6	19	
V41	7·5	23	
V43	-4	18	
V21	91	100	
V22		20·5	
V24(b)	30	38	
V25(a)	125	125	

Tube No	Grid Volts	Cathode Volts	Remarks
V27	G3, - 13		Check that there is no break through at plate
V28	G3, - 19		
V29	7·5	26	
V31	G3, - 32		
V34		14	
V35(a)	34	39	
V36		27	
V40		23	
V42(a)		10	
V42(b)	12	12	

FLIP-FLOP VOLTAGES

Tube	G1	A1	K	G2	A2
V11	41	48	38	-59	160
V12	-52	152	36	39	55
V13	-20	182	-3	- 3	94
V14	-20	213	0	3	88
V15	-19	198	0	0·5	92
V16	-21	213	0·5	1·0	92
V17	-19	213	- 1·0	0·0	76
V18	-21	213	0·5	1·0	97
V19	-19	213	- 0·5	0·0	72
V20	-21	213	0	1·0	98
V12*	+17	142	37	39	63

* 3/12/53 Unit running. 210 H.T. = 205.

6. DELAY LINE ADJUSTMENTS

6.1 Delay Line DL1 is required to provide co-incidence of the p and C pulses at the inhibitor V2. No adjustment should be necessary.

6.2 Delay Line DL2. The position of the tap (a) determines the position of the start and finish of P2-3, P2-5 and P2-9.

P2-3 start .... Photograph 31

P2-3 finish .... Photograph 32

P2-5 start .... Photograph 33

P2-5 finish .... Photograph 34

P2-9 .... Photograph 35

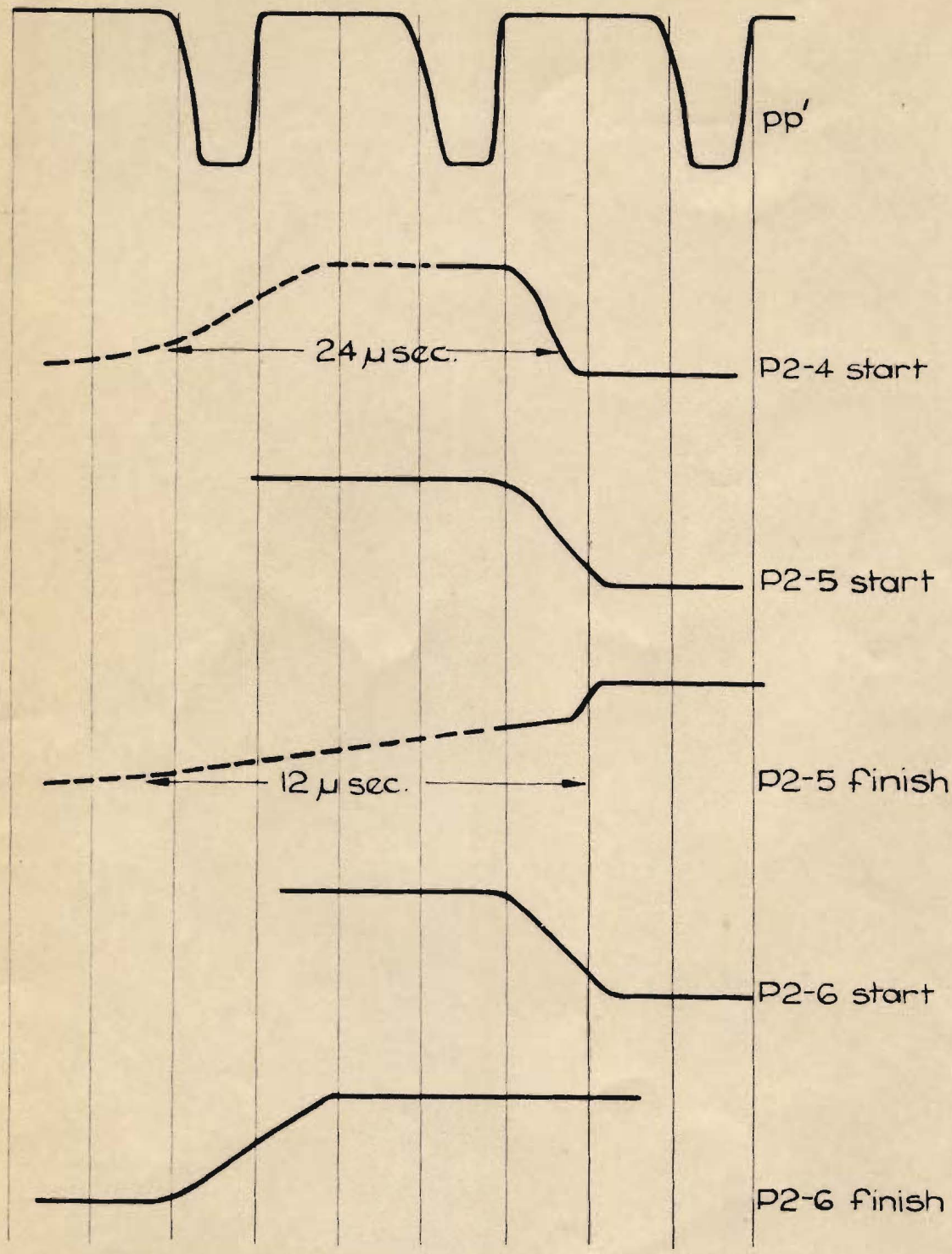
Variations of the position of P2-5 may effect the Time Selector due to mis-alignment of the p pulses and P2-5 inhibition pulse. Such mis-alignment should be corrected by adjusting the tap (a) on DL2, not by adjusting the time selector line.

The position of tap (b) determines the end of P2-1, P2-6 and P2-8.

P2-1 finish .... Photograph 25

P2-6 finish .... Photograph 28

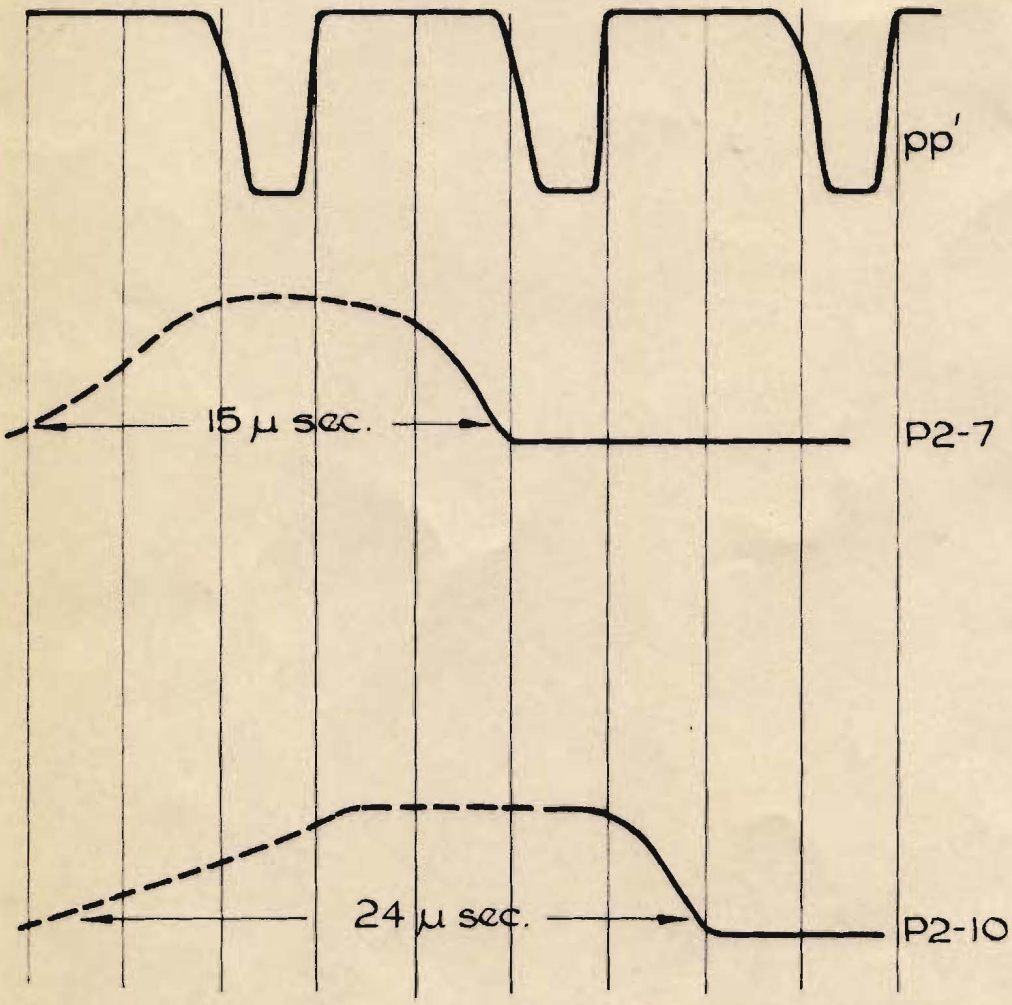
6.3 Delay Line DL3. The delay to tap (b) is required to delay the triggering of V11 and hence the opening of gate G1. This delay prevents the trigger pulse itself being gated by G1. No adjustment should be necessary.



MK II SEQUENCE UNIT WAVEFORMS
18·10·54

FIG. 1 (b)

R.P.L. 99



MKII SEQUENCE UNIT WAVEFORMS
18·10·54

FIG. 1 (c)

R.P.L. 99

SECTION K

TIME SELECTOR AND TRANSFER CONTROL UNIT MK II

Circuit: B22983

1. Circuit Description
2. Testing
3. Voltages.

1. CIRCUIT DESCRIPTION

1.1 Input pulses enter on P5A and set up the flip-flops V19-V23 via the 2 gate D4, D5 and trigger tubes V8 - V11.

(a) The flip-flops are connected as a binary counter and have been initially set to zero by the clearing pulse P2-4. This pulse is amplified and lengthened by V24, D25 and V6 and fed to the grids of the flip-flops.

1.2 During the periods of the P2-5 sequence unit pulse p pulses are counted into the flip-flop chain V20 - V23 via V (b), the 2 gate, D2, D3 and inverter V19.

1.3 The waveforms at the flip-flop plates A, B, C and D are shown in Photographs 75- 78. During one minor cycle period the four plates are all at a high voltage and allow the 5 gate D19 - 23 to open. P2-5 is applied to the fifth diode via V17.

(a) The actual minor cycle period during which the 5 gate is opened depends on the initial number set up on the flip-flops.

(b) The P2-5 pulse is required to prevent the flip-flops opening the gate outside the P2-5 period. This could occur if the initial number fed to the flip-flops set them up with the four plates A - D in the "up" position.

1.4 The minor cycle pulse output from the 5 gate is amplified and fed to the transfer control trunk P13 via V5, V4 and the cathode followers V15, V16.

1.5 The transfer control unit which feeds pulses from P6 to P5 during the P13 period consists of the 2 gate D12, D18, amplifier V3, V2 and cathode followers V13, V14.

1.6 A speed-up pulse is sent to the Sequence Unit via P13-2 unless inhibited by a pulse on P91 when multiplication is called.

2. TESTING

Routine tests should be made as follows:-

2.1 Check supply and divider voltages.

2.2 Check cathode voltages at 5 gate. This requires V20, V21 and V23 to be in the cleared position, V22 in the "on" position, and the sequence unit to be stopped.

2.3 Check p pulses at plate of V19. There should not be any breakthrough of a p pulse in the c pulse position.

3. VOLTAGE MEASUREMENTS 6/5/52

3.1 Supply volts

Nominal	Measured
210 V	212 V
100 V	110 V
70 V	68 V
50 V	50 V
30 V	30 V
-20 V	-22 V
-100 V	
-250 V	-246 V

3.2 Valve Voltages

Valve No.	Grid	Plate	Cathode	Screen	Design Values
D4			26		equal to ± 2 V
D5			26		
D2			36		equal to ± 2 V
D3			36		
V6			-94		-100 ± 5 V
V7	126		130		

Valve No.	Grid	Plate	Cathode	Screen	Design Values
V2		115	26	74	
V4		33	19·5	98	
V13			16·5		
D17			24		equal to ± 2 V
D18			19·5		
D19			98		equal to ± 2 V
D20			98		
D21			100		
D22			98		
D23			98		
V17		98	64		
V25(a)			69		
V26(b)		212			

3.3 Flip-flop Voltages

Voltages measured with flip-flops in cleared position.

Valve	Grid 1	Plate 1	Cathode	Grid 2	Plate 2
V20	60	98	57	36	180-21
V21	57	98	55	37	180-18
V22	60	100	57	40	180-17
V23	59	98	56	37	178-19

SECTION L

LINE CODE REGISTER AND LINE SELECTOR

Register Circuit: B22583

Line Selector Circuit: B23751

Register Valve Layout: SKE5554

Selector Valve Layout: SKE5537

LINE CODE REGISTER

1 The Register consists of 6 standard flip-flops and read-in gates.

2 The Register is cleared by means of P2-4 pulses applied via a cathode follower to the grids of the flip-flops.

LINE SELECTOR

1 The Selector is similar to Source Selector except that there are two trees, the lower one (valves V17-V24) connected to three flip-flops of the Register and the one on the left (valves V60, 61 etc.) connected to two flip-flops.

2 Note that the terminals A-L are connected to the flip-flop plates and hence anypart i.e. AB, CD, EF, etc. must have one terminal up and the other down.

3 For any given number fed into the unit one plate only of the valves V17, V19, V21, V23 and one plate only of valves V51, V63 will be down.

It can then be seen that this will mean the cut off of one only output triode.

4 Valve V56 is no longer used.

5 Valves V57, V64 are used to drive the interspacing gate in the memory read in unit.

6 Voltage measurements.

Normally the line code register is cleared by a P2-4 pulse. In order to measure the flip-flop voltages with "1"s in the register the P2-4 pulse is removed. i.e. first of all put N1 to K switch on "one shot", read in zeros and measure voltages on the terminal points A, B, C etc. Then remove P2-4 and read in "1"s to all positions.

VOLTAGES

Terminal	"0"	"1"
A	108	13
B	18	103
C	63	41
D	44	52
E	62	43
F	40	49
G	27	105
H	106	23
I	110	19
J	23	106
K	-47	-19
L	-35	-56
V20 - k	-32	-18
V24 - k	-36	-33
V18 - k	63	47
V22 - k	59	50
V17 - k	68	58
V19 - k	68	49
V21 - k	61	57
V23 - k	68	57

210V Nominal
= 206 Volts

The above readings indicate an undesirable unbalance in the circuit. The inputs to the tree have been unbalanced also so it is proposed to overhaul the components as soon as an opportunity arises.

The table below shows the present grid-cathode voltages.

Valve	"0"		"1"	
V20	-15	-3	-38	-1
V18	-23	-1	- 4	+2
V22	-19	+3	- 7	-1
V17	-24	-5	-17	-6
V19	-24	-5	- 8	+3
V21	-17	+2	-16	-5
V23	-22	-5	-16	-5

The values underlined should all be positive 2 or 3 volts.

SECTION M

SOURCE AND DESTINATION SELECTOR

Circuit: B22584

Plug and Valve Layout: C22575.

1 The selector is shown in partly schematic form in Fig. 19 of RPR 117. Refer also to page 16 of same report.

2 The inputs to the selector are connected directly to the flip-flops of the Interpreter Unit via plug P3 and P4.

3 P2-3 is applied to V37 so that the output is inhibited during this period.

4 Source Selector Voltage Measurements. Set operation switch to N1—Int. and with the required number on N1 do a one shot to set up the Interpreter.

210 Nominal H.T. = 206

-100 " " = -100

	V35g		V34g		V32g		V18g		V17	
Number in Source	1	2	1	2	1	2	1	2	1	2
00000	-21	-2	-27	-61	-86	-49	24	83	96	21
00001					-51	-63				
00010			-61	-25						
00100	+2	-26								
01000							83	28		
10000									25	88

V37-c = -102 V37-g = -108

5 Destination Selector Voltage Measurements

	V35g		V34g		V32g		V18g		V17g	
Number in Source	1	2	1	2	1	2	1	2	1	2
00000	?	-32	-68	-37	-76	-51	35	92	99	34

	V35g		V34g		V32g		V18g		V17g	
00001					51	-67				
00010			-36	-68						
00100	-2	?								
01000							84	30		
10000									30	102

V37-e = -102 V37-g = -110.

SECTION N

TAPE READER, INPUT CONTROL AND INPUT REGISTER

Tape Reader Control Circuit: SKE5188

Input Register: SKE5187

Tape Reader Control Logical Schematic: SKE5186

1. Input Equipment
2. The Tape Reader
3. Photo-cell Amplifier
4. Tape Reader Control
5. Input Register.

SECTION N

TAPE READER, INPUT CONTROL AND INPUT REGISTER

1. INPUT EQUIPMENT

A block diagram of the input units is shown in Fig. 1. It consists of a tape reader, photocell amplifier, tape reader control circuits and the input register.

Paper tape $2\frac{3}{8}$ in. wide can be punched with holes in any of 14 positions, 10 of which represent part of a number or command; 2 positions are used to denote special functions to be performed by the computer on the incoming data and 2 are not used. The tape is read by the photo-electric tape reader which is under the control of the tape reader control unit. The photo-cell amplifier amplifies the photo-cell output and delivers the information to the input register. The computer takes the information from the input register whenever input source is called, provided that the operation of reading off the tape has been completed.

2. THE TAPE READER

2.1. Description and operation

The tape reader consists of a light source and a photo-cell, separated by the paper tape which has various configurations of holes punched in rows across its surface (Fig. 2). The

light system also includes a rotating drum shutter with slots placed on a spiral line about its surface. The slots in the shutter allow light to strike the photocell from each of the tape holes in turn, thus producing at the output of the photo-cell a train of pulses with a configuration which depends upon the holes in the tape. (Fig. 3).

A pulse generator is on the end of the shutter shaft and produces timing pulses (Fig. 4) which, after amplifying, are used to gate the output of the photo-cell amp. into different flip-flop registers.

The pulse generator consists of a rotating magnet which induces a voltage in coils situated upon pole pieces distributed around the circumference of the stator in the same angular positions as the spiral holes on the rotating drum shutter. The small generated pulses are amplified before being applied to a gate.

A $\frac{1}{3}$ H.P.,D.C. motor drives the rotating shutter and pulse generator at 3,000 R.P.M.; it also drives a geneva movement through a reduction gear to 100 R.P.M. and a slipping clutch. An electro-magnet prevents the geneva movement from turning until it receives a pulse from the control unit. When this occurs the clutch moves the shaft 90° and turns a sprocket which moves the tape along to the next row.

The magnet operates in approx. 20 m. seconds and the tape is moved to the next row in 150 m. seconds. The fact that this operation has been completed is indicated to the control unit by the closing of a contact which is actuated by a cam

on the geneva movement shaft.

3.2. Maintenance

The mechanical parts of the tape-reader should be kept oiled using Essolube 20.

The photo-cell should be removed and cleaned at 6-monthly intervals. Dust accumulates and lowers the light transmission. To reach the photo-cell remove the four 2 B.A. screws which hold the unit to its base, swing it to one side and undo the two 5 B.A. screws which hold the photo-cell onto the tape support. The support may then be removed.

The timing of the pulse generator can be varied by adjusting the two vertical 2 B.A. screws on the front of the reader after the locknuts have been loosened. The angular position of the pole pieces is critical and should not need to be altered. When resetting this adjustment the time relationship of the pulse generator pulses and the photo-cell amp. output should be observed on a C.R.O., which may be triggered from the plate of V8(a) in the tape-reader control unit. It may be necessary to use the C.R.O. amplifier unit to amplify the pulse on V8(a) anode in order to obtain a pulse with a sufficiently short rise time. -20 volts (or more) should be applied to P113-1 of the amplifier as otherwise the pulses from the amplifier are inhibited.

Fig. 5 shows the pulses observed on the grids of the 6SA7 gating tubes V23-V29. The G1 pulse (amplifier output) should be observed on the input side of the grid resistor. The

coil-pulse generator pulses vary in width and amplitude, but the phasing is correct when the widest coil pulse is central with respect to the adjacent amplifier pulses. The smaller coil pulses may then appear slightly early or late but coincide sufficiently to produce a trigger pulse to the flip-flop. The coils may be examined by removing the circular end plate which holds the bearing for the shutter shaft. The contact should be set in the position shown in Fig. 3; on no account should the reader be turned backwards as this will bend the contact rods.

The magnet position should be adjusted as shown in Fig. 7. Adjustment of the lamp position may be done with the cover off, by observing the output of the photo-cell amplifier on a C.R.O. as the lamp is twisted.

3. PHOTO-CELL AMPLIFIER

3.1. Description and operation

This amplifier (Fig. 11) accepts milli. volt +ve pulses 350 μ secs long from the photo-cell, amplifies them to 74 volts, (peak to peak), then lets them appear at the output P111 when the inhibiting pulse P113-1 is removed.

The effective gain is controlled by varying the negative bias on V3. Diode D2 clips the output of V4 to a constant amplitude and the series combination 60 k and 0·1 μf counteracts the droop in pulse amplitude which occurs due to the finite time constant of the clipping diodes H.T. supply. This +90V

H.T. is taken from a D.C. cathode follower, V5(b).

The plates of V4 are held down by the positive voltage on grid V4(b) and the negative pulses on V4(a) grid produce no output on V4(a) plate until P113-1 goes negative to greater than -12V and allows the plates of V4 to rise.

V5(a) is a cathode follower output for the amplifier. D1 and D3 are D.C. restorers.

Fig. 6 shows the waveform on the grid of V3 with the bias increased to prevent the pulses being limited.

3.2. Maintenance

The bias of V3 should be adjusted so that it is midway between the position where holes on the tape are missed and the position where one hole tends to produce an output wide enough to set up two flip-flops in the input register instead of one. This adjustment is done while the test tapes are being run on the tape-reader. A typical range of voltage is 10V to 20V.

Voltages at different points in the circuit as measured on an electronic voltmeter are listed below. There was no output from the photo-cell.

R.P. ELECTRONIC VOLTMETER. 210V H.T. reads 208V

Valve	Plate	Screen	Cathode
V1	163 Volts	103 Volts	2·2 Volts
V2	23 Volts	98 Volts	0
V3		46* Volts	0
V4	90+ Volts		
V5(a)	208 Volts		10 Volts
V5(b)	208 Volts		92 Volts

* Variable from 46V to 162 Volts.

+ With Ga = 0, Gb = -40V.

4. TAPE-READER CONTROL

4.1. Description and operation

The tape-reader control operates in either of two modes. Case A is when the tape reader is ready to operate when source input is called by the computer.

Case B is when the tape-reader is not ready to operate, i.e. it is in the process of moving the tape along to the next row. The fact that the tape has been moved is indicated to the control unit by a contact which produces a pulse on P110-2.

Case A. Tape-reader ready. SKE 5565 for waveforms and SKE 5186 for logical diagram.

Flip-flop V22 has been cleared by contact P110-2 and gate C is closed. When P3-3 input source pulse rises it opens gate A and, after the transfer from the input register has taken place, allows P2-10 from the sequence unit to trigger V14 and V22 flip-flops. V14 opens gate B. The first P110-1-18 generator pulse passes through gate B and triggers V3 which produces a wide pulse P113-1 that removes the inhibition on the photo-cell amplifier output, thus allowing the input register to be set up. The input register had just been cleared by the rise of V3, a pulse called P113-2, at the end of read out.

The rise of V3 triggers V4 which generates a pulse P113-3 $\propto$ 20 m. secs long which operates the controlling magnet in the tape-reader clutch.

When the new transfer from photo-cell amplifier to

input register is complete P110-1-15 chain pulse clears V3 which then clears V14.

N.B. V12 and associated gate D are not used in Case A operation.

Case B. Tape-reader not ready. Flip-flop V22 has been set up by a previous read (see SKE 5565).

Gate C is open when the source pulse P3-3 rises and the differentiated rise triggers V12 flip-flop. The differentiated rise of V12 produces P19 stop pulse which stops the sequence unit. P84 stop add-one is also produced by V12. This P84 keeps the computer on the same instruction, i.e. (Input $\rightarrow$ (x)).

The first P110-1-15 pulse passes through gate D and is used as P83 to start the sequence unit.

A series of P19, P84 and P83 pulses is produced until the contact P110-2 clears V22 and closes gate C.

The first input source pulse P3-3 reads the content of the input register which was set up by a previous tape-read operation. It also gates a P2-10 pulse via gate A which triggers V14 and resets V22. The operation from this point onwards is the same as Case A.

Points to note.

(1) Tape chain pulses are approx. $\frac{1}{3}$ millisecond long, the time from P110-1-18 to P110-1-16 is 6 milliseconds and from P110-1-18 to the next P110-1-18 is 20 milliseconds.

(2) The magnet pulse is $\propto$ 20 milliseconds long.

(3) From the start of the magnet pulse until the close of

contact P110-2, i.e. the time required to move the tape to the next row is $\propto$ 150 milliseconds.

4.2. Detailed operation of circuit

See schematic SKE 5188.

One coil of the pulse-generator has one end connected to P110-1-15, the other to P110-1-16. Diodes D1 or D2 hold the positive going end of the coil at -6V so that a negative pulse can be produced at the other diode plate. D1 plate receives the first negative pulse followed immediately by the second negative pulse on D2 plate. These negative pulses are generated in the pulse-generator coil by the magnet sweeping across the coil's pole piece. The grids of V1 are normally held positive by the 500k resistor from H.T. to D1 plate. The negative pulses produce positive pulses 85V amplitude and 300 μ secs length on the plates of V1. Trigger C.R.O. from P2-10 with operation I$\rightarrow$Z. V2 is a cathode follower mixer; its output resets V3 flip-flop via diode D4. D3 prevents the positive reset pulse from rising above earth. Diodes D5 and D6 have a similar function in association with the triggering pulse from V10(b). The voltage rise of V3(a) plate is differentiated by a 50 p.f. condenser and a 1 Meg. resistor, and applied to the grid of V11(b) cathode follower. V11 (b) output is the pulse P113-2 which clears the input register. V3(b) plate is D.C. coupled to V11(a) cathode follower which provides the wide pulse P113-1 that removes the inhibition from the photo-cell amplifier output. The voltage rise on

V3(b) plate is differentiated and triggers flip-flop V14 via diode D22. This voltage rise also triggers self-setting flip-flop V4 via D7.

The positive 20 milliseconds pulse on V4(a) plate is D.C. coupled to cathode follower V5. V5 output drives the grid of V6 which has the clutch magnet coil in its plate circuit via P113-3(-11 and -12). Condensers 0·1 µf and 0·01 µf are across the magnet coil to reduce the inductive overswing.

V8(a) receives a pulse P110-1-18 from the chain pulse generator in a similar fashion to V1; and V8(b) is a cathode follower which drives D11 in the two-gate D11, D13.

V12 is a flip-flop triggered via D14 by a pulse from the two-gate D23, D24. Cathode follower V17(b) takes the load off the two gate.

The resetting pulse P2-1 operates via diode D17. Diodes D15 and D16 prevent the grids of V12 from rising above the cathode voltage.

Three outputs are taken from V12(b) plate; one is D.C. coupled to V18(a) which is a cathode follower driving the two-gate D26, D27. The second output is the differentiated rise of V12(b) plate voltage which produces the stop pulse P19 via cathode follower V17(a). The third output is D.C. connected to V20(a) cathode follower and produces the stop add-one pulse P84.

One output is taken from V12(a) plate; the differentiated rise of plate voltage produces a pulse P2-4 via cathode

follower V23. P2-4 clears the time selector.

When the tape-read switch is closed, P3-3 source input pulse is applied to the grid of V13(a) which is a cathode follower driving D18 in the two gate D18, D19. D19 is driven by V13(b) which has P2-10 pulse on its grid. The output of D18, D19 two gate triggers V14 flip-flop via diode D20. D21 prevents V14(a) grid voltage from rising above the cathode voltage.

The resetting pulse as described above comes from V3(b) plate via diode D22. V14(b) plate is D.C. coupled to cathode follower V10(a) which drives the diode D13 in the two gate D11, D13.

Flip-flop V22 is triggered by the output of two gate D18, D19 via the invertor V24(b) and diode D43. V22 is reset by the closing of the contact on the tape-reader which shorts point P110-2 to ground, thus producing a positive pulse which resets V22 via the trigger tube V24(a).

The grid of V15(a) is D.C. coupled to the plate of flip-flop V22, and V15(a) drives the diode D24 in the two gate D23, D24 via a network which delays the rise and fall of the voltage pulse applied to D24.

The tape-read switch connects P3-3 input source to V15(b) grid via a differentiating network 500 p.f. and 250 kΩ. V15(b) is a cathode follower driving D23 of the two gate D23, D24. This gate produces a pulse which triggers flip-flop V12 via V17(b) cathode follower. V19(a) cathode follower is

connected to the output of the two gate D26, D27 and produces the start pulse P83.

The combination D28, V22 and V23 is repeated fourteen times. D28 and D29 are connected to opposite ends of a coil in the chain pulse generator. When P110-1-14 goes negative V22 produces a positive pulse on its cathode which is applied to the suppressor grid of V23. Whenever this pulse and the output of the photocell amplifier which is applied to the grid control of V23 are coincident, a negative pulse appears on the plate which triggers the appropriate flip-flop in the input register.

V50 is a cathode follower which drives the fourteen control grids of V23-V49. Its grid receives the output of the photocell amplifier P111 and also goes to -80 Volts so that V50 cathode will be below the cut-off potential of V23 - V49 control grids.

4.3. Maintenance

The complete system of tape-reader and control should be run whilst the H.T. is varied by ±5 per cent; the flip-flops and amplifier should operate over this range. The grids of cathode followers driving gates should be checked.

It is possible for one of the flip-flops to be set up wrongly when the H.T. is first switched on; this is corrected by manually releasing the clutch on the tape-reader so that it moves through one operating cycle. A bad fault which occurred in the past was a poor contact on the relay which switches

P3-3 source pulse. This caused occasional wrong reading.

5. INPUT REGISTER

5.1. Description and operation

The input register consists of flip-flops and gates which allow information to be set up in the register or which allow the register content to be read out by the computor.

5.2. Detailed operation of circuit

Flip-flop V1 which corresponds to a P10 digit, is set up by the coincidence trigger tube V23 in the tape-reader control, whose plate is connected to the plate of V1(b) via P113-4. This only occurs when there is a hole on the tape corresponding to the P10 digit position.

Immediately prior to a reading operation from the tape-reader, all the flip-flops V1 - V14 are cleared by P113-2 which is amplified in the cathode coupled amplifier V36 and applied to the grid of cathode follower V37. The cathode of V37 is connected to the bottom of the grid divider on one side of each flip-flop, and all these grids are sent positive when the positive pulse appears on V36 plate; the correct D.C. potential on the cathode of V37 is maintained by returning the grid resistor to -125 Volts.

The plate of flip-flop V1(a) is D.C. coupled to the grid of cathode follower V15(a); when V1(a) plate is high V15(a) cathode rises from - Volts to + Volts, and hence removes the bias from V15(b), allowing the chain pulse P15-20 to appear

on its cathode.

The cathodes of V15(b) - V34(b) are in parallel and drive diode D21 of the three gate D21, D22, D23. D22 is driven by V38(b) cathode follower which has P3-3 input source pulse on its grid. D23 diode is driven by V38(a) cathode follower which has clock pulses P1 on its grid. The output of this three gate is amplified by V39 and V40 cathode coupled amplifier then applied to the grid of cathode follower V41 which drives the output trunk P6.

D24 and D25 are D.C. restorers. V35 is a D.C. cathode follower which maintains the cathodes of V15(b) - V34(b) at the correct potential when these tubes are not conducting. The grids of V15(a) - V34(a) can be switched to the conducting region by switches P80-1 on the control panel as well as by the flip-flops.

When the input is not being derived from the tape-reader, the tape-read switch allows the clearing of the flip-flops to be accomplished by the differentiated start of P3-3 input source pulse which is connected to V36(a) grid.

<u>Note:</u> In the input control unit P2-4 pulse is too close to the restart pulse P83 to allow the time selector to be cleared before new information is read into it by P2-1. This is partly owing to the long clearing pulse produced by the time selector clearing circuits. This prevents the operation I→M or I→D being carried out under all conditions and these are avoided by the programmers. I→C or to any register which does not involve time digits is satisfactory.

6. FAULT DATA

21.1.53.	P8 not switched on. Broken wire on switch panel.
	P20 and P1 read out together. Ch. 20 too long and wrong time.
29.1.53.	Pulses from input on P5 varied their position of start w.r.t.pp'. Chain pulses not correctly gating pp'. Position of pp w.r.t. pp'altered in clock.
10.2.53.	Breakthrough pulses due to 15Volt step on P3-3. Cut-off of V39, V40 increased by a 150k 2W to grid of V40.
12.2.53.	Breakthrough pulses due to step on P3-3 which only occurs when P3-4 is called.
16.4.53.	Double reading due to poor contact on commutator.
8.6.53.	When contact broke R.F. was picked up on pulse gen. output, causing spurious gating pulses.
8.6.53.	2nd P2-4 is not generated by tape reader control; hence can't read into any register with time positions.

17.6.53.	Tape misread - holes not aligned, shifted sprocket holes.
18.6.53.	Lamp blew.
19.6.53.	Motor erratic - take-up spring jumped out of place (Singer motor).
22.6.53.	P2-4 generated by diff. tail of P84.
26.6.53.	P2-4 pulse was clearing out some of the resetting pulses in time selector - occurring too close to P2-1.
2.7.53.	Stop flip-flop failing to trigger owing to 0·001 µf. cond. inst. of 0·01 from gate.
3.7.53.	Lamp blew.
7.7.53.	Clutch magnet 6V6 made a pentode.
24.8.53.	Tape-reader running free, owing to weak return spring on magnet.
10.9.53.	Failed to move on. Time constant on V10(b) grid was too small, put in a 0·01 µf. condenser.

30.9.53.	Tape-reader overhauled.
2.10.53.	Pin came out of magnet when running at double speed.
16.10.53.	Tape-reader motor relay failed to operate.
24.11.53.	Lamp blew.
20.1.54.	Missing P7 and P8, pulse generator coil had shorted turns. Fitted a new coil.
15.2.54.	Made shutter holes narrower to stop pulses from P.E. cell from running together.
18. 3.54.	Lamp blew.
1.4.54.	Loose pin in magnet assembly. Holding pin for return spring. Motor start relay coil O/C.
9.4.54.	P7 missed out. Weak pulse from new coil in pulse generator. Put in a transformer to increase size.

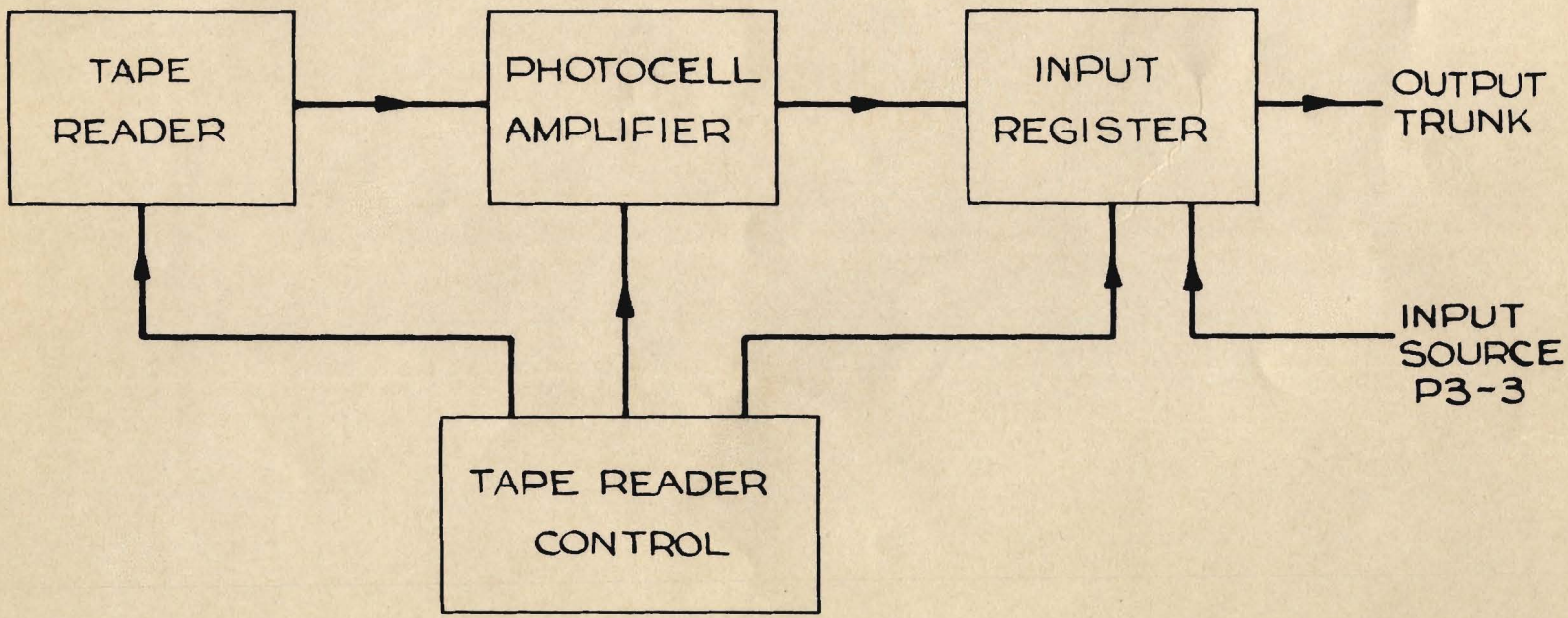
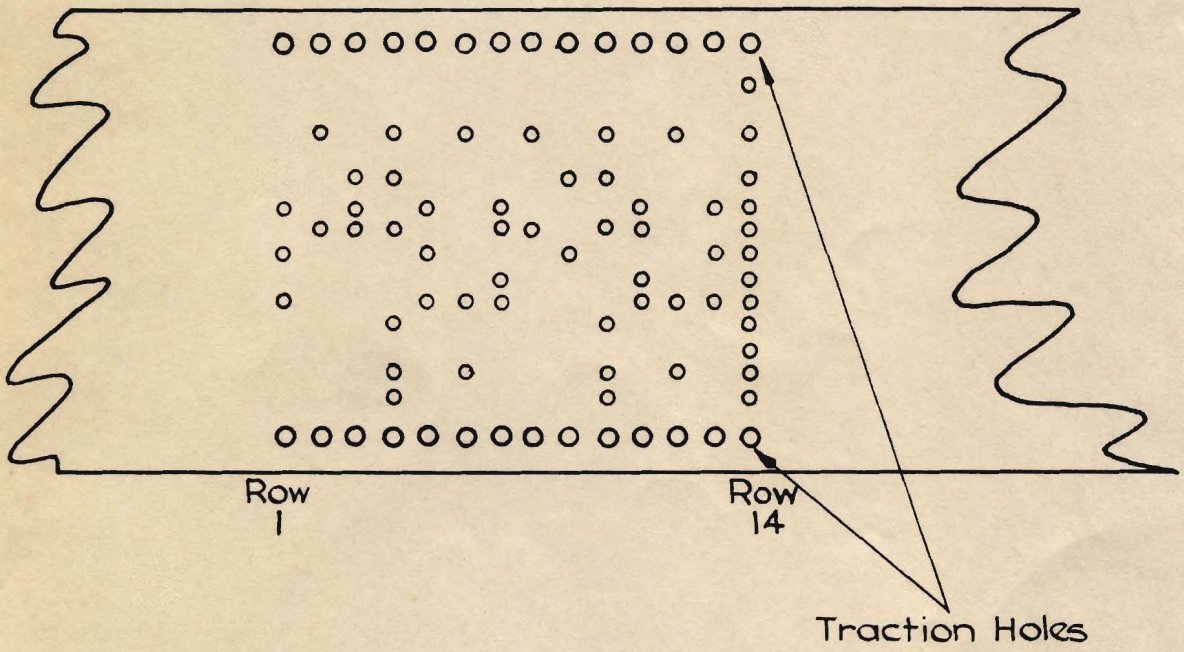

TAPE READER
PHOTOCELL AMPLIFIER
INPUT REGISTER
OUTPUT TRUNK
INPUT SOURCE P3-3
TAPE READER CONTROL

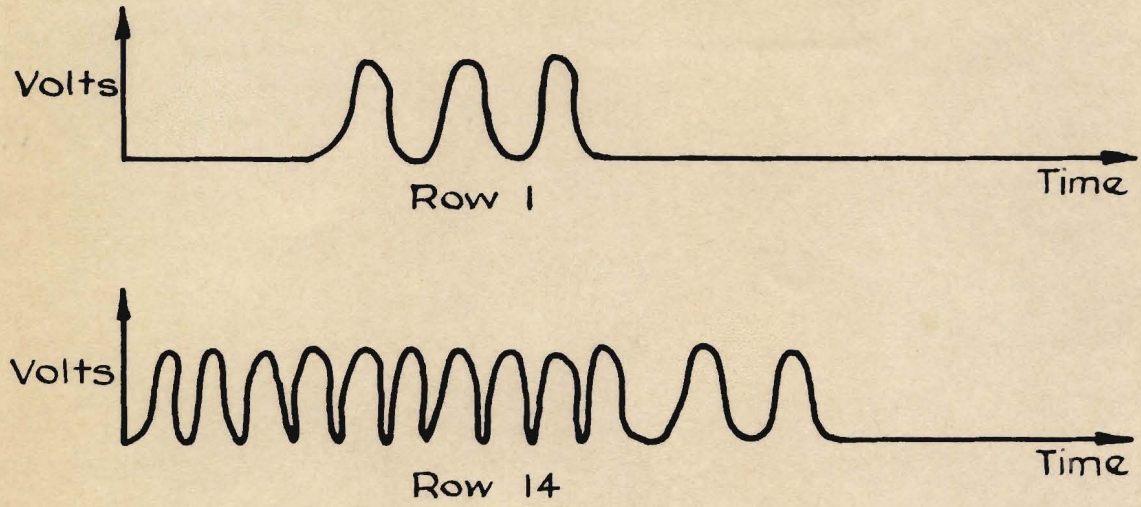
FIG. 1



TAPE

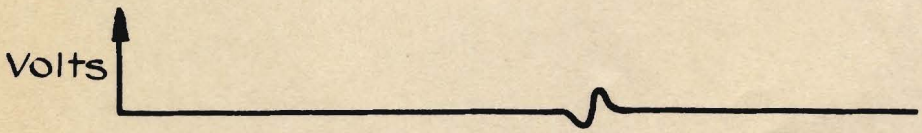
FIG. 2

R.P.L. 99



OUTPUT OF PHOTO-CELL

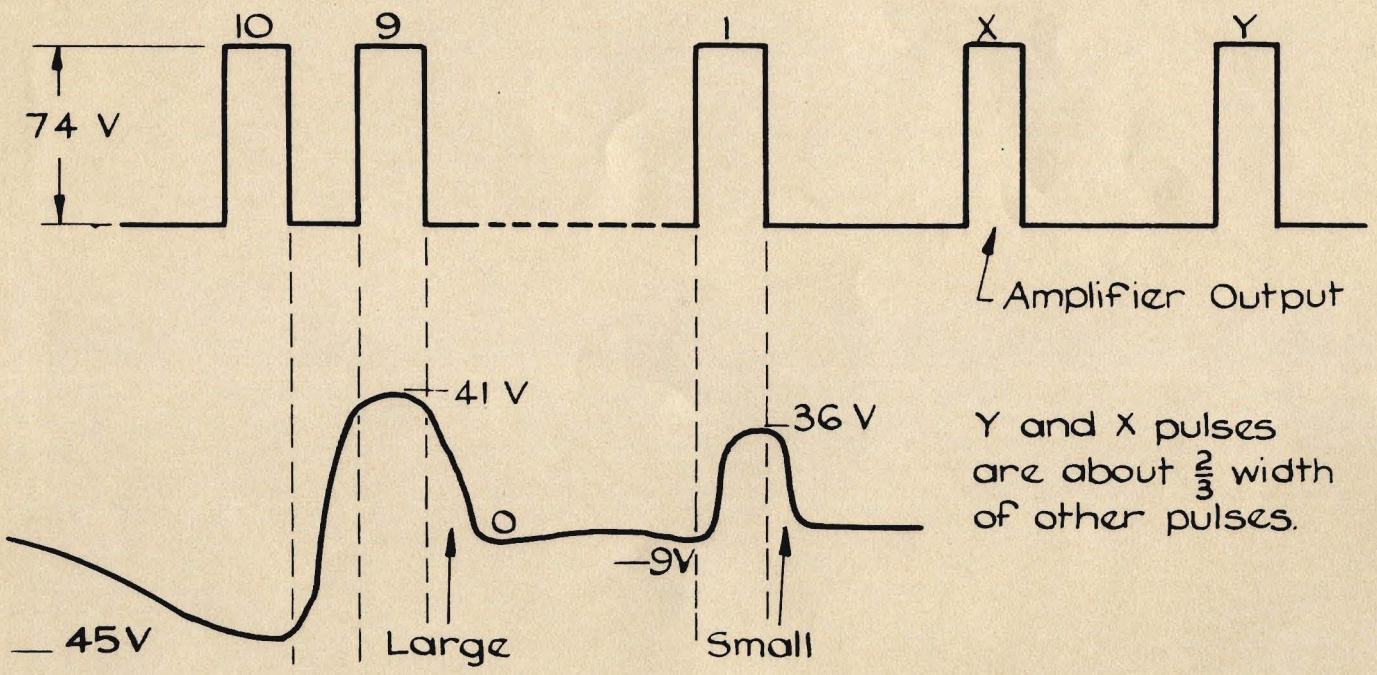
FIG. 3



OUTPUT OF COIL OF PULSE GENERATOR

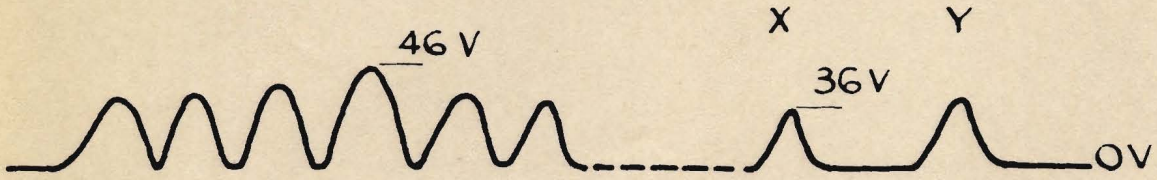
FIG. 4

R.P.L. 99



AMPLIFIED COIL PULSES

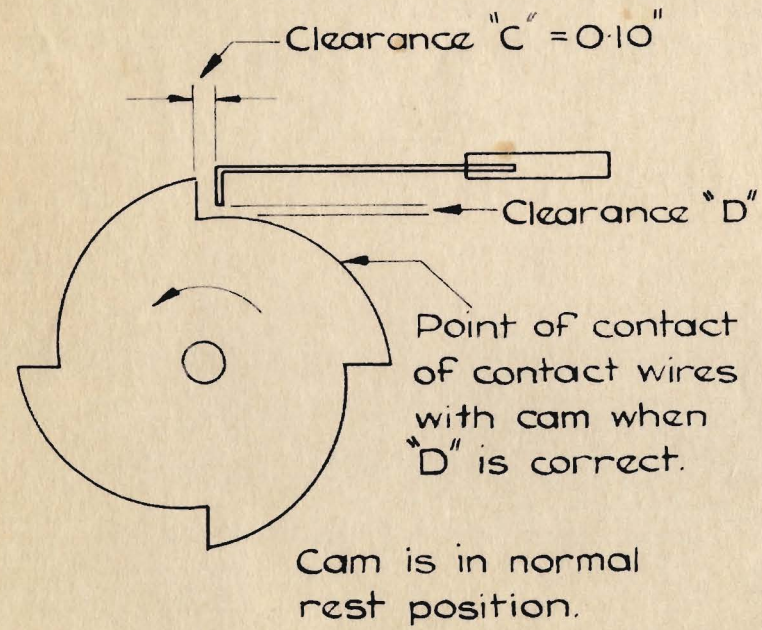
FIG. 5



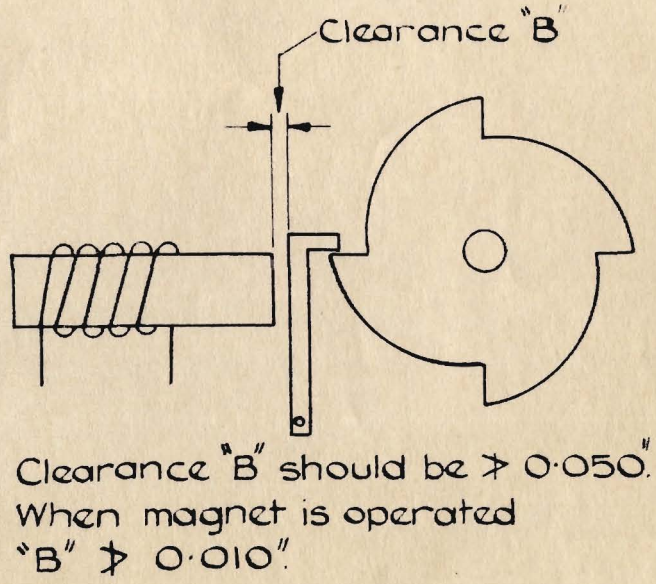
OUTPUT OF PHOTOCELL
AT GRID V3

FIG. 6

R.P.L. 99

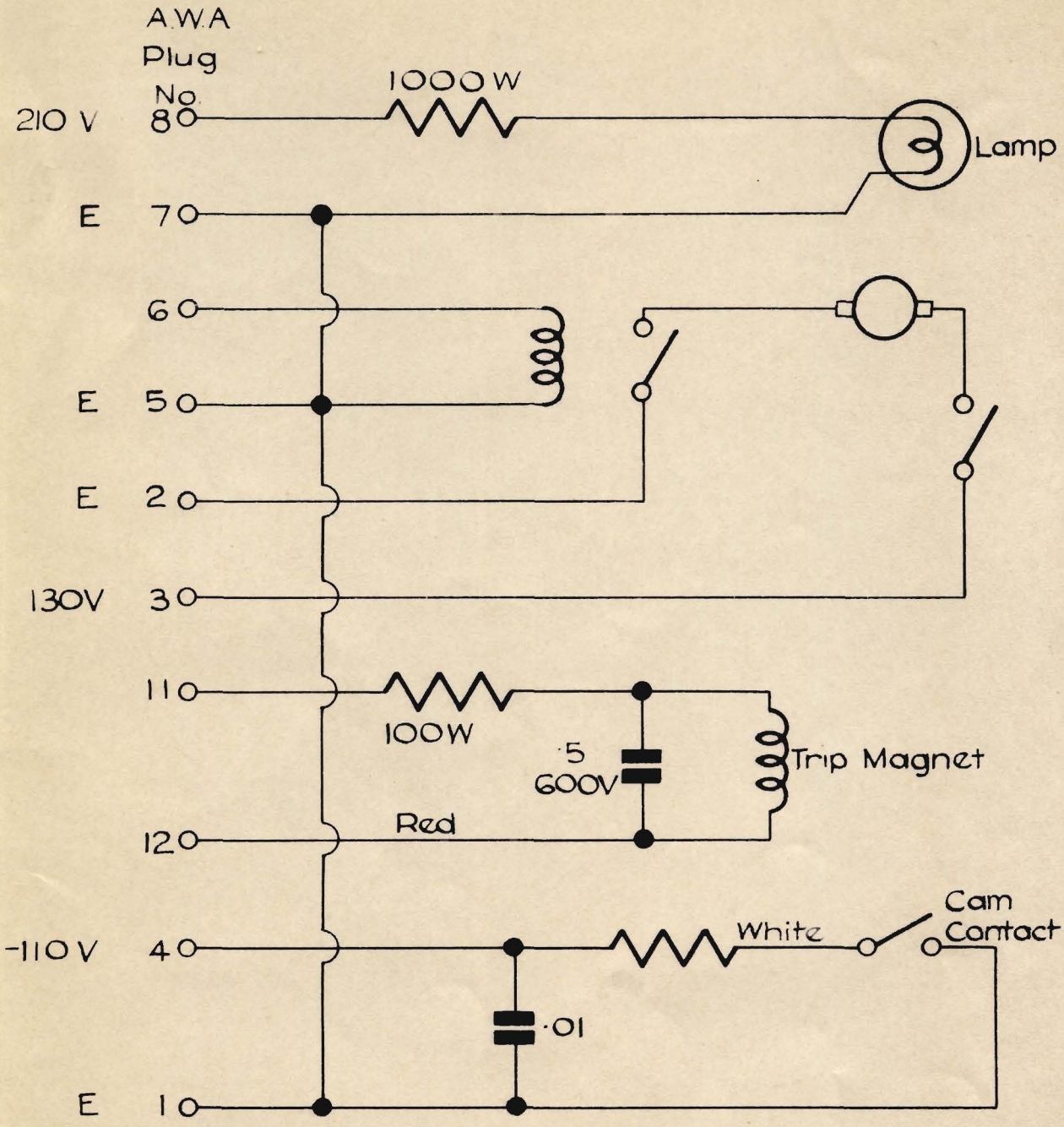


CAM



STOP PLATE

FIG. 7



TAPE READER CONNECTIONS

FIG. 8

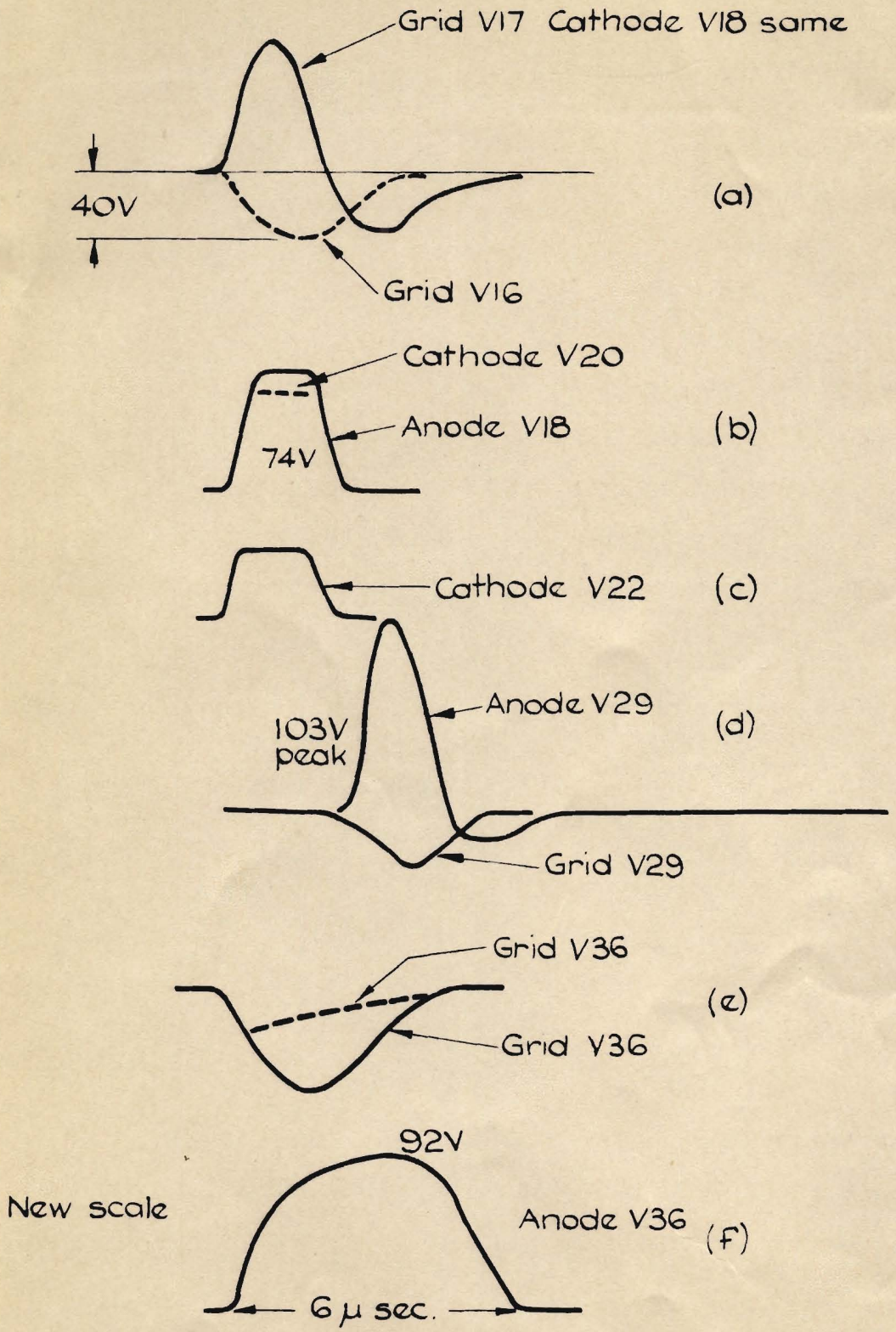

Grid V17 Cathode V18 same
40V
(a)
Grid V16
Cathode V20
Anode V18
(b)
74V
Cathode V22
(c)
Anode V29
103V
peak
(d)
Grid V29
Grid V36
(e)
Grid V36
92V
New scale
Anode V36
(f)
6 μ sec.

FIG. 1 (a-f)

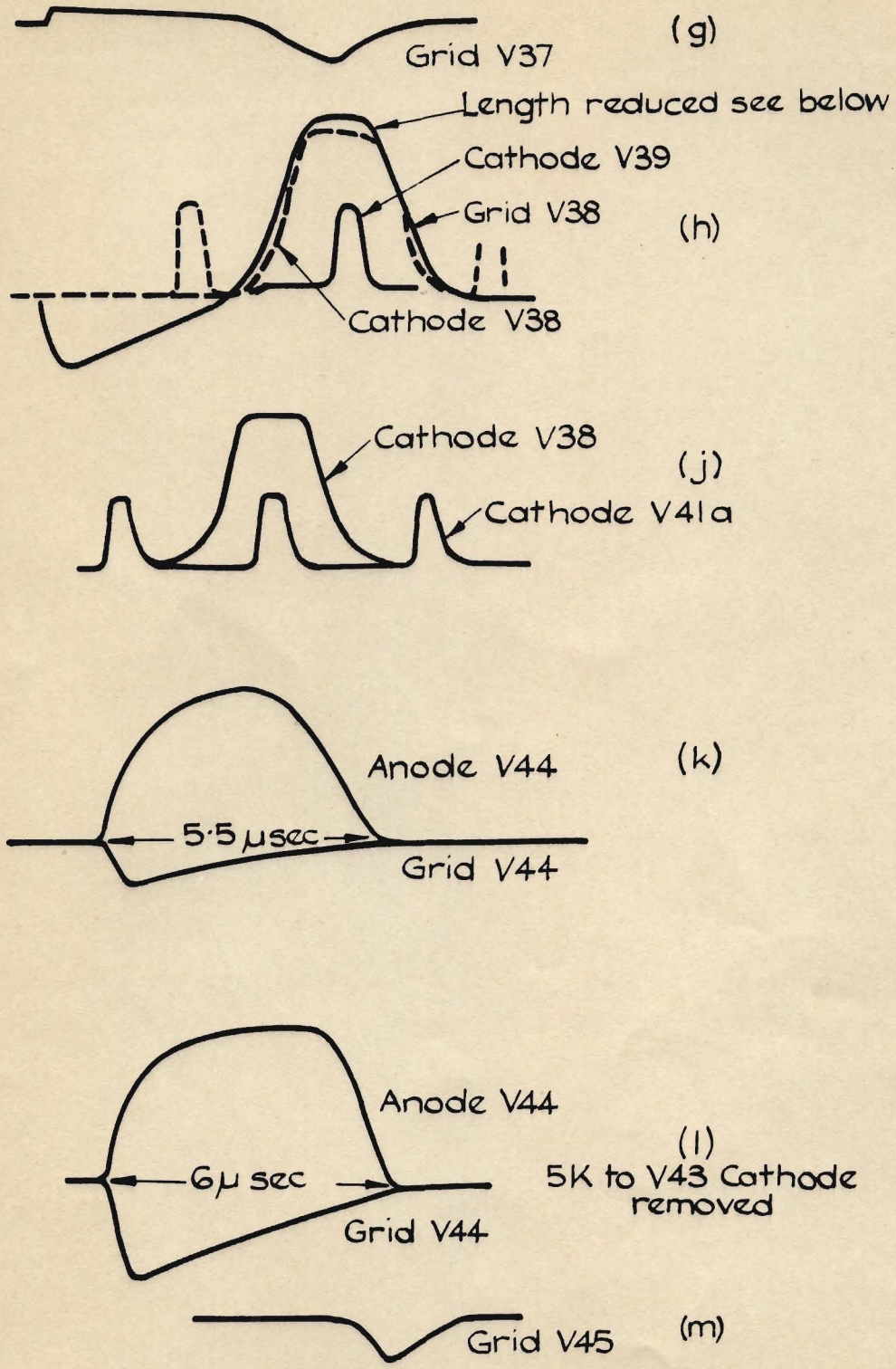

(g)
Grid V37
Length reduced see below
Cathode V39
Grid V38
(h)
Cathode V38
Cathode V38
(j)
Cathode V41a
Anode V44
(k)
5·5 μsec
Grid V44
Anode V44
(l)
6μ sec
5K to V43 Cathode removed
Grid V44
Grid V45
(m)

FIG. 1 (g-m)

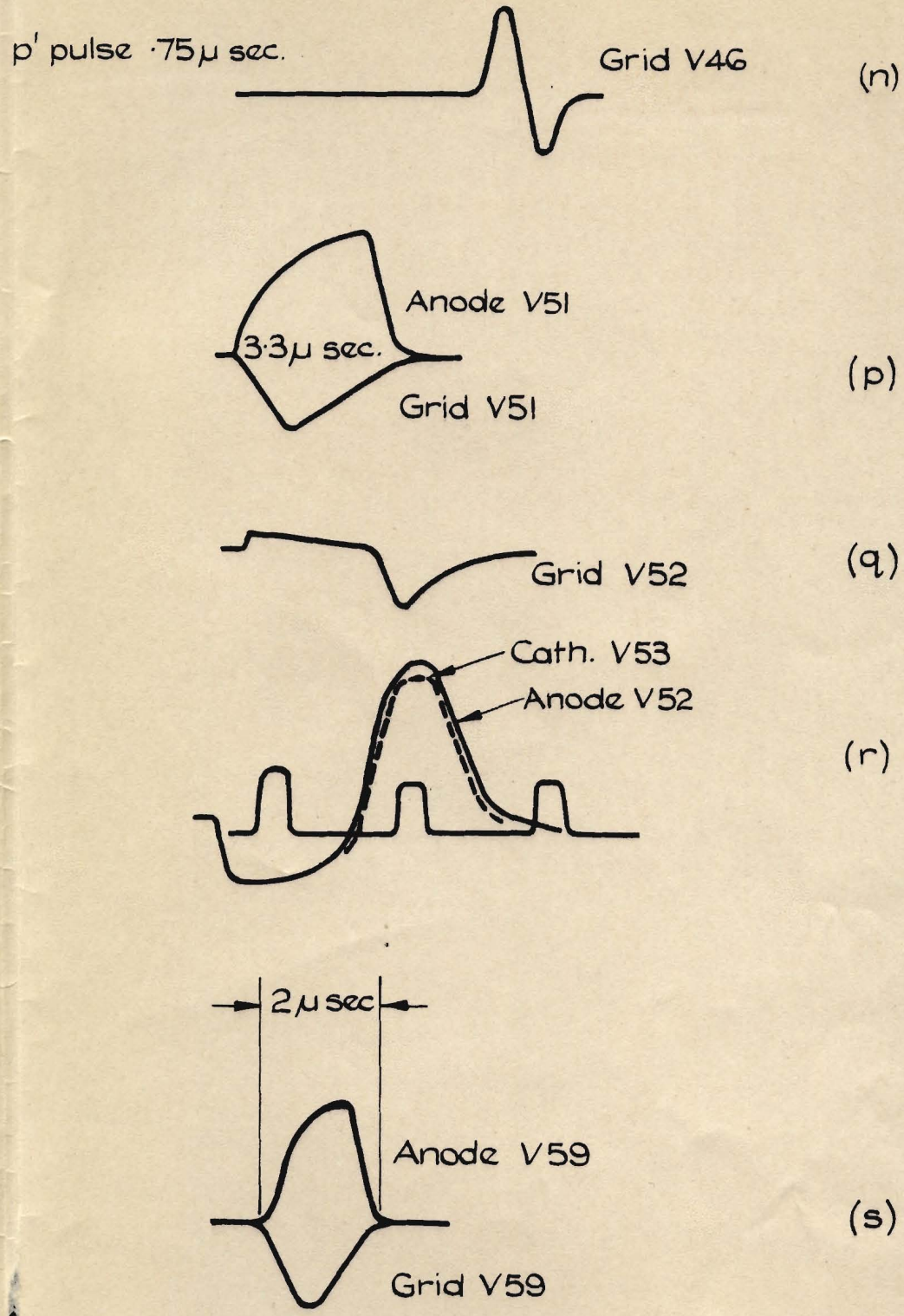

p' pulse ·75μ sec.
Grid V46
(n)
Anode V51
3·3μ sec.
Grid V51
(p)
Grid V52
(q)
Cath. V53
Anode V52
(r)
2μ sec
Anode V59
Grid V59
(s)

FIG. 1 (n - s)

SECTION P

CONSTANT GENERATOR

Circuit: B22591

1. **Circuit Description**
2. **Testing**
3. **Voltages.**

1. CIRCUIT DESCRIPTION

1.1 Two 20 digit constants and 3 single digit constants are available. The 20 digit constants are preset by means of switches on the control panel.

1.2 The switches are connected to the constant generator via plugs P80-4 and P80-5. When a switch is operated the corresponding (2) gates (V1a - V10b) or (V12a - V21b) allow a chain pulse to pass to the (3) gate controlled by the source selector.

1.3 Clock pulses are also fed to the (3) gates. The output is amplified and fed to the output trunk P6.

1.4 The three single digit sources produce pulses p1, p11 and p20 directly from the (3) gates as shown.

2. TESTING

Routine tests:-

2.1 Check divider voltages.

2.2 Check cathode voltages at the (3) gates. Note: Measure with S.U. off and all switches on N1, N2 off. The level of the base of the clock pulses ± mean voltage - 1/3 amplitude. There are two sources of clock pulses which must be checked independently.

2.3 Check breakthrough particularly in p1 position.

2.4 Check pulse output amplitude on P6.

2.5 The grid voltages of the (2) gate triodes should be checked occasionally - with switches down. Should equal -17 V ± 3 V.

3. VOLTAGE MEASUREMENTS

(a) Divider and Supply Voltages

Nominal	Measured
210 V	210 V
-100 V	-102 V
150 V	154 V
63 V	63 V
45 V	45 V
25 V	25½V

(b) Valves

Valve	Cathode	Design Value
D1	41	
D2	42	
D3, D6, D7	40*	
D4	41	Difference ± 2 V
D5	38	
D8	36	
D9	34	
D14, D17	36ø	
D15	35	
D16	41	Difference ± 2 V
D18	36	
D19	36	

* Mean = 48 V. Amplitude = 25 V.

ø Mean = 48 V. Amplitude = 35 V.

SECTION Q

ARITHMETIC UNITS

CIRCUITS

A Reg., B Reg., C Reg.,	A02 Chassis	-	B18599
	A03 Chassis	-	B18600
H Reg.,	A04 Chassis	-	B22585
D Reg.,	A04 Chassis	-	B22581
C Reg. and Shift Left		-	C23912
C and D Adders	A05 Chassis	-	B22590

LOGICAL SCHEMATICS AND LAYOUTS:

A Reg., B Reg., C Reg.,		-	B23209
D Reg.,	A04 Chassis	-	SKE 5167
H Reg.,	A04 Chassis	-	SKE 5166
C and H Reg.,	A04 Chassis	-	C-23125
C Reg. Layout		-	C22576
A04 Layout		-	C22562

PHOTOGRAPHS:

	Negative Number
A Reg.	3430-3
A and B Reg.	3430-7 3430-1
B Reg. Multiplier Seq. Unit	3430-4 3430-5
C Reg.	3460-6
D Reg.	3430-9

NOTE: The arithmetic units are distributed over four main chassis A02, A03, A04 and A05. The circuits drawings for any one chassis may therefore contain circuits belonging to more than one register. The division of the circuits is clear from the block schematics.

1. GENERAL NOTES
2. A REGISTER
3. B REGISTER
4. C REGISTER
5. D REGISTER
6. H REGISTER
7. OPERATION SHIFT LEFT
8. MULTIPLICATION

1. GENERAL NOTES

The form of the Arithmetic Unit is shown clearly in the logical schematic diagrams. The source and destination numbers and symbols are marked alongside the corresponding terminals so that the operation for any given command may be followed. The simple operations of read in, add in, read out etc. are straightforward whereas the operation Multiply into B (x B) results in a relatively complicated operation of gates.

An important point to note is that before any change is made in the circuit one must be certain that the true cause of the fault has been discovered. If this is not done it is possible to start a whole train of circuit modifications which are not necessary. The same principle is particularly important in regard to LC delay lines. A change in length of one delay line may affect several circuits and yet not correct the true fault.

2. A REGISTER

(a) Operation Read to A (→A). Destination P4-12

Input trunk pulses pass via gate G9 into the grid of V59(a) in the adder. At the same time a one minor cycle pulse via gate G10 inhibits the circulation of any pulses already in the A Register.

It is necessary that any pulses read into the adder be clocked accurately by the adder clock pulses on the grid of V59(b).

The accuracy of the clocking may be checked easily by observing V59 cathode. Photographs 1, 2, 8 and 10 (A Reg.) show good clocking while 5, 15 and 16 show the pulses slightly incorrect but not enough to cause wrong operation.

The clock pulses are fed from delay line L1, and their position must satisfy the requirements of pulses arriving from any possible source. These latter pulses vary in position slightly. Photographs 29-45 (A, B Reg.) show the pulses as they arrive in the P5 trunk, and Fig. 1 is a composite drawing. Note that the P5 pulses undergo a delay and are inverted before they reach the adder (Photographs 3, 4 (A Reg.)).

The spread of the pulses in Fig. 1 is reasonable except for those from the memory which are too late. This position may be improved with the design of a new memory read out unit.

The read in pulses pass through the first ½-adder and are amplified by V65 and appear as negative pulses on V67(a) grid. (Photograph 7 (A Reg.)). Photograph 8 shows the clocking which is observed now on the cathode of V67.

The pulses are amplified, pass through gate G26 to the modulator. The receiver output pulses are amplified and circulate through the LC delay lines L2, L3, gate 25, back to the circulating pulse input of the adder. The clocking of these circulating pulses must again be correct and should be observed the first time around by looking at V.

Should the clocking of the circulated pulses be incorrect, it is again important to be sure of the reason, e.g. low gain

in one of the amplifiers could result in apparently late pulses as well as changes in the LC or Hg delay lines.

Fig. 2 shows a block schematic of a register similar to the A Register with the relevant delay lines.

The order of adjusting the delays in the above circuit is as follows:

(i) Read in from a source which has read out pulses known to be in the correct position. There is no adjustment in the read out chassis, so any source except the memory should be satisfactory.

(ii) Adjust L1' and L2' taps so that the clocking is correct.

(iii) Adjust L3' for correct clocking on carry pulses.

(iv) Adjust L3 so that the circulating pulses are clocked correctly.

(v) Read out from Pt.A (in this case source ½A) and check that the position of these pulses is correct for the arithmetic unit read out clock. Adjust L1. (see(vii) below).

(vi) Check that the arithmetic unit read out pulses are correct in position by comparing these on the P5 trunk with those from the correct source chosen in (i).

(vii) The adjustment of L1 necessitates another adjustment of L3 so that the total delay in the loop remains the same.

(viii) Read out from Pt.B, check clocking in adder read out clock gate and adjust L2 and L3 again of required,

The exact connection to the delay lines is not always clear from the schematic and should be checked before making an adjustment. Fig. 3 shows another possible loop with an adjustable delay line. In this case, tap C, for read out at Pt.A, could be adjusted without affecting the loop delay. Adjustment of D would affect the loop delay without affecting the position of the read out pulses. Adjustment of tap B would affect both read out and loop delay.

(b) Operation Subtract from A(⇒A) Destination P4-28

Subtraction is carried out by adding the complement of the number plus a unit digit in the first position. This is carried out by gates G5, 6, 7 and the inhibited amplifier feeding V37(a).

The complement is obtained simply by feeding clock (pp') pulses into an amplifier and inhibiting the amplifier for any pulse coindident with a pulse in the incoming number.

01011101	incoming number
10100010	complement
1	fugitive digit

The fugitive digit is fed from V112(a) cathode to the

grid of V64(b) where it is added to the complement in the second ½-adder. The operation of the adder will be dealt with in Section (d).

Photographs 13-16 show the pulses on V59(a) grid and cathode with zero read in on the input trunk. No. 17 shows the fugitive digit on V64(b) grid and No. 18 the carry pulses on the grid of V66(a). The pulse on the right of No. 18 is that due to the fugitive digit. The result of the late pulses from the memory source is shown clearly in Photographs 29 and 41 (Memory). The late pulses fail to inhibit correctly in the amplifier gate and leave a spike at the beginning.

(c) Operations 'A, vA, vA

These operations should be clear from the logical schematic and the description given in Section B.

(d) The adder

Fig. 4 shows in simplified form the first half-adder. The shaded tubes denote conducting tubes for the conditions listed in the table. The tubes conduct during the clocking period when there are also pulses on the input and hence produce negative pulses at the outputs (s) or (c).

The sum pulse (s) from the first ½-adder is amplified in a cathode coupled amplifier V65 and fed to V67(a) grid in the second ½-adder.

Carry pulses (c) from the first ½-adder pass through a short delay line to the grid of the amplifier V63 and then to the grid of V66(a). Carry pulses from the second ½-adder

return directly to the grid of the amplifier which also acts as a delay of approximately 3 μsecs. The short delay line L7 is adjusted to make the time of arrival of pulses from both ½-adders the same at V66 grid.

The fugitive digit is fed into the second ½-adder grid which normally receives carry pulse. This is possible as there can be no carry in this position.

The carry pulse which would normally occur when adding two digits in the p20 position is inhibited by means of a P15-20 (chain) pulse on V64(a) grid. A positive pulse on the grid prevents a negative pulse being formed on V63(a) grid.

During multiplication it is necessary to inhibit the inhibition of this overcarry. This is obtained by increasing the bias on V64(a) via V127 and a pulse from the multiplier sequence unit.

(e) Read out operations from the A Register

These are clear from Section B and the logical schematic.

Flip-flop V27(A02) is set up if there is a p20 digit in the A Reg., and the 3 gate then allows a p1 digit to be read out during the transfer period. The flip-flop is reset by P2-4 pulses.

3. B REGISTER

The B Register loop does not have an adder so it is necessary to clock the pulses in a special gate comprising valves V53, 54, 57. The pulses appearing on the anode of V54 are clocked through to the cathode by the clock pulses on the

grid. V57 is a cathode fed amplifier.

In order to obtain sufficient tolerance on the clocking of the circulating pulses the delay line L6 is tapped at two points and the pulses mixed via V53. This results in a widening of the circulating pulses.

4. C REGISTER

This register is similar to the A Register. The adder also is similar except that the short (½ μsec) delay line has been omitted.

5. D REGISTER

Similar to the C Register except that the Register is 16 minor cycles long.

6. H REGISTER

This Register holds only 10 digits instead of the normal 20. A flip-flop V2 (A04) is triggered by P15-1 and P15-11 chain pulses and is used to gate in either the top half or the bottom half of an incoming number. Likewise the 10 digits in the Register may be gated out either in the top or bottom positions.

7. OPERATION SHIFT LEFT

When this destination is called and there is a p20 digit in the number received from the source, then the flip-flop V28 (A04) is triggered. The filp-flop is returned two minor cycles later by a P15-1 pulse, the resulting positive and

and negative double minor cycle pulses being applied to terminals P34 and P33A respectively.

Referring to A02, A03 block schematic it will be seen that the result of this operation is to connect the A and B Registers in series for the duration of the pulse. In addition, an extra 3 μsecs delay is included in the A loop immediately following the adder. The numbers originally in A and B thus finish up shifted one position to the left.

The series loop is obtained by the closing of gates G25, 24 and 26 and the opening of gates G22, 23 and 20.

8. MULTIPLICATION. DESTINATION P4-16 (x, B)

(a) Circuit

In order to multiply two numbers the multiplicand is first transferred to the C Register and then the multiplier is transferred to the B Register. The calling of the second destination (P4-16, x, B) initiates the multiplier sequence unit operation.

Referring to the A02, A03 block schematic the wave forms from the multiplier sequence unit are shown at the top. At the end of the transfer minor cycle, P33. P34 switch over for a period of 41 minor cycles. This period is called the multiplication cycle and during this time the A and B Registers and an extra 3 μsecs delay are connected in series as for the shift left operation.

Starting with the sign digit, each digit of the multiplier is inspected by gate G30. If the sign digit is unity the multiplicand is read out and subtracted into the A Register. If

any of the other digits are unity the multiplicand is added into the A Register. Owing to the extra 3 μ secs delay line, the contents of A and B shift left one position every two minor cycle circulation and thus the contents of C add into a different position each time. As each digit of B is inspected it is removed if it is unity and the growing partial product moves into the space provided. The sign digit of C is always removed as it is read out.

When the multiplicand is negative the flip-flop V85 (A03) is operated and the multiplier is subtracted into the A Register during the minor cycle when the multiplier is read into the B Register.

During multiplication it is necessary to remove the inhibition on the carry from the p20 to p1 position. This is done by means of V127 (A03) connected to the P34 pulse. This removal of the inhibition must be delayed until the end of the second minor cycle as otherwise the subtraction from C is not correct. The delay is produced by the connection to P31 from the grid of V127.

(b) Fault finding

Faults in the multiplier are usually discovered during the standard arithmetic test. The instruction which produces the error can be determined readily. When this is done the test CRO is triggered from the trigger unit and the multiplication inspected till the time of first appearance of the fault is discovered. It is often best to first check the output of the

multiplier sequence unit.

The above assumes that the fault results in erratic behaviour which can be seen on the CRO. A steady fault such as failure of the C Register sign test flip-flop may be more difficult to discover although observation of the results with positive and negative numbers would disclose the source of the fault.

One fault which occurred with the C Register sign digit flip-flop showed up as an error in multiplication with a positive multiplicand only after a negative number had previously been held in C. This was due to failure of the reset pulse to function properly.

The phantastron adjustment should be checked periodically. The present control has a tolerance of approximately ±80° of movement. The delay however is slightly dependent on duty cycle and if the setting has drifted to the edge of the band it is possible for a fault to occur at rare intervals depending on the duty cycle of the multiplications in the program. To reset the control check the setting during the standard arithmetic test and leave in the centre of the band.

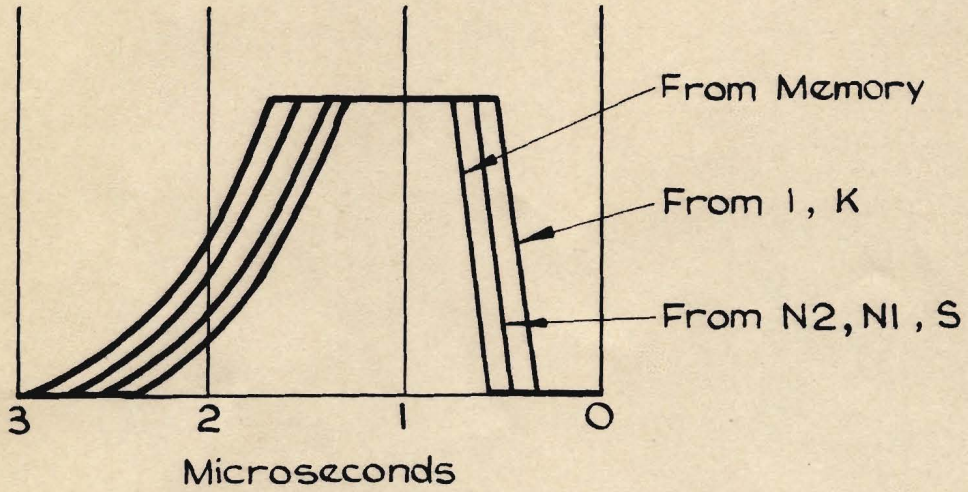


FIG. 1

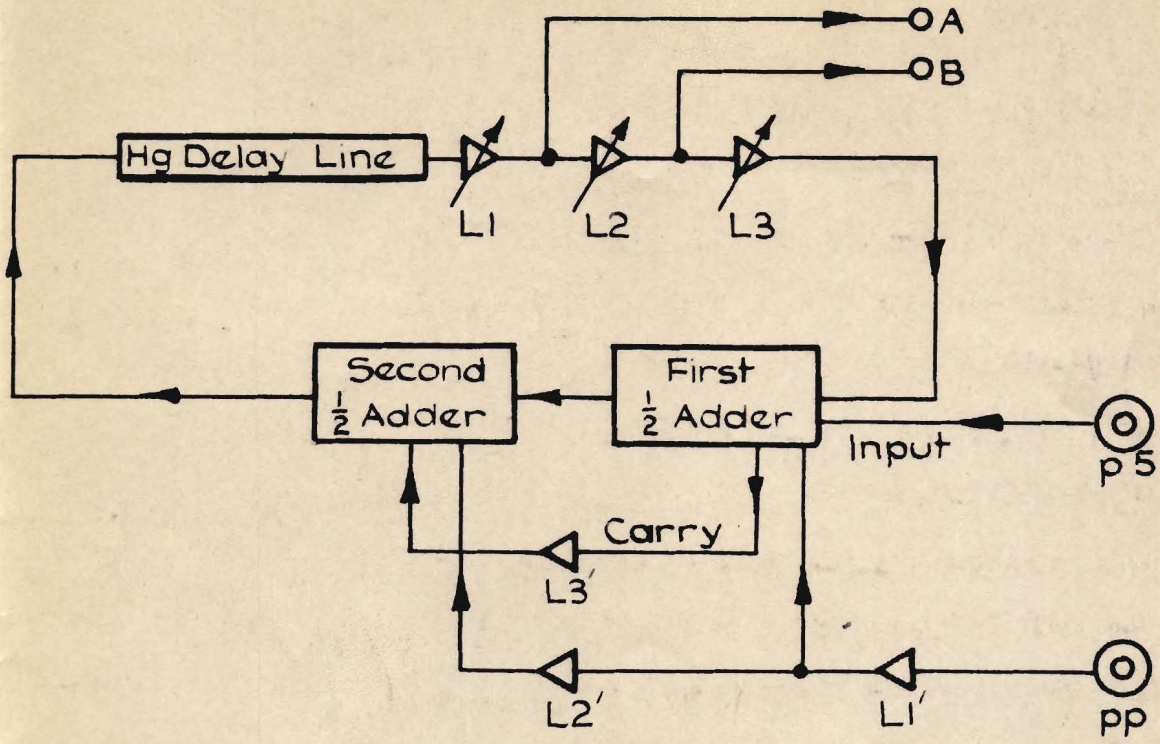

A
B
Hg Delay Line
L1
L2
L3
Second
½ Adder
First
½ Adder
Input
p 5
Carry
L3′
L2′
L1′
pp

FIG. 2

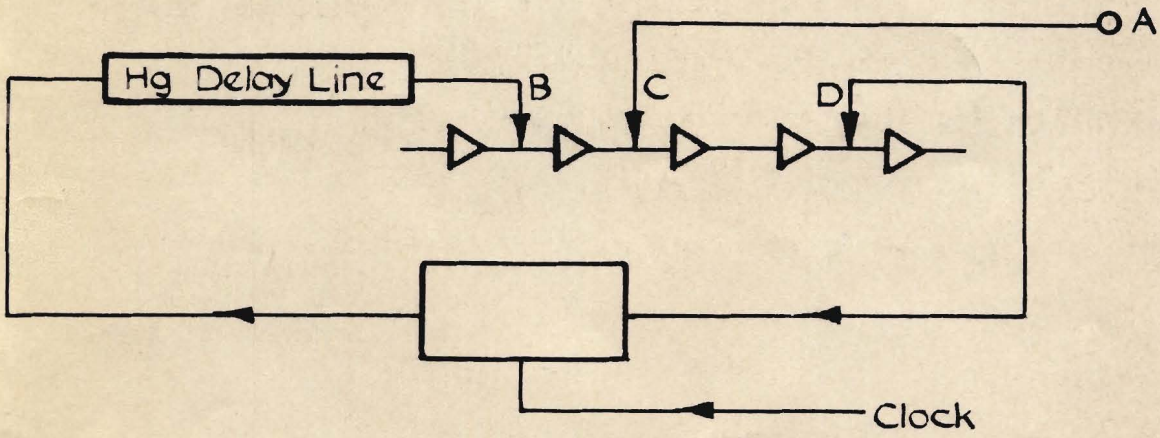

A
Hg Delay Line
B
C
D
Clock

FIG. 3

SECTION R

MULTIPLIER SEQUENCE UNIT

Circuit: B22589

Block Schematic: C23079.

Function:

The Sequence Unit is required,

(a) to connect the A and B registers in series for the period of the multiplication (41 minor cycles).

(b) to provide a minor cycle pulse which allows the multiplicand to be subtracted into A, during the first operation only, when the multiplier is negative.

(c) to provide odd chain 20 position pulses which inspect the digits of the multiplier and set up a flip-flop if the digit is a unit.

(d) to provide even p position pulses which reset the flip-flop mentioned in (c).

Pulse	Terminal	
	Positive during multiplication	Negative during multiplication
41 minor cycle	P34	P33
1 minor cycle	P32	P31
odd chain 20	P29	
even chain 20	P28	

Operation:

(a) At the commencement of multiplication a minor cycle pulse is fed to P35. This pulse coincides with the transfer control pulse.

(b) At the end of this pulse a p pulse, applied to P9, is gated and triggers the flip-flop V2.

(c) When flip-flop V2 triggers it is allowed to gate a p-pulse which triggers V10. There is an R.C. delay between V2 (V9)

and the gate so that the p-pulse which is gated is the one about a minor cycle after the start of V2.

(d) For as long as V2 remains triggered a chain of pulses is applied to V10 via the gates D9, D10 and D11, D12 on to one grid and via the gate D13, D14 onto the other grid. V2 thus switches back and forth each p-pulse.

In order to avoid trouble due to applying p pulses to both grids at the same time an integrating circuit is used in conjunction with the gates D11, D12 and D13, D14. Thus when the flip-flop is up one way, the gate which would pass the unwanted pulse at the next change over point is inhibited. The circuit is designed to be independent of component values and HT variations as much as possible.

(e) The outputs from V10 are applied via R.C. delay circuits to two sets of three gates. One set produces the train of even p position pulses and the other a train of odd chain 20 position pulses.

The P34 pulse (delayed) is also applied to the three gates to limit the pulses at P28, P29 to the length of the multiplication cycle.

(f) The trigger pulse from the D1, D2 gate (see(b)), also triggers the flip-flop V15 which is then restored by the next p pulse.

(g) The output from V15 gates a p-pulse at the end which triggers a second flip-flop V17. V17 produces the required minor cycle pulse at terminals P31, P32.

Both V15 and V17 use the combined integrating and gate circuit to prevent interference between triggering pulses.

(h) When V2 is triggered (see(b)) a pulse is applied to the phantastron V5, 6 which is adjusted to approximately 40 minor cycles in length. The output of the phantastron is amplified and applied to the three gate D6, 7, 8.

(j) While the phantastron is operated the three gate is closed. At the end of the phantastron pulse the next odd chain 20 pulse passes through the gate and resets V2. The odd chain 20 pulse will be the one occurring at the end of the 41st minor cycle so that P33, 34 are 41 minor cycles in length. The odd pulses are used so as to allow a greater tolerance on the setting of the phantastron pulse length.

Testing:

Assuming the P35 and P9 pulses have been checked it is best to check the operation in the following order.

(a) Check trigger pulse from D1, D2.

(b) Check that cathode of D9 is up after trigger pulse.

(c) Check operation of V10 and output from the following three gates.

(d) Once the P28, P29 pulses have been checked it is simple to check the three gate D6, D7, D8 and the operation of the V15, V17 flip-flops.

Voltages:

Note- All gates should have their base level at 28 volts. If any cathode differs from this voltage it is important to locate the reason for the change and not alter the voltage dividers which are common to several gates. The cathode followers V3, V4, V11, V16, V18, V19 have diodes to fix the base level. A check should be made periodically to ensure the

diodes are conducting when the grid voltage is low. The flip-flop voltages should be checked before making any change to the divider network which connects the plate of the flip-flop to the grid of the cathode follower.

21/10/54

Nominal -60 V - -62

Nominal 210 V - 207

M.S.U. H.T. - 200

Valve		Volts
V5	G1	-28
	G2-4	-14
	G3	-39
	K	-27·5
V2	K	-4·5
	G-a	-28
	G-b	-0·5
	A-a	138
	A-b	17·5
V10	K	+1
	Ga	-23
	Gb	0
	Aa	140
	Ab	26

Valve		Volts
V21	K	0
	Ga	0
	Gb	-40
	Aa	18·5
	Ab	160

Divider Voltages

Nom 20 - 20·5

Nom 13 - 13·5

Nom 50 - 50·0

SECTION T

MAGNETIC DRUM STORAGE UNIT

Sequence Unit B21944

Input Register and Writing Circuits.. C21976

Output Register C22031

Amplifier SKE5043

Counter and Coincidence Detector SKE4410

Clock Track Writing Unit C22620

Position Selector Unit B21622

Logical Schematic C22042

Sequence Unit Waveforms C22043

1. General
2. The 4096 Word Storage System
3. Magnetic Drum
4. Amplifier Unit
5. Input Unit
6. Output Unit
7. Position Selector Unit
8. Drum Sequence Unit
9. Voltage Measurements
10. Clock Track Writing Unit
11. Data on Drum Recording Heads
12. Notes on Coating of Drum.

MAGNETIC DRUM STORAGE UNIT

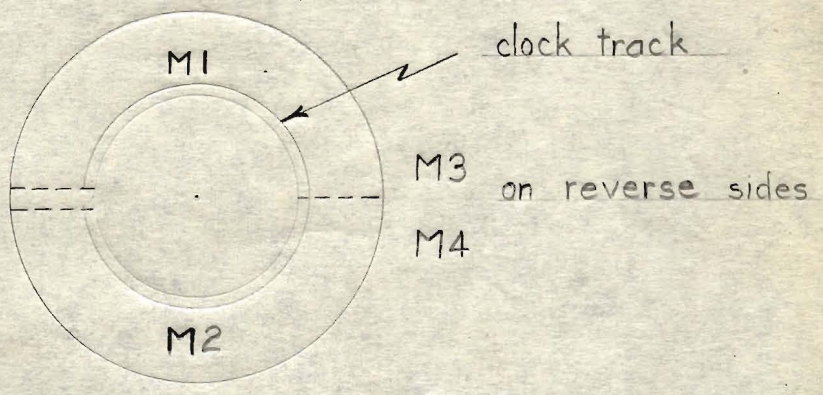
Servicing Notes

1 General.

These notes are intended to supplement report RPP 172 and to give additional information on the organization of the 4096 word drum which was not described in RPP 172.

2 The 4096 Word Storage System.

Disposal of the 4 groups of 1024 words on the drum is shown below.



Figures applying to the drum are as follows:-

Drum speed	2900 r.p.m.
Digit packing density	75 per inch of track.
Digit scanning rate (i.e. drum clock frequency)	100 kc/s.
Duration of gap between start and finish of tracks.	150 µsecs. (approx.)
Average access time (exclusive of time required to decode instruction)	10·3 milliseconds.

Storage groups M1 and M2 are associated with one set of tracks and recording heads, and groups M3 and M4 with another set. Relays are used to connect the reading and writing circuits to the desired set of heads.

As there are now 2048 rows of digits disposed around the drum compared with 1024 around the small drum the position selector unit has had an extra stage added. The position register has an extra flip-flop which is set to the "1" state if group M2 or M4 are called upon and remains in the "0" state otherwise. The clock track has 2048 intervals and the counter accordingly has eleven stages. Thus in selecting a position in group M1 or M3 the coincidence detector will operate some time during the first half revolution after passing the clock track gap, and in selecting a position in group M2 or M4 the coincidence detector will operate during the second half revolution.

Should it ever be desired to put the small magnetic drum back in service it will only be necessary to connect its coaxial cables to the amplifier unit and to unplug V44 in the position selector unit (see cct. B21622). In this case the eleventh stage of the position selector unit becomes inoperative, and, since the changeover relays will not be in use, any of the source of destination lines M1, M2, M3 or M4 will be equally effective for operating the drum.

3 Magnetic Drum.

(a) Motor. The "9" magnetic drum should not be started up too frequently since the starter winding is in circuit for about 10 seconds and is inclined to overheat.

The small magnetic drum requires a supply of 22 volts D.C. at approx. ·75 amps for a speed of 6000 r.p.m.

(b) Recording Heads. These should be set with the pole tips parallel to the drum and with a clearance of ·0015" from the highest spot on the drum i.e. ·0015" feeler is just gripped.

Initial magnetization of the tracks to the "0" level is most conveniently performed by momentarily connecting a 1·4 volt cell to the recording heads while the drum is rotating. The negative battery terminal must be grounded, and to avoid overheating the recording head the battery should not be connected for more than a fraction of a second.

4 Amplifier Unit.

The amplifier unit holds 20 identical channels for the data tracks plus a special amplifier for the clock track. There are two spare channels at the right hand side of the chassis which are not in use. The clock amplifier is at the extreme left-hand end of the chassis and is operated at full gain so that the last stage produces a square wave output. The 6SN7 blocking oscillator which generates the counter zeroing pulse is located at the top left-hand corner of the chassis.

The output stages of the digit amplifiers are now operated with zero bias. This places the operating point of the 6AC7's below the knee of the Ep - Ip curve so that only positive pulses can appear at the plate and much of the residual signal due to "0" digits is suppressed.

The amplifier gain controls should be set so that the minimum output amplitude for "1" pulses is 40 volts. If the track concerned has any eccentricity the output amplitude produced by portions of the track which approach closely to the recording head will of course be much higher than 40 volts. These regions should be watched for any tendency towards break-through of residual "0" signal.

5 Input Unit. See circuit SK(E)440.

The input digit train comes from the drum sequence unit on P106-5. The digit train is "staticised" through a row of 6SA7's at left of circuit and occupying the top row of chassis. The 6SA7's set the 6SN7 flip-flops (middle row of valves) to the appropriate digit configuration. A clearing pulse on P106-3 has previously reset the flip-flops to zero. The flip-flops operate on the -250 V supply. Their plate potentials set the bias on the control grids of the writing thyratrons (bottom two row of valves). Thus if V2 holds a "1" the control grid of V3 rests at -20 volts and the grid of V4 at -120 volts. A trigger pulse on P106-1 timed by the position selector unit is applied to all control grids. In the above case V3 fires and delivers a pulse of -ve polarity. When a "0" is recorded V4 fires and generates a positive pulse. The 50 K - 100 pF - 50 K decoupling network between the flip-flops and thyratrons is introduced to prevent thyratron trigger pulses upsetting the flip-flops.

Writing power for the thyratrons can be switched on or off by a push-button operated relay. Push buttons are also provided on the control desk. Special Notes: Precautions

must be taken to prevent removal of bias while the writing power is still applied to the thyratrons. If this happens a string of randomly timed pulses will be written into the drum tracks,obliterating any data which may be held there. Furthermore if any negative pulses are written into positions intermediate between the standard "cells" the resulting magnetic pattern cannot be overwritten by pulses timed by the position selector unit. The tracks must then be "cleaned up" by the standard procedure described previously.

Wherever possible the writing power should only be switched on when required. To take care of other contingencies such as may occur when the equipment is switched off with writing power still applied, the -250 volt supply is equipped with sufficient shunt capacity to make its decay time constant much longer than the time constant of the anode power supply. An interlock relay in the -250 volt supply switches off the +200 volt supply whenever the former voltage is removed.

6 Output Unit. See circuit SK(E)4430.

Numbers enter the output register through the row of 6SA7's at the top of chassis. Outputs of the drum reading amplifiers are applied to the 6SA7 third grids. First grids of the 6SA7's are commoned and are turned on by the position selector pulse (P106-2). A positive peak in any amplifier output at the selected position will set the associated output flip-flop (middle row of valves) to the "1" state.

The flip-flops are cleared at the start of a "read" operation by a positive pulse on the clearing line P106-3. A manual clearing switch is also provided.

Parallel to serial gating. This function is performed by the bottom row of 6SA7's. The first grids of the latter valves are turned on if the associated flip-flop holds a "1". A negative train of pulses then appears on the common plate lead. This is coupled to the grid of V61A with D.C. restoration. A positive train of pulses is developed at the plate of V61A and fed to the cathode follower V61B. This cathode follower operates in a normally cut-off condition to remove "break-through". Its standing cathode potential is set at +15 volts to suit the gate at the receiving end of P105-1. The digit train appears on P105-1 continuously as long as there are one or more unit digits in the output register.

Special Notes: Owing to the extra width of the "Chain 20" pulse a differentiating circuit is used to couple it to the associated 6SA7 to prevent break-through in the p1 digit position.

A cathode follower is used to provide the +100 volt supply. This is necessary to achieve good voltage regulation since the bleed varies by about 15 mA depending on the content of the output register.

7 Position Selector Unit. (Circuit B21622).

The operation of this unit differs from the one described in RPP 172 in the following respects.

1. The counter operates subtractively.

2. The 100 K summing resistors are connected between corresponding plates of the counter and register flip-flops.

3. The blocking oscillator pulse shaper has been replaced by a different circuit.

4. An additional counter and register stage have been added to take care of the 9" drum.

5. Provision has been made for an additional row of position register indicator lights on the computer front panel.

As a result of modification 1 the counter is cleared to zero in the clock track gap and then goes through a complete count 2047, 2046, ..., 0, as the drum rotates.

Modification 2 then ensures that the storage positions 0, 1, 2, 3 etc. occur in correct time sequence starting from the beginning of the tracks.

Owing to the limited space available for adding valves to the chassis, 4 EA50's have been used as buffer diodes between the last three counter stages. Shaping of clock pulses is now done with the aid of an inductor L1 in the plate circuit of V57B. V57B is turned off by the negative-going edges of the square wave train received from the clock amplifier. A train of positive pulses is then generated across L1, their duration being determined by its natural frequency (about 2 μsecs.)

Negative swings are also produced at the plate of V57B due to the positive edges of the clock amplifier waveform. However the negative swings are cut off by the cathode follower V57A which feeds positive pulses to a 6 μsec delay time.

<u>Special Notes</u>: The counter time delay for propagation of carries between stages is about 0·2 μsec.

8 <u>Drum Sequence Unit</u>.

Circuit B21944 Block schematic SK(E)4429. Waveforms SK(E)4993.

(a) <u>Writing Operation</u>.

General remarks: When writing on the drum the main

sequence unit runs through its normal cycle and is then stopped. Receipt of the second component of P2-4 indicates that the position register and drum input register have been properly set up. The next available position selector pulse can then be used to trigger the writing circuits. However if the current operation involves changing over the track selecting relays an extra 4 msecs delay must be introduced before accepting the position selector pulse. This is to ensure that the relay contacts are properly closed.

The main sequence unit is restarted as soon as the writing operation is complete.

Detailed Operation:

1. Activation of any of the destination lines P4-13, P4-14, P4-21, P4-30 causes the common cathode potential of V21, 22, 23 and 24 to rise and hence also the cathode potential of V28. This occurs at the end of P2-3.

2. The output of V28 is applied to a "2" gate (G9, G10, V35) along with P2-9. The leading edge of the gated output triggers thyratron V34 which generates a clearing pulse for all the drum registers.

3. The latter pulse is fed to P19 through cathode follower V27B and trips the "stop" flip-flop in the main sequence unit.

4. If the operation involves M2 or M4 (either as destination or source) the cathode potential of V14 and V15 will rise.

5. The latter potential opens "2" gate V46 along with P2-6 and sets up the position register 11th digit via P106-7.

6. The position digits appearing on P6A are gated through V20, G5 and G6 to P106-4 and thence to the position register.

7. The digits appearing on the input trunk P5 are gated through V39A, G11 and G12 to P106-5, and thence to the input register.

8. If "condition A" applies (see top of SK(E)4993) the second component of P2-4 passes through V36 and triggers V33. Slow rise of destination line prevents first component of P2-4 getting through V36.

9. If "condition B" applies the state of flip-flop V3 will be reversed. V3 is tripped over by either V12, 13 or V25, 26, and also causes V5 to be triggered through V4. V5 is A.C. coupled and provides a time delay of 4 milliseconds. During the time delay period V36 is inhibited by removal of screen voltage and at the end of the time delay period V33 is triggered through V6B. V3 "remembers" which track group was last referred to and is unaffected if same group is called on again. If M3 or M4 is called upon the change-over relays are energized through cathode follower V7, and if M1 or M2 is called upon the relays are de-energized.

10. V33 is an A.C. coupled flip-flop with a natural delay time of about 80 µsecs. Injection of drum clock pulses ensures that its back edge is locked to one of the latter pulses. This back edge triggers flip-flop V29.

11. V29 has a natural delay of at least 25 milliseconds. It allows the next available position selector pulse on P102-1 to pass through gate V31, G7, G8 and V32A. The latter pulse resets V29 so that the actual time delay of this

flip-flop may be anything from a few microseconds to 20 milliseconds depending on the chance time relationships existing between the drum and computer systems. Interposition of flip-flop V33 ensures that V29 does not open V31 in the middle of a position selector pulse.

12. The output pulse of V32A passes through gate V37 and triggers blocking oscillator V38 whose output in turn goes out through P106-1 to trigger the writing circuits.

13. Flip-flop V45 is also triggered by the output of V32A and its back edge is reset by a P pulse after a delay of 4 to 5 minor cycles. A negative pulse coincident with the back edge is generated by V44 and passed to P83A as a sequence unit restart pulse. The latter pulse is inhibited during one-shot operations.

14. The most critical condition which can occur with the computer operating on "speed-up" is when the contents of the sequence register end with ----1111. In this case the destination line will start rising just before the end of the first major cycle period and just before the beginning of P2-6. Hence the position register will be cleared a few microseconds before new digits are set into it. However no trouble should result from this circumstance unless some agency causes the destination (or source) lines to rise more slowly.

(b) Reading Operation.

General Remarks: When a number is read out of the drum the main sequence unit executes two "shots". During the first "shot", waveforms are generated as far as the end of

P2-9 and the rest of the waveforms are inhibited. This allows the position digits to be read out on P6A into the position register whereupon the next available position selector pulse is allowed to gate the contents of the selected storage position into the drum output register. At this point the main sequence unit is restarted and executes its second shot during which the contents of the output register are transferred to the selected destination.

Detailed Operation:

1. Activation of any drum source line causes the common cathode potential of V8, 9, 10, 11 to rise at the end of P2-3. During the second "shot" the source line drops when the interpreter is cleared by P2-7 and rises again at the end of P2-3.

2. The source line waveform is transferred through the inhibition gate V16 and is inhibited during the majority of the second "shot" by a waveform from flip-flop V42 (to be described later).

3. The output of V16 is fed through cathode follower V27A to P84 and prevents the main sequence unit generating any waveform subsequent to P2-6 during the first "shot".

4. Generation of pulses on P106-4 occurs in much the same way as was described for a writing operation. Similar considerations apply to the triggers of V3, V5 and V33 except that V33 is triggered by P2-6 through V17 when "condition A" applies.

5. V29 is triggered by the back edge of V33's pulse and allows the next available position selector pulse to pass through V31 and V32A resetting V29.

6. The output of V32A passes through V18 and triggers blocking oscillator V19 which opens the reading gates in the output unit via P106-2.

7. V45 is triggered from P106-2 and reset by a P pulse causing the main sequence unit to be started through P83A. Note that under one shot conditions the main sequence unit will stop after the second "shot" by virtue of its own internal arrangements.

8. The A.C. coupled flip-flop V42 having a natural delay time of 4 msecs is triggered by V19's output. It is however reset by P2-10 at the end of the second "shot". The V42 pulse inhibits V16 as previously described and its leading edge is differentiated and mixed into the P2-4 line via cathode follower V43. This pulse is necessary to clear the time and line selectors circuits which would otherwise remain uncleared after the incomplete first "shot".

9. The "source" waveform has meanwhile opened gate V3 etc. and allows the contents of the output register received via P105-1 to pass to the output trunk after "clocking". Since the output register is initially cleared nothing actually appears on P6 until the position selector pulse is gated through to P106-2.

MAGNETIC DRUM SYSTEM

VOLTAGE READINGS

UNIT	TEST POINT	NOMINAL VOLTAGE	ACTUAL VOLTAGE
	Supply Voltages	+210 V +300 V -250 V	+210 V +290 V -250 V
Position Selector Unit	Voltage Dividers	+185 V +170 V +100 V - 20 V - 60 V	+185 V +167 V + 95 V - 20 V - 57 V
	All flip-flops: Cathode		48- 54 V
	All flip-flops: "off" plate		180-184 V
	All flip-flops: "off" grid		30- 34 V
	All flip-flops: "on" plate		95-105 V
	All flip-flops: "on" grid		49- 55 V
	V44-V54 plate		180 V
	V44-V54 cath.		167 V
	V55 plate		+210 V
	V56A grid		+ 3 V
	V56A plate		+ 25 V
	V56B cath.		+ 9 V
	V57B cath.		+ 3 V
	V57A cath.		+8.5 V
Input Unit	Voltage Dividers	+120 V - 25 V	+118 V - 23 V
	All flip-flops: Cathode		-182 to -187 V
	All flip-flops: "off" plate		- 16 to - 17 V
	All flip-flops: "off" grid		-205 to -210 V
	All flip-flops: "on" plate		-120 to -130 V
	All flip-flops: "on" grid		-182 to -187 V
Amplifier Unit	1st stage: Cathode		1.0- 1.2 V
	1st stage: Screen		58- 65 V
	1st stage: Plate		90-110 V

	2nd stage (Cathode Screen Plate)		1·4-2·0 V 95-120 V 100-130 V
	3rd stage (Cathode Screen Plate)		50-70 V 50-80 V
Output Unit	Voltage Dividers	+100 V + 70 V - 25 V	96 V 66 V
	Cathode "off" plate "off" grid "on" plate "on" grid		49-52 V 165-170 V 32-38 V 67-73 V 52-55 V
	Grid3 V41-V60	on off	110-120 V 44-50 V
	V61A grid V61A plate V61B grid V61B cathode	Output register cleared	+·25 V +90 V + 5 V +15 V

10 Clock Track Writing Unit.

Refer Schematic C-22620.

This unit enables the computer to be used to write on the initial clock track. It is necessary to generate an alternative source of clock pulses synchronized to the drum and to feed these pulses into the counter of the drum unit. It is very difficult to maintain an oscillator in synchronism with the drum for the 5 (or 10) secs required to write in the clock track. This problem is overcome by putting a single pulse on the drum and using this pulse to start off a ringing oscillator at each revolution. The oscillator is adjusted so that just before the end of the revolution 1024 (or 2048) cycles have been produced. At this point the oscillator is shut down until the next synchronizing pulse is received.

The procedure then is to put a single pulse anywhere on the drum clock track by discharging a ·01 condenser through the head with the drum stationary. With the drum running at speed the single pulse output from the clock track amplifier is fed to the start terminal of the clock track writing unit. The connection from the amplifier to P101-24 is removed. The output from the writing unit is connected to P101-22 on the counter unit.

The stop terminal of the writing unit is connected to the anode of V1.

The frequency of the gated oscillator is then adjusted until there is a gap of about 150 μsecs between the first and last pulses.

The clock pulses may then be written onto the drum by

setting N1 to N2 $\longrightarrow$ M' and using the operation N1 + S.R. to K. Starting from S.R. = 0 the required number of pulses will be read in. For the large drum it will be necessary to trigger stop the read in at 1023 and then switch the destination selector to provide the zero digit in the units position.

11 <u>Data on drum recording heads.</u>

<u>Notes</u>:

(1) Recording done with ·002 μF condenser discharged through head. Tests were done with 100 turn windings. Results should be similar with 45 turn heads using ·01 μF condenser charged to same voltage.

(2) Playback pulse is described in terms of its extrapolated pulse length (EPL) viz.

If EPL is measured as t microseconds at drum velocity v (inches/microsecond) then EPL can be expressed as vt inches equivalent length on drum surface.

Digits can be packed at spacings down to 70 % of EPL or permissible no. of digits per inch = 1·4/EPL.

(3) Increasing condenser charging voltage increases playback amplitude until saturation is reached. EPL increases progressively with condenser voltage.

MEASUREMENTS USING 2" WHEEL AT 12,000 R.P.M.

i.e. ·00125"/µSEC.

Head Serial No.	Head Clearance	Condenser Charging Voltage	Playback Peak to Peak Volts	EPL µsecs	EPL ins	Permissible digit packing density digits/inch
ζ (·001" gap spacer)	·001" to ·0015" (not accurately known)	120	100% = 19mV	20	·025"	56
		100	90%	16	·02 "	70
		80	80%	13	·016"	87
		60	65%	12	·015"	93
δ (·002" gap spacer)	·001"	120	100% = 12mV	18	·022"	64
		100	100%	16	·02 "	70
		80	90%	13·5	·0175"	80
		60	60%	10	·0125"	110
H (·001" spacer)	·0015"	150	100% = 13mV	20		
		100	90%	15		
		75	70%	13		
		50	60%	11		
	·001"	100	100% = 12mV	14·5		
		75	90%	12·5		
		50	60%	10		
TEST ON MK1 HEAD USING ·01 µF CONDENSER						
Two heads much the same performance	·0015"	200	100% = 4mV	14·5	·018"	77
		150	95%	14·0	·0175"	80
		100	75%	14	·0175"	80
		75	60%	12·5	·0155"	90
		50	40%	11·5	·0145"	97

12 <u>Notes from P.R.E. (U.K.) on Coating a Drum with Magnetic Oxide Dispersion.</u>

Drums may be coated directly on to the metallic surface, but when a steel drum is used, electro-plate the steel with copper to a thickness of the order of 0·015 inches. This should then be turned on the drum bearings, and the surface skimmed to make it truly concentric with the axis to within 0·0001 inches The thickness of the remaining copper will be something over 0·012 inches. At R.R.E. no appreciable loss of signals has been observed due to the magnetic coating being close to the conducting surface.

The magnetic material which has been used is a red oxide suspension obtained from the Minnesota Mining and Manufacturing Co. Ltd., and is identified by the code B25S. The company advises the use of any good nitrocellulose undercoat for use as a primer, but we, at R.R.E., have used the E.M.I. primer "S". It is understood that bute rubber has been used in the U.S.A. but we have no experience with it.

First, degrease and clean the surface of the drum quite thoroughly. The E.M.I. primer is thinned with methyl acetate. Then, for the magnetic coating, we have thinned down the magnetic oxide dispersion far more than is recommended in the company's leaflet; we used 1 c.c. of suspension in about 40 c.c.s. of thinners composed of 2 parts butyl acetate, 1 part toluene and 1 part xylene. This almost watery suspension is sprayed on the drum, after filtering, with a very fine air brush while the drum is rotated at about 200 r.p.m. The final

thickness is of the order of 0·0005 inches for each of the primer and of the magnetic coating. If the latter is continued much beyond this, we find that after some critical thickness has been reached, the surface rapidly becomes very rough, with the result you describe of outputs of varying amplitudes due to pin head size bumps etc.

Allow the coating to harden for about a week; we have not yet met any bubbles, and have found that the coating will stay put on the surface of a drum six inches in diameter while it is spun at 31,000 r.p.m. (We pushed up the frequency of a 400 cycle synchronous motor.)

SECTION U

OUTPUT REGISTER AND CONTROLS

Circuit: SKE5185

Logical circuit: C23911

A. Firstly consider the operation when the teleprinter or punch is ready to receive a signal.

1. During the read in part of the cycle gate G22 is open and the digits are fed into the register. The register will have been cleared just previously by the P2-6 pulse passing through gate G1.

2. The P2-10 pulse which occurs near the end of the computer cycle triggers V41.

3. The pulse formed from the differentiated front of the V41 change over passes through either gate G6 or G7 (see note C.1.) depending on whether Punch or Print has been called.

4. The output of gate G6 is amplified and triggers V46 flip-flop to give a clutch or relay operating pulse of length approximately 20 millisecs long.

5. At some time during the teleprinter or punch cycle a positive pulse is received on P87 to indicate that the unit is ready to receive another signal. In the case of the tape and card punch, a clear register pulse is also received on terminal U (P86-1).

6. When V50 is triggered, gate G5 is opened and a P2-1 pulse, if the sequence unit is running, resets V41. If the sequence unit is not running, the end of the V50 flip-flop pulse is differentiated and will reset V41.

7. The resetting of V41 sends a start signal to the sequence unit via P83.

B. Secondly consider the operation when the teleprinter or punch is <u>not</u> ready to receive a signal.

1. V41 flip-flop has been set up as in paragraph A.2.

2. When the output register is again called, the rise of the destination signal triggers V43 via gate G4 which has been opened by V41.

3. The rise of V43 sends a stop pulse to the sequence unit via P19, and a stop add one pulse via P84. The length of V43 must be adequate to cover to the end of P2-6, i.e. at least 1½ millisecs. The fall of V43 produces a P2-4 pulse which is required to clear the time and line selectors.

4. The sequence unit therefore remains inoperative until a ready signal is received via P87 as in paragraph A.6.

5. It is necessary to reset V50 with the P87 trigger pulse as otherwise it was found the V50 sometimes gated two P2-1 pulses. The second pulse then gave a false indication that the output unit was "ready".

C. General Notes.

1. The gates G6 and G7 have one gate voltage applied to the lower end of the grid resistor and limited by a diode to ground. The other gate voltage is applied to the grid and must be also limited in amplitude to prevent breakthrough. Limiting depends on choosing a suitable value of the grid to ground condenser.

2. P84 (stop add one pulse) inhibits all sequence unit waveforms after and including P2-2, thus necessitating a P2-4 pulse to be generated to clear the time and line selectors.

SECTION V

START UNIT

Circuit: C22573.

1 This unit accepts pulses which may occur at any time and delivers start pulses to the Sequence Unit at times fixed relative to p pulses and in such a position that they cannot cause incorrect operation of the Sequence Unit.

2 Incoming pulses trigger the delay multi V2. The anode of V2a rises and allows delayed p pulses to be passed through V3.

3 The negative delayed "p pulses" then trigger the Sequence Unit.

SECTION W

TRIGGER UNIT

Circuit: SKE4942.

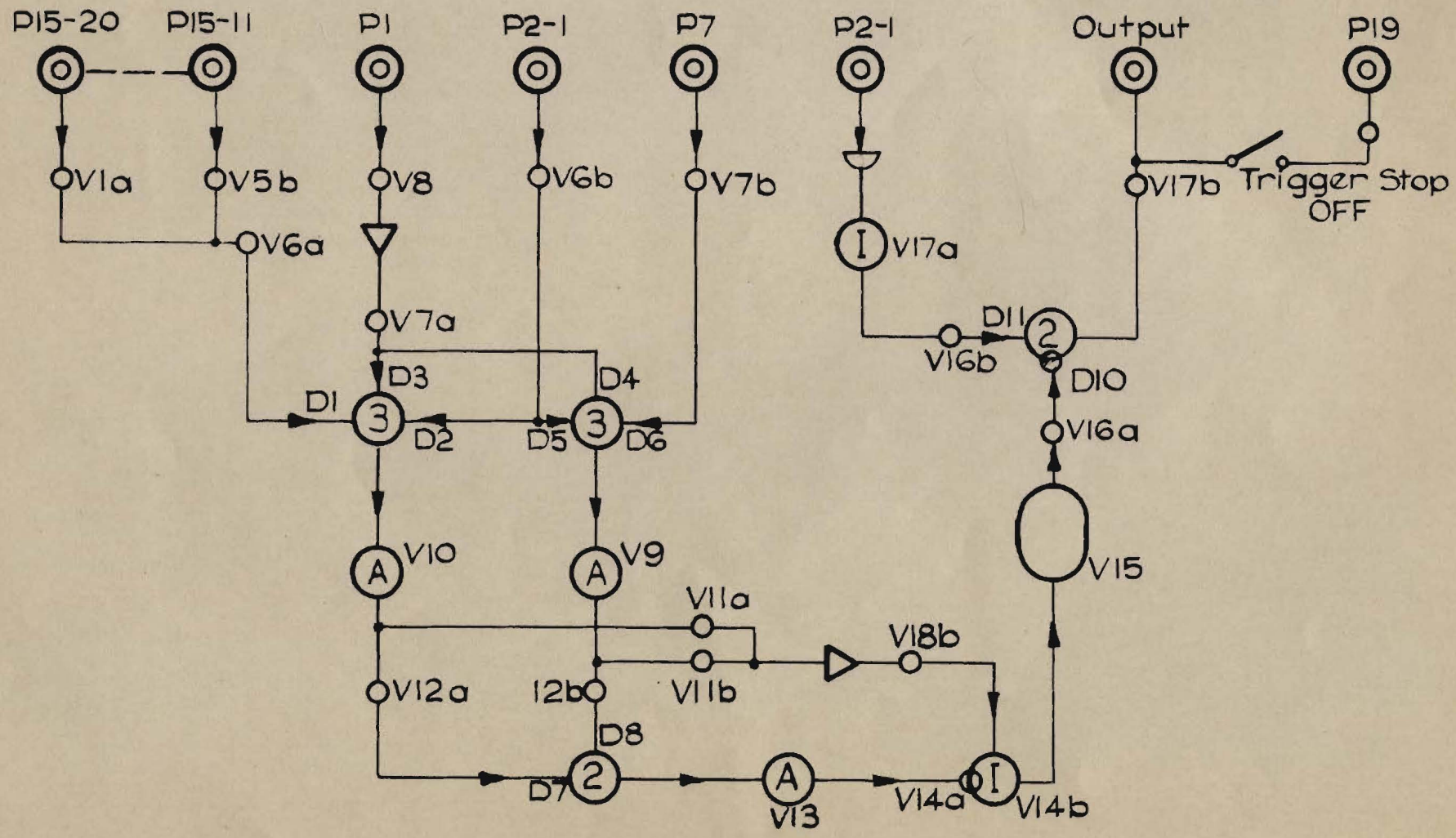
1 The trigger unit detects coincidence between the number read out of the sequence register during the P2-1 cycle and a number set up on certain switches of the control panel.

2 When the above numbers are equal a pulse is sent to the output terminal. This pulse may be used to trigger a CRO or stop the sequence unit at the end of the current cycle.

3 Referring to Fig. 1, it can be seen that the clocked digits of the two numbers will appear at the cathodes of D7 and D8 and V11a and V11b. If the numbers are identical there will be inhibition pulses on the grid of V14a and no output from V14b.

4 V15 will not be triggered so that the D10, D11 gate will remain open and the differentiated back edge of P2-1 will form the trigger pulse.

5 Note that the trigger pulse on V16(b) only gets through if the flip-flop has <u>not</u> been operated.



TRIGGER UNIT

FIG. 1

SECTION Y

CONTROL DESK UNITS

Drawings

Uniselector Input:	B21768
Operation Control Relay Unit:	C22992
Control Panel - Front View:	B21341
Wiring and Tag Strip Connections:	SKE5191
Teleprinter Control Unit:	C22563
Output Driver Unit:	C23914
Card Punch Control Unit:	C23781

1. Uniselector Input
2. Operation Control Unit
3. Control Panel
4. Teleprinter Control Unit
5. Output Driver Unit
6. Card Punch Control Unit.

1. UNISELECTOR INPUT

1.1 This unit is used to feed the initial data into the computer. The data is wired into the uniselectors which, on the pressing of the "Uniselector Start" button on the control panel, automatically scan the data and feed it into the memory.

1.2 On pressing the "Uniselector Start" button 100 volt is applied to P80-3 terminal 2, RY 2 closes followed by RY 3, RY 2 releases, RY 3 releases, RY 2 closes, RY 3 closes and so on until the end of the scan.

1.3 During the scan the 100 volts is maintained via bank 17 so that the start button need not be held closed for only a short period.

1.4 Relay RY 4 (two relays in parallel) closes each time RY 3 closes and supplies volts to the motor coils of each uniselector. The scan ceases when the contact on bank 17 rotates back to the first position and removes the 100 volt supply.

1.5 The contacts on bank 16 serve to clear the sequence register before and after the read-in operation.

1.6 Bank 18 contacts operate the "start" relay in the sequence unit.

1.7 Bank 20 contacts close RY 5 in the Operation Control Unit and remove the "lock in" on RY 4 of the same unit. (See notes on the Control Unit)

1.8 The Uniselectors may be "homed" to the correct starting position by closing RY 1 via a push button on the Control Panel.

2. OPERATION CONTROL RELAY UNIT

This unit is provided in order to simplify the switching required for special operations. For example, during read-in from the uniselectors it is only necessary to press the Uniselector Start button. The other operations such as clearing the sequence register, setting up digit d6 on N1, one shot etc. are connected in circuit automatically by the relay RY 4.

The operation of the other relays is clear from the circuit.

3. CONTROL PANEL

3.1 Referring to B21341 the switches are numbered from right to left with an S number for each row as shown on the drawing.

3.2 Row S1.

The tape and slow speed controls have not been connected. The tape controls were intended for direct high speed or one shot stepping of the tape. The slow speed controls were for motor operated "one shot" operation of the sequence unit.

3.3 Row S2.

The central group of switches control individual relays in the computer and enable any special operations, not found in the "Operation" switches (S7), to be obtained. The switches are normally all in the up position.

Switch	Function
S2-14	Contents of Sequence Register are read into the Interpreter during the P2-3 cycle.
S2-13	Removes "add one" pulse from the Sequence Register.
S2-12	Continuous or one stop operation.
S2-11	Reads contents of N1 into the Interpreter during the P2-3 cycle.
S2-10	Operates relay in Input Register which allows the Register to be cleared by a pulse from the Tape Reader Control Unit.
S2-9	Not connected. Was intended to operate relay which disconnected the stop pulse lead from the Sequence Unit.
S2-8	Connects the stop pulse from the Trigger Unit to the Sequence Unit.
S2-1,2,3	Operate relays controlling the supply of 100 volts to the units named.

3.4 Row S3.

(a) Switches S3-15 to S3-20 select the Hg store line for presentation on the monitor CRO.

(b) Switch S3-14 changes from Hg store to the D register.

(c) Switches S3-1 to S3-10 select the Sequence Register number for which a coincidence pulse is required. (See notes on Trigger Unit.)

3.5 Rows S4, S5 and S6.

Refer to the constant and input registers which may be set up manually.

3.6 Row S7.

(a) Switches S7-11 to S7-20 provide manual clearing of the registers named. All the arithmetic registers are cleared by S7-20.

(b) Switches S7-1 to S7-10 operate through the operation control relay panel, to provide correct group operation of the various relays throughout the computer.

3.7 Row S8.

(a) Positions S8-1, 2, 3 are not used.

(b) S8-4, 5 are in parallel.

4. TELEPRINTER CONTROL UNIT

4.1 The control unit can be understood better if we state the requirements of the Teleprinter. The timing cycle of the printer is shown in Fig. 1.

(a) The printer is at rest when a number is fed into the output register.

(b) The code bars must first be set up and then the clutch magnet operated.

(c) The symbol is printed at A and the code bars reset at B.

(d) The next code may be reset any time after B and before F.

(e) The clutch magnet for the next operation may be operated anytime after C.

(f) Motor speed = 33 revs/sec.

Teleprinter shaft speed = 7·3 revs/sec.

4.2 The timing of the relays is shown in Fig. 2.

(a) V1 is triggered with a pulse on P86-3.

(b) Relay K closes after a delay determined by the value of R5, C5.

This delay is required to allow time for the relays L, M etc. to operate or open as the new digits are set up.

(c) When K closes, the code bar magnets are operated.

(d) After a delay determined by R6, C7 relay J operates to remove the voltage from the code bar magnets and apply volts to the clutch coils.

(e) The contact on the teleprinter shaft cam closes shortly after the shaft commences to rotate and relay H closes.

(f) Relay K and Relay J then open, the latter removing voltage from the clutch magnet.

(g) Fuses F1 to F6 protect the code bar magnet & clutch magnet coils and will open circuit if the voltage is left on the coils for appreciably longer than shown in Fig. 2 time cycle.

(h) When the shaft has rotated about half a revolution the cam contact opens, H opens and a "teleprinter ready" signal is sent to the computer. The cam contact is arranged to open well before the shaft completes the revolution in order to speed up the printing time.

4.3 Contact S1 is opened when the teleprinter motor is off. This prevents the thyratron being triggered and energizing the clutch magnet. Unless the shaft is rotating, the clutch magnet remains energized and would blow the fuse.

5. OUTPUT DRIVER UNIT

5.1 This unit contains 6V6 cathode followers for driving the magnet coils in the tape punch,card punch and teleprinter.

5.2 Tubes V1 to V12 operate the interposer bar magnets on the tape punch or the digit relays on the card punch control unit depending on which unit is connected. V16 operates the tape punch clutch coil or RY 10 on the card punch unit.

There is no provision for operating both punches at the one time.

5.3 Tubes V13 to V17 operate the digit relays in the teleprinter control chassis.

5.4 Tubes V19, V20 are connected with the control of the tape punch.

The cam on the tape punch opens and closes a contact as on the teleprinter. When the contact closes at about half way around, a clear pulse is sent to the computer and the delay multi V19 is triggered. At the end of the delay period of 20 millisecs a tape punch ready pulse is sent via P87 to the computer. The early clear pulse ensures that the interposer bars have time to fall out properly.

OUTPUT DRIVER

Cable P114-A to Punch

Output Driver	Pin No.	Punch Pin No.
Digit 1	A	A
d 2	B	B
d 3	C	C
d 4	D	D
d 5	E	E
d 6	L	F
d 7	M	G
d 8	N	H
d 9	P	J
d10	R	K
130 V	S	S
	T	T
d19 (x)	W	L
d20 (y)	W	M
Clutch coil	X	P
Cam	Y	V
H.T.	b	b
Earth	d	d
	a	a
	F	N

OUTPUT DRIVER

Cables P86-1A, P86-1B to Tag Strip

P86-1B

Output Driver	Tag Strip	Digit	26 Pin on Output Reg	Neon Plug
1	236	19 (x)	L	V
2	237	20 (y)	M	W
3	245	Punch clutch		
6	231	6	F	L
7	232	7	G	M
8	233	8	H	N
9	234	9	J	P
10	235	10	K	R
12	26	Punch H.T. On Sw		
4	243		U	

P86-1A

1	226	1	A	A
2	227	2	B	B
3	228	3	C	C
4	229	4	D	D
5	230	5	E	E
12	27	Teleprint On Sw		

6. CARD PUNCH CONTROL

6.1 Circuit ..... shows the punch control relays and also the wiring in the Hollerith punch unit.

6.2 When a (card) punch signal is received from the Output Control Unit relay RY 10 operates and locks in.

6.3 Any digits in the output register flip-flops close the corresponding digit relays RY 0 to 9, y, x.

6.4 When RY 10 closes, RY 11 closes after a delay and releases RY 10. We will assume that both RY.x and RY.y have not been operated. RY 10 closing resulted in the appropriate holes being punched.

6.5 RY 11 closing operates the racking magnet. At the end of the rack RY 11 opens and sends a card punch ready signal to the computer via pin V and relay H in the teleprinter control chassis.

6.6 RY 10 closing also operates RY 10a.

6.7 RY 10a closing applies voltage to RY 13 through a delay network and in the event of RY 10 remaining closed too long, RY 13 will close and remove voltage from the key magnet and racking coils.

6.8 The release of RY 10 and hence of RY 10a results in a clearing signal being sent to the computer output register.

6.9 When RY.x and RY.y are closed together the operation is different as this punching requires the card to be ejected and a new card fed.

6.10 RY.x and RY.y together close relay RY 12 which locks in.

6.11 RY 12 closing shorts terminal V to ground and prevents a punch ready being sent until the new card is fed along to the end of its travel. At the end of the new card feed RY 12 is released and sends the ready signal in the normal manner.

6.12 At the end of the racking out of the old card relay RY 10 is released having been locked in through contacts on RY.x and RY.y and the last column contact on the punch.

The card is ejected by means of a mechanical interlock system on the punch. This requires that the key punches x and y and the racking magnet be held down until the ejection is finished. It is also necessary that the x and y punches be operated before the racking magnet as otherwise the mechanical interlock does not function.

6.13 The relay mounted on the punch is operated by the NO CARD contact. When a new card is not fed this relay operates and prevents the relay RY 12 opening. The computer therefore does not receive a "ready" signal.

SECTION DD

POWER SUPPLIES

Circuit Drawings

Power Supply Cabinet No.1 wiring: B19620

Cabinet No.2: B21057

Regulated 300-0-300 Volts: SKE4232

Shunt Regulator for 300 Volts: SKE

1 The meters M1-M6 in cabinet 1 indicate % variation from the correct voltage. The power supplies are adjusted to the required voltage and the potentiometers R4, R9 etc. adjusted to give zero reading on the meter.

The diodes prevent the meters drawing excessive current during switching on or in the event of the failure of the supply voltage.

2 The supplies in the cabinet are conventional and need no description.

3 Cabinet 2 contains regulating reactors and control circuits for the Memory and Main 210 volt and filament supplies.

The D.C. current through the reactors is shown on front panel meters. The operating range of the 807's for the H.T. reactors is 0 to 70 mA and for the filament reactors is 0 to 140 mA. The transformer taps should be adjusted so that the normal operating point is about the centre of the range.

Fig. 1 shows test results on one of the H.T. supplies.

4 The input to the computer is 3 phase with the maximum load approx. 30 amps per phase.

5 The D.C. supplies available are shown below:-

(a) Cabinet No. 1

210 Volt	10 Amp	2 supplies
270 Volt	3 Amp	(nominal 300 Volts)
+300 Volt -300 Volt	100 mA	for % error meters
- 30 Volt	0·3 A	
- 60 Volt	2·4 A	
-100 Volt	0·5 A	not used
50 Volt		for relay supply

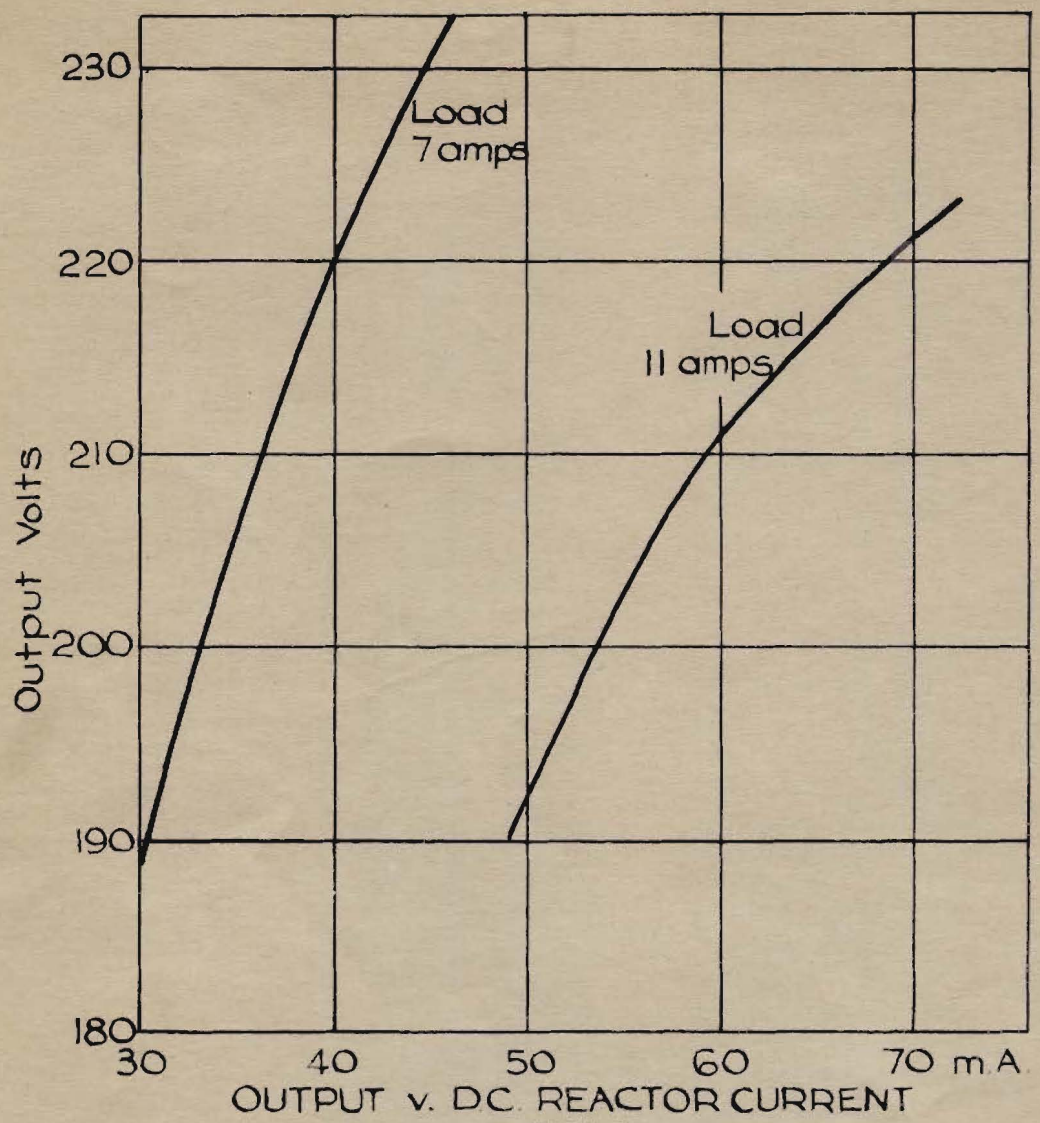
(b) Cabinet No. 2

-250 Volt	0·5 Amp	
-100 Volt	1·2 Amp	
30 Volt	2·4 Amp	Drum motor
250 Volt	0·5 Amp	for Reactor supply
130 Volt	6 Amp	for Uniselectors, Hollerith Punch and Editing equipment

6 The 270 Volt 3A supply has a shunt regulator connected (mounted in No. 2 memory cabinet). This reduces the fluctuations which occur when reading into different line positions. Fig. 2 shows the voltage of the supply with and without the regulator connected.

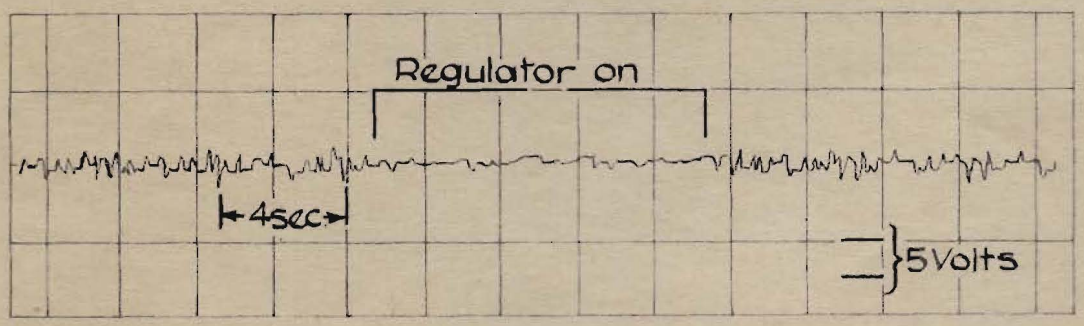
PIPE ON 270V SUPPLY

KEEPS MOLE NO STARTS



OUTPUT v. D.C. REACTOR CURRENT

FIG. 1



RIPPLE ON 270 V SUPPLY

FIG. 2

RPL 99

SECTION JJ

VALVE TESTER

Circuit: B22579

1. Valve types
2. Mains Voltage
3. Test for Shorts
4. Cathode to Filament Leakage
5. Plate Current
6. Mutual Conductance
7. Cut-off Bias
8. EA50 Diode Test
9. Germanium Diode Test.

1 **Valve Types**

The tester was designed for checking particular types of valves and diodes used in large numbers in the computer.

The types which can be tested are 6SN7, 6V6, KT61, 6AC7, 6SJ7, EA50 and Germanium diodes type CG1-C, CV425, CV488.

In order to save time, separate sockets are available for each type of valve so that there is no need to set up a bank of switches.

2 **Mains Voltage**

The tester should be connected to a small variac in order that the AC volts can be set to the correct value. Input AC current to the unit is amps.

The table below shows the effect of filament voltage in the IA and Gm as measured on a G.R. Valve Bridge.

Fil. Volts	Fil. Current	IA	ISc	Gm
5·0	0·4	7·0	1·7	8·5
5·25	0·41	7·8	1·9	8·9
5·5	0·42	8·2	2·0	9·1
5·75	0·43	9·0	2·2	9·4
6·0	0·44	9·4	2·3	9·7
6·25	0·45	9·9	2·45	10·0
6·5	0·46	10·6	2·55	10·6

Isc.

3 **Test for Shorts**

A valve can be tested for shorts, but without filament volts, in socket 6. H.T. is applied to each pin in turn with all other pins connected together and to ground. (switch S4). A resistor limits current to 1mA (reads 50) and is

indicated on the "Bias" meter. S2 must be set to IA or Gm.

4 Cathode to Filament Leakage

The leakage resistance is indicated on the "Bias" meter when the valve is plugged into any of the test sockets 1 to 7.

5 Plate Current

Set S1 to valve socket used, S2 to IA. Plate current is measured as percentage of book value. Grid bias is zero and plate voltage 150 volts. The resistors R1 to R6 were adjusted to give the correct value with the plate loads shown.

The effect of gas current may be estimated by pressing the "GAS" button. This switch puts a resistor of 1 megohm in the grid circuit.

6 Mutual Conductance Gm

Set S2 to Gm. An AC voltage of 1·0 volts RMS. is applied to the grid (with zero bias) and the output voltage is measured through an amplifier. The gain of the amplifier may be checked by pressing the "Gm test" button when the Gm meter should indicate 100 per cent. If required the amplifier gain may be adjusted through a hole in the side of the case.

7 Cut-Off Bias

Set S2 to "CUT OFF" and adjust bias control knob to give zero plate current. The "BIAS" meter reads the cut-off voltage.

8 EA50 Diode Test

Cathode to filament leakage is indicated as in 4 above. Set S1 to 7, S2 to Gm, and S3 to "FORWARD". 1·0 volts RMS

is applied to the diode, and the IA meter indicates the percentage of the correct value of rectified current.

Set S3 to Reverse. 50 volts is applied in the reverse direction to the diode and the back resistance is indicated on the IA meter.

9 <u>Germanium Diode Test</u>

Similar to 8 above.

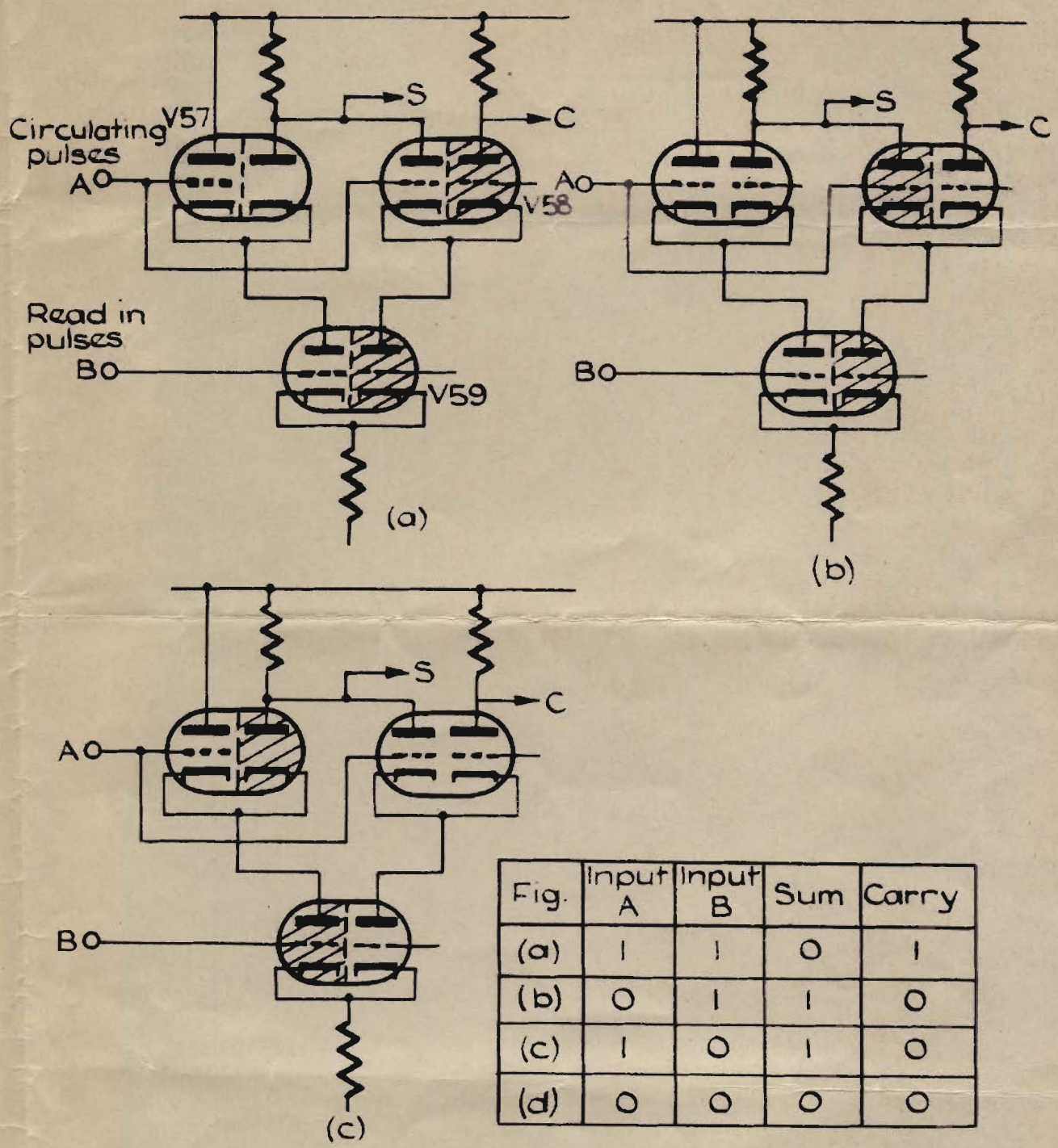


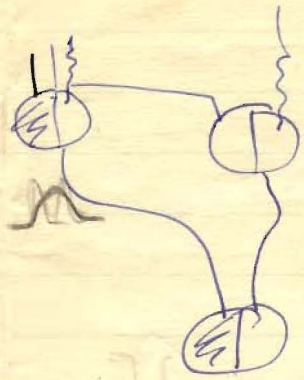
Fig.	Input A	Input B	Sum	Carry
(a)	1	1	0	1
(b)	0	1	1	0
(c)	1	0	1	0
(d)	0	0	0	0

FIG. 4

RPL 99

A No Input.

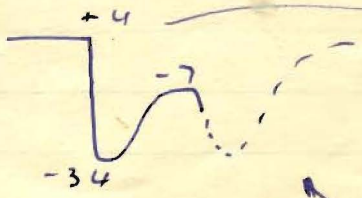
No current flowing as shown by the shaded sections.



No current thru' V3 or V2b as V2b cut off by -11 even at top of clock cathode say +4V

B Neg pulse at B

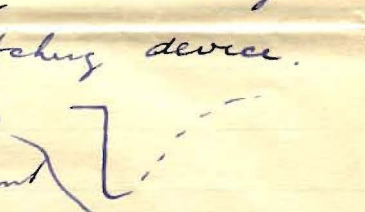
This cuts of V2a (x) and its cathode falls down by ≈ 38V when clock pulse arrives the cathode goes up again but not so far as before.] (x) this is to cut off rather - it is cutoff a fraction later when clock pulse hauls up cathode



assuming -4V bias on tubes.

and on cathode The current that was flowing before in V1a now switches over to V3a Think of circuit as essentially a current switching device. This current flows thru' R1 and produces

C neg pulse at A + B.

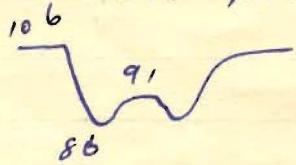


In this case current gets pushed over to 2nd half of V3 as V3a cut off & our output pulse is developed across R2

D neg pulse at A

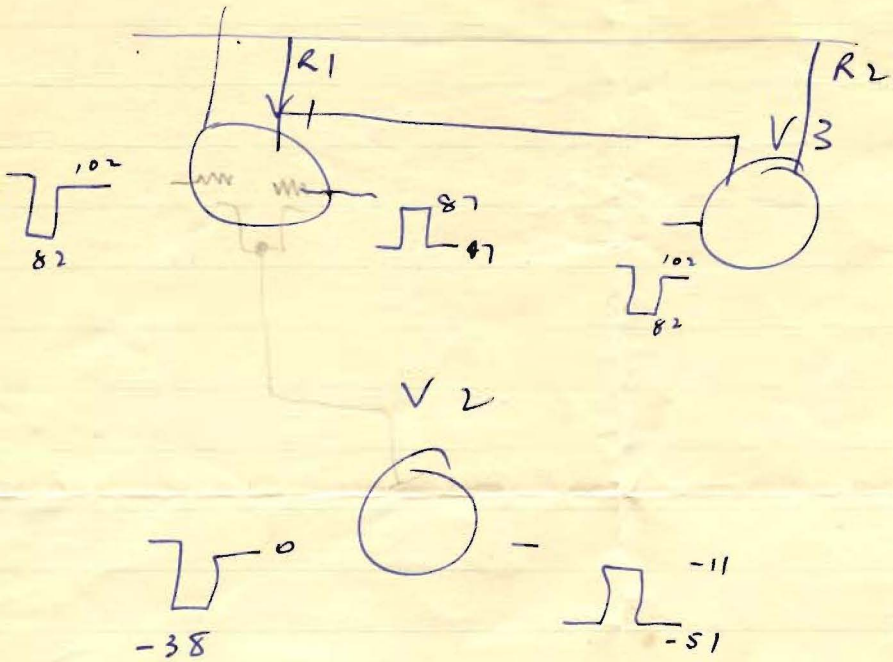
V2a remains conducting & the current is pushed from V1a to V1b as the former is cut off (x) -

The cathode V1 probably behaves much the same as V2 cath. ie

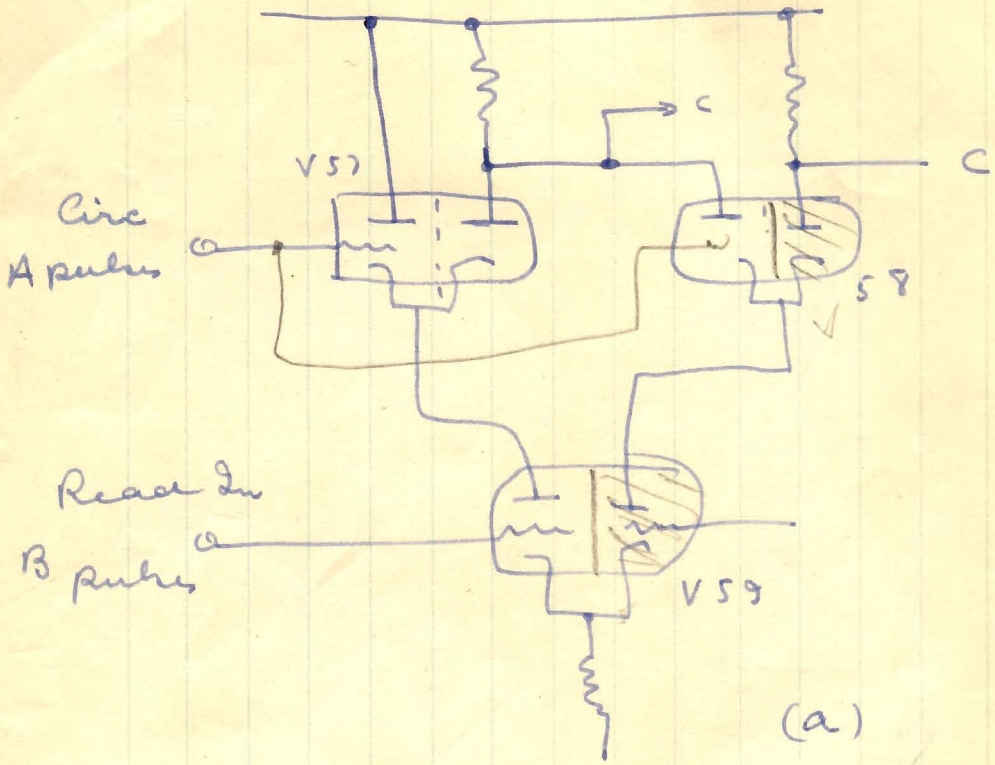


although would not expect spikes as big Off CRO capacitis affect things a lot.

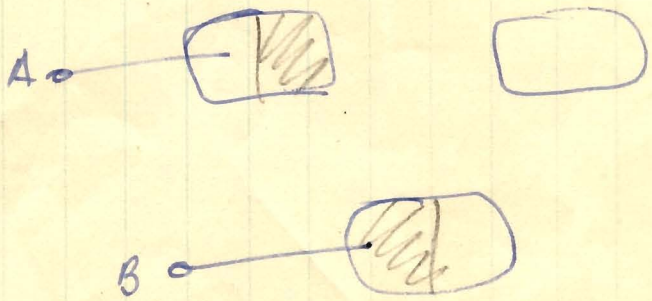
Would not expect any spike on V3 cath as the current flows only during the clock pulse (ie via V2b) Design possibly originally in ACE

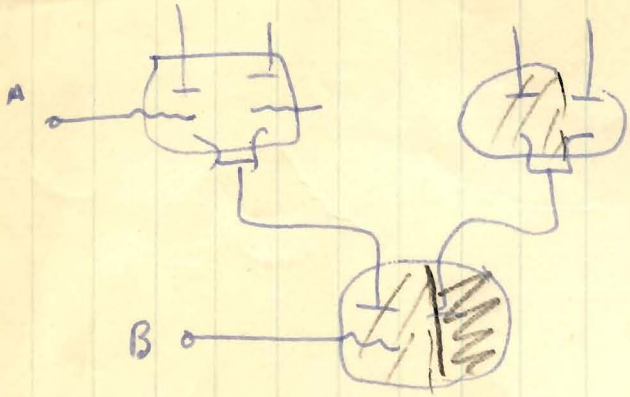


80



(a)





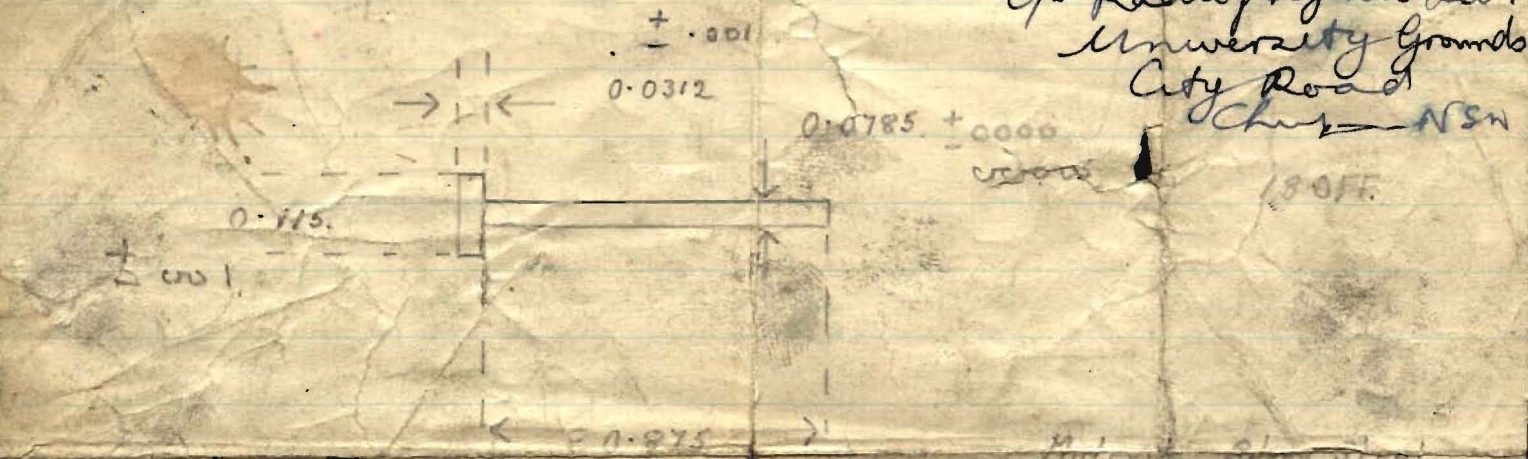
(b.)

Fig	Input A	Input B	Sum	Carry
a	1	1	0	1
b	0	1	1	0
c	1	0	1	0
d	0	0	0	0

FIG 4

Radiophysics

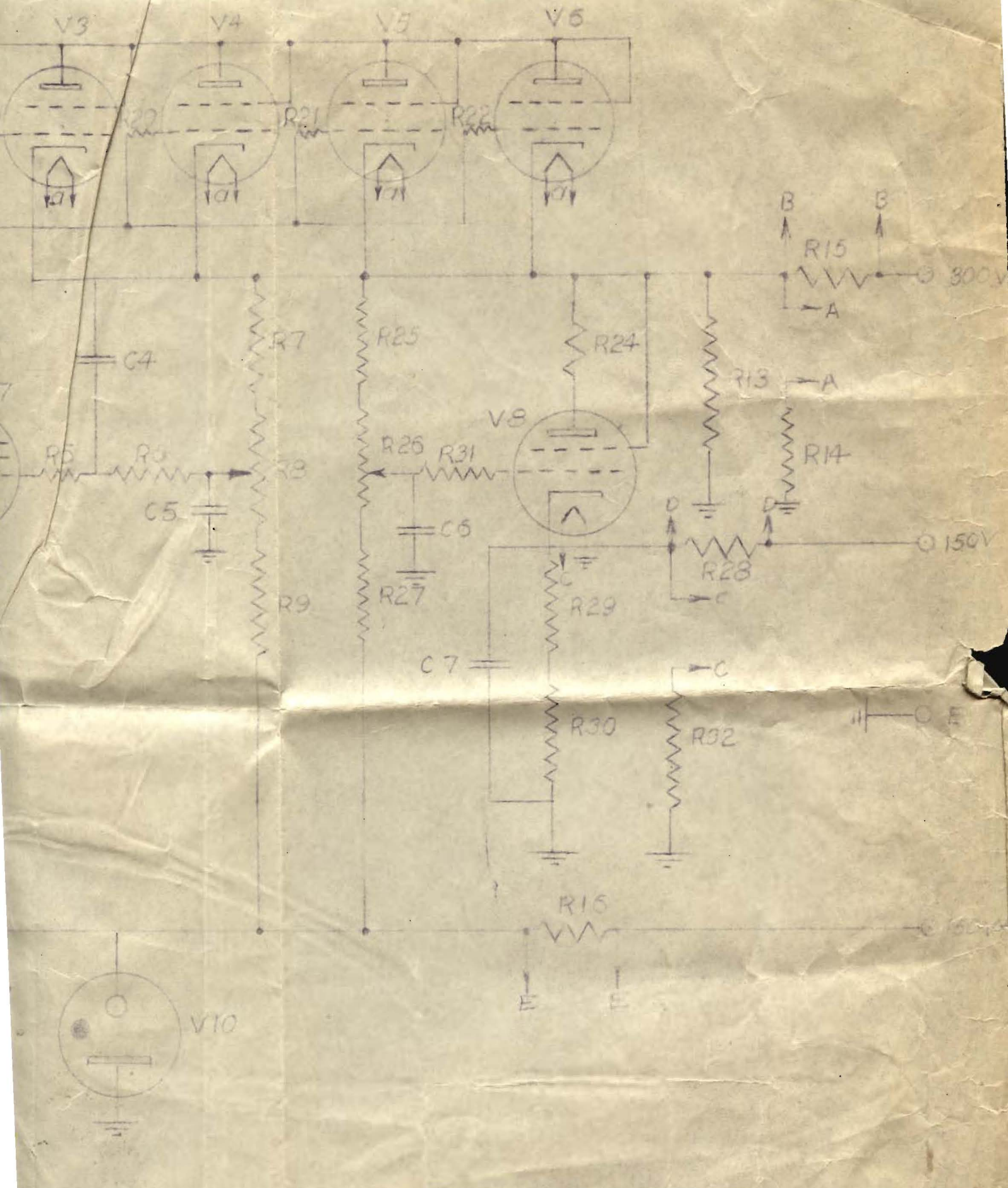
J M Beard
MW2484.
c/- Radiophysics Lab.
University Grounds
City Road
Chippendale NSW



Material M.S

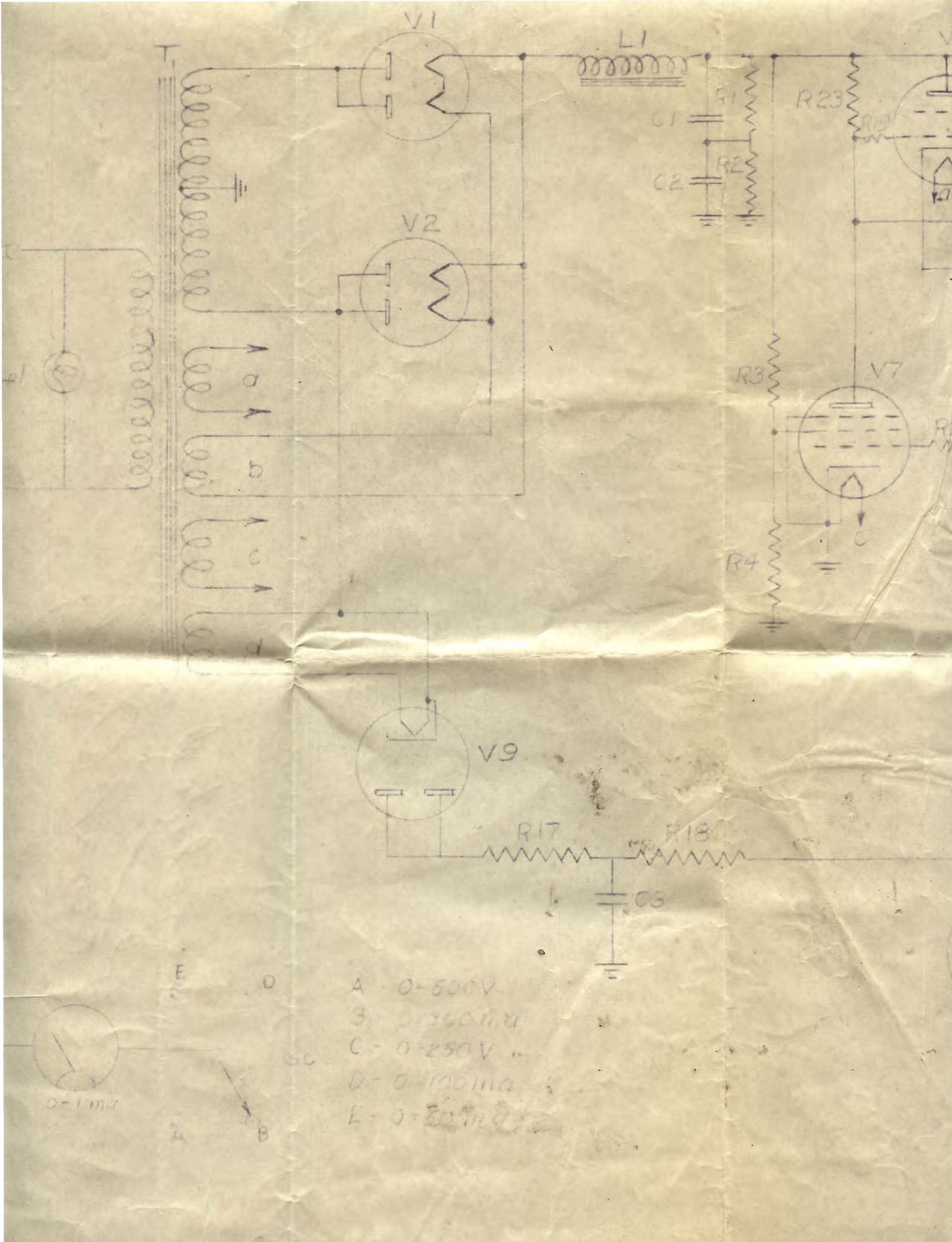
2-off Combs. Grind to $\frac{1}{16}$

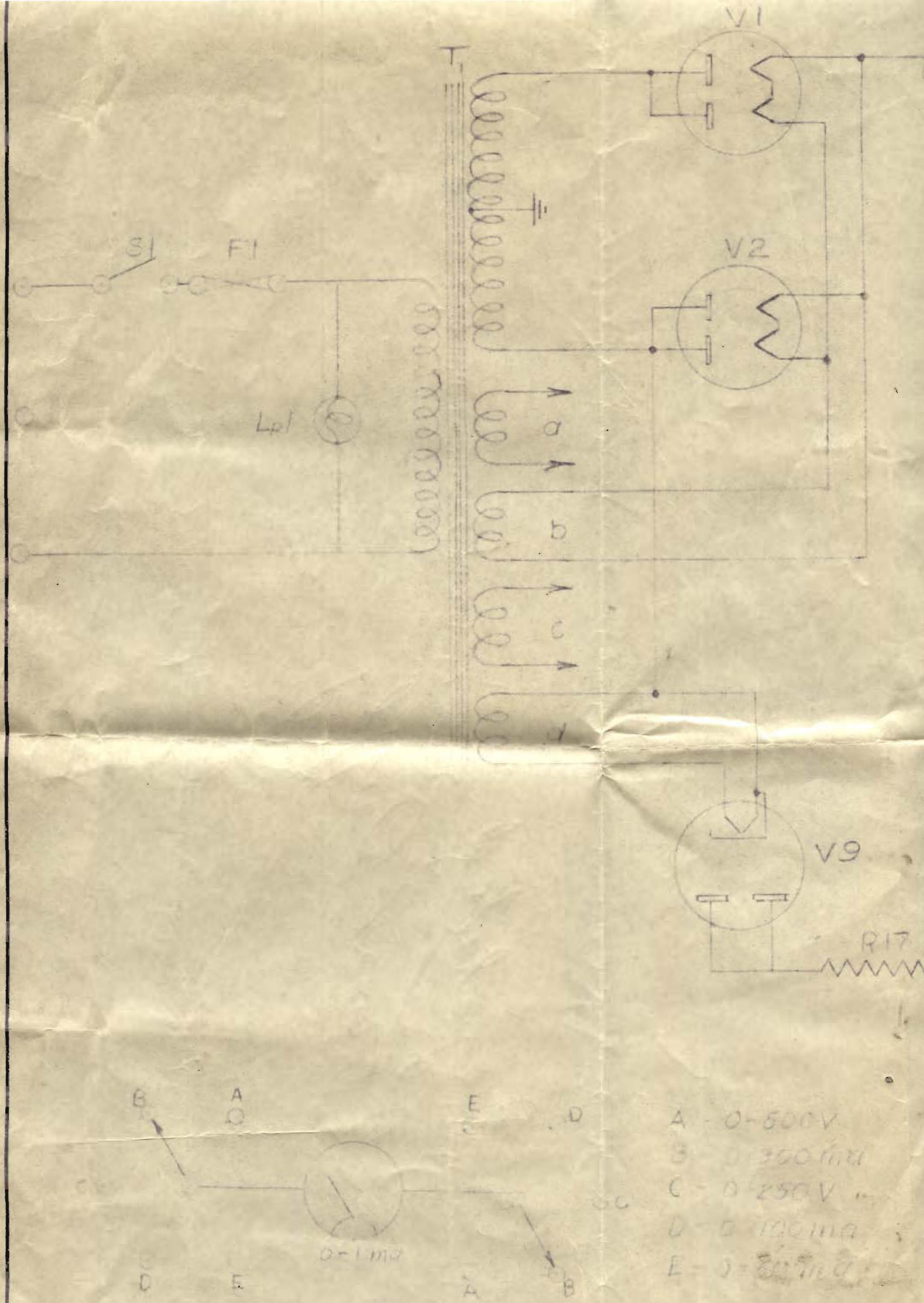
N577



C.S.I.R.
RADIOPHYSICS LABORATORY

REGULATED POWER SUPPLY


V1
V2
T1
L1
C1
C2
R1
R2
R23
R3
R4
V7
a
b
c
d
V9
R17
R18
C3
E
D
B
0-1 ma
A - 0-500V
C - 0-250V
D - 0-100ma


V1
T1
V2
S1
F1
Lp1
a
b
c
d
V9
R17
B
A
E
D
0-1 ma
D
E
A
B
A - 0-500 V
B - 0-300 ma
C - 0-250 V
D - 0-100 ma
E - 0-30 ma