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A Magnetic Drum Digital Storage System

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Summary.

A magnetic drum storage system for an electronic digital computer, having a storage capacity of 1024 "words" of 20 binary digits, is described. Data are read in or out, word by word, with an average access time of 5 milliseconds. Basic circuits are included.

1. Introduction.

(*a*) *Digital computer principles.*

The development of electronic digital computers has been conditioned largely by the availability of suitable forms of storage for the data being handled. While it is not within the scope of this paper to describe the working of a complete computer, it will serve as a useful starting point to consider the role played by the store in an elementary machine.

An automatic computer takes over numerical calculating work which would otherwise be done by a human operator manipulating a standard desk calculator. The possibility of mechanizing such calculations arises because, no matter how complex a problem may appear initially, it can always be reduced to a predetermined sequence of simple arithmetical operations. It is therefore possible to devise an automatic operator to replace the human operator mentioned above. The use of an automatic computer becomes especially valuable when the problem involves hundreds or even thousands of repetitions of the same sequence of operations, each sequence being started with slightly different initial data.

For the realization of an automatic computer the following basic equipment is required.

1. A storage system to hold the problem data.
2. An arithmetical unit which is capable of adding, subtracting and multiplying numbers.
3. An input device.
4. An output device, i.e., printer.
5. Means for transmitting numbers into and out of the above devices.
6. A sequencing unit. This can be envisaged primarily as a stepping-switch-cum-plugboard which can connect the above units together in pairs according to a sequence or "programme" worked out to suit the problem in hand.

The mode of operation of such a machine can be explained most easily by considering the solution of a specific problem. Suppose, to take a very simple example, it is desired to calculate a table of the function $y = x^2$ with x taking the values 0.1, 0.2, 0.3, . . . It is assumed that the arithmetical unit is equipped with registers† termed A, B, C and D; A is an adding register, and B, C and D are used for multiplication. In multiplication, the multiplicand is set into the B register and the multiplier into the C register whereupon the product is generated automatically and appears in D. In this simple example the store, which should have a large number of "compartments" to take care of general requirements, is required merely to hold the value 0.1 representing the increment of x. Let this value be placed in store compartment 1. Then the plugboard will be set up so that when the stepping switch is started the following transfers are executed cyclically.

	Step No.		*Transfer effected*	*Result*
Repeat	1	Contents of store compartment 1	→ Added into A register	A register holds current value of x
	2	Contents of A register	→ Read to B register	x inserted as multiplicand
	3	Contents of A register	→ Read to C register	x^2 formed as product
	4	Contents of D register	→ To printer	x^2 printed.

Note: All registers are cleared before starting the machine.

Although the input unit does not appear in the above cycle it will have been used initially to load the store.

While some machines have in fact used a plugboard-sequenced system, a much more flexible scheme has become almost universal in present day designs. In these machines the information represented by the plugboard connections is coded as a sequence of numbers termed "instructions" which are inserted in the store. When the machine is started these instructions are transmitted one by one to a decoder which sets up connections to secure the same result as the original stepping switch. The flexibility of this system arises from the fact that, although instructions and ordinary numerical data are normally kept separated in the store, it now becomes possible to operate on instructions in the arithmetical unit during the course of the calculation. This causes the machine to vary its sequence of operations as it works.

The foregoing remarks show that each programme step involves extracting an instruction from the store, decoding it, and then carrying out the specified operation, which may itself involve the store. Thus access time to the stored instructions is an important factor determining machine speed while access time to other stored data is of greater or lesser importance depending on the nature of the individual calculation.

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†In computing practice the term "register" describes any device which is capable of holding the digital representation of a number, e.g., the assembly of toothed wheels in a desk calculator.

(*b*) *Storage principles.*

Organization of a computer storage system is usually facilitated by expressing numbers in the binary scale so that all digits take the value 0 or 1.** Any electrical device exhibiting two-state characteristics can then be used for storage of a binary digit. However, modern computers require storage for tens of thousands of digits and not many storage principles can be economically applied on such a scale. Thus the familiar Eccles-Jordan flip-flop‡ is an excellent fast-acting device for storage of a binary digit, but expense precludes its use for anything but specialized functions in a computer.

On the other hand, in a magnetic drum storage system, a binary digit is represented by a localized magnetic impression recorded on the specially-treated surface of a rotating drum. Recording is done by a head which can imprint two types of magnetic impression to represent 0's and 1's, and by the use of a multiplicity of heads several hundred digits can be stored on each square inch of surface. Thus a very large number of digits can be stored in a small space. In addition, a comparatively modest amount of auxiliary electronic equipment is required to operate the store. Another very important advantage possessed by magnetic drums is " non-volatility " of the stored information, meaning that the latter is not lost when the equipment is switched off. This feature is especially important in a high-capacity store since it saves time which would otherwise be wasted in reloading the store when data is to be used over an extended period. On the debit side the access-time for random store references may be anything up to one complete drum rotational period, and because of mechanical limitations this time is inherently much longer than can be attained with other high-capacity systems employing electrostatic storage tubes or supersonic delay lines.[1] Because of their short access time the latter two systems have advantages for the storage of instructions or other operands which may need to be dealt with at high speed. However they are " volatile " in nature and are much more expensive to build than magnetic drums.

The magnetic drum storage system which is described in the following sections was designed as an auxiliary store for the C.S.I.R.O. Mk. I Electronic Computer.[2] This computer was already in operation with a mercury delay line storage system and the magnetic drum was added to provide additional storage capacity for problems of the type discussed in Appendix I. It has a capacity of 1024 words* of 20 binary digits (approximately equivalent in precision to 6 decimal digits) and its rotational speed of 6000 RPM gives it an access time on the average of 5 milliseconds for random references. It has served as a pilot model for a drum of 4096 words capacity which is now nearing completion.

2. The Experimental Magnetic Drum.

Figure 1 is a photograph of the experimental magnetic drum. The rotor has a diameter of $4\frac{1}{2}$ inches and a length of 3 inches. Motive power is provided by an internal DC motor which was taken from an aircraft gyroscope. This motor provides quiet running at a speed of 6000 RPM.

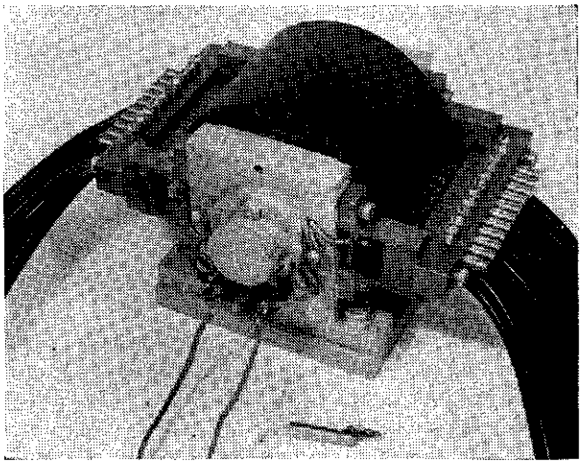

Figure 1.—*Photograph of magnetic drum.*

A coating of commercially-prepared magnetic iron oxide lacquer is sprayed on to the surface to serve as a recording medium. This coating was adopted because of the high value of its figure of merit H_c/B_r, where H_c = coercivity and B_r = remanence. The latter figure of merit is well known in sound recording work and its application to digital recording can be seen from the following qualitative reasoning. Binary digits are recorded on the drum in terms of localized magnetic impressions and in endeavouring to increase digit packing densities a point is reached where the stray flux from one region tends to demagnetize an adjacent region. The onset of this effect is delayed if the recording medium has a high coercivity and if the stray flux, measured roughly by B_r, is low. Owing to the very short magnetic dipoles employed here the effective remanence is much less than the conventional value of B_r which applies to closed magnetic circuits, but the ratio H_c/B_r is still a good guide to performance of the recording medium. Thus the oxide coating as used here, having $H_c = 280$ oersteds and $B_r = 550$ gauss was found to be usable at twice the digit packing density which would be used with plated nickel ($H_c = 20$ oersteds, $B_r = 2000$ gauss).

The drum surface is divided into 21 tracks each served by a " head " which functions for both reading and recording. For reasons of mechanical convenience the heads are mounted in two staggered rows. Of the 21 tracks 20 can have numerical data recorded on them and the 21st holds a permanently recorded timing waveform (clock track). Each track is divided into 1024 storage cells,

**For example the decimal number 19 is transformed in the binary scale to $10011 \equiv 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$.

‡The term flip-flop here implies a bistable multivibrator.

1. Engineering Research Associates Inc., " High Speed Computing Devices," Chapter 14, McGraw-Hill, New York, 1950.
2. Pearcey, T. and Beard, M., " An Electronic Computer," Jour. Sci. Inst., **29**, No. 10, Oct., 1952, p. 305.

*The term " word " is often used to cover both instructions and ordinary numbers.

spaced 75 per inch, which are defined by the intervals of the clock track and are identified by counting from a small gap between start and finish of the clock track. The cells can be selectively magnetized to either of two polarities representing the digit 0 or 1. The 20 digits making up a number are recorded simultaneously in the 20 tracks and are therefore spread in a row across the drum. This general scheme of "parallel" recording has been described previously by Booth[3] and Cohen.[4]

As the computer itself operates in the serial mode, that is numbers are transmitted as trains of digits on a single circuit, it might seem preferable to have adopted the serial mode also for the magnetic drum, and to have made use of the computer timing facilities by adopting a synchronous system of the type developed by Williams.[5] A digit train would then be transmitted directly into a selected track leaving a magnetic pattern spread over a selected portion of the periphery. However it was considered that development of a synchronous system would be more time-consuming and would not result in any appreciable saving of equipment over the present system which uses an unsynchronized drum and a static buffer store for holding numbers temporarily during transfer. The static buffer store has permitted the adoption of a parallel-working drum with the simple writing and reading circuits described in Section 4.

3. Recording Method.

The manner of recording digits in a track is illustrated in Figure 2 which shows a diagrammatic cross-section of a track and its recording head. A recording head consists of a single strip of .003 inch mumetal bent to shape and carrying a 100 turn magnetizing winding of 36 B and S wire. Pole tips are separated by a .001 inch non-magnetic spacer and a clearance of .0015 inch is maintained between the head and the drum. Operation in contact is not possible because of the high peripheral speed.

The recording circuits which are described in detail in Sub-section 4 (c) employ thyratrons which can be switched to deliver to each head either a positive pulse when recording a 0 or a negative pulse when recording a 1. The pulses are approximately a half sinusoid in shape and have a peak amplitude of 1 ampere and duration 1 microsecond. Motion of the drum during the latter interval is negligible and in consequence a small area of the magnetic coating immediately adjacent to the recording head gap is magnetized to saturation. The use of pulses which are always of saturation intensity ensures that new data automatically supersede previously recorded data without the intervention of a special erasing operation. The recording thyratrons can only be triggered at instants when the head is centred on a cell, triggering being performed by a "position selector pulse" derived from the unit described in Sub-section 4 (a).

3. Booth, A. D., "A Magnetic Digital Storage System," Electronic Engineering 2, 1949, 234-238.
4. Cohen, A. A., "Magnetic Drum Storage for Digital Information Processing Systems," Math. Tables and Aids to Computation IV, January, 1950, p. 31.
5. Williams, F. C. and West, J. C., "The Position Synchronization of a Rotating Drum," Proc. I.E.E. 98, Part II, 1951, 29.

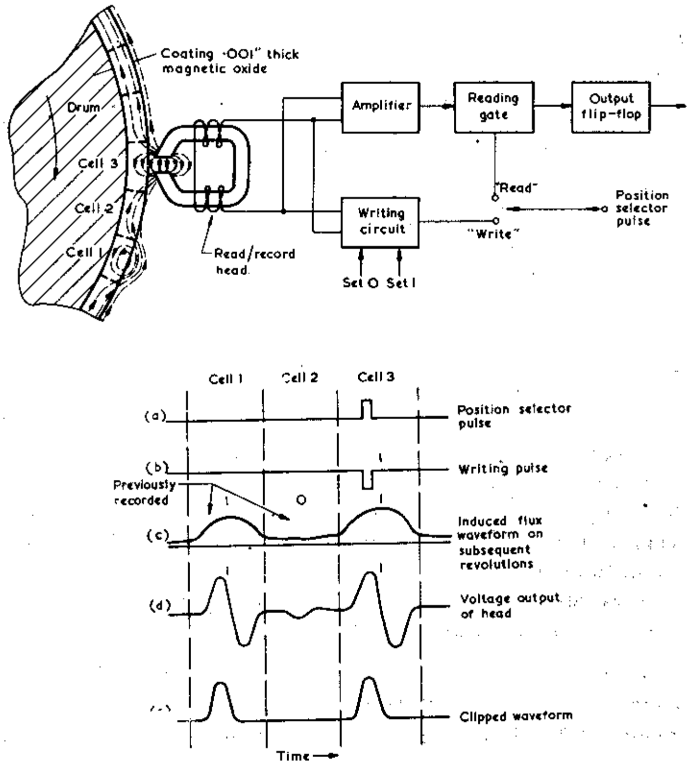

Figure 2.—Cross-section of drum and recording head. The basic units involved in reading operations and the method of representing digits are also shown.

So far it has been implied that the medium is initially in a magnetically neutral state and that the recording process imprints magnetic dipoles in the cells with one polarity representing 0 and the other representing 1. However, it has been found advantageous to adopt a slightly different scheme in which the coating is initially magnetized uniformly in one direction. This is achieved by passing DC of positive polarity and saturation intensity through the heads while the drum is rotating. The coating is then said to be "uniformly magnetized to the 0 state." If now a 1 is recorded in a cell such as cell 1 or cell 3 of Figure 2 the magnetism is locally reversed and the residual flux density in the region immediately adjacent to the cell thus treated is double the value which would result from simple dipole recording. This means that the EMF induced in the head during reading operations is also doubled. Recording of further 1's in a cell already holding a 1 has a negligible additional effect, but recording a 0 restores the residual magnetism approximately to its initial state.

The basic units involved in reading operations are also shown in Figure 2 and consist of an amplifier, a reading gate, and an output flip-flop. Figure 2 (c) shows the flux waveform induced in the head by the passage of three cells holding digits 1, 0, and 1. The voltage output of the head being proportional to the time derivative of the flux wave has the shape shown in Figure 2 (d). After amplification and clipping the waveform of Figure 2 (e) is produced. (The amplifier is, of course, strongly overloaded by a writing pulse but it recovers full sensitivity in less than 1 millisecond, well before any subsequent reading operation may be called for.) The clipped waveform is now applied to one input of the reading gate which is a coincidence type requiring two simultaneous input pulses in order to generate an output pulse. In reading the content of a cell the position selector pulse is phased appropriately, as for example in Figure 2 (a), and is switched to the second input of the reading gate. Thus an output is developed by the gate only if the selected cell contains a 1. This pulse is used to set the output flip-flop to the 1 state.

An oscillographic record of the output waveforms resulting from various digit configurations is shown in Figure 3. The first waveform shows a pair of isolated 1's recorded on the medium immediately after it has been uniformly magnetized. Next, additional 1's are recorded to make a block of five 1's spaced at 75 per inch. In the final two waveforms the 1's are overwritten by 0's to show the magnitude of the residual 0 signal. Tests have shown that this signal does not change noticeably in shape and magnitude even after 10^6 reversals of the cell content. The waveforms correspond to a peak to peak output from the head of 5 millivolts.

Other more intricate methods of digit representation have been described, based on " pulse envelope " principles which permit much higher digit packing densities (see for example Cohen and Keye[6]). A pulse envelope scheme was tried in the early developmental stages but was found to require rather critical circuit adjustments. Consequently, the method described here was adopted on the grounds of its greater simplicity and reliability.

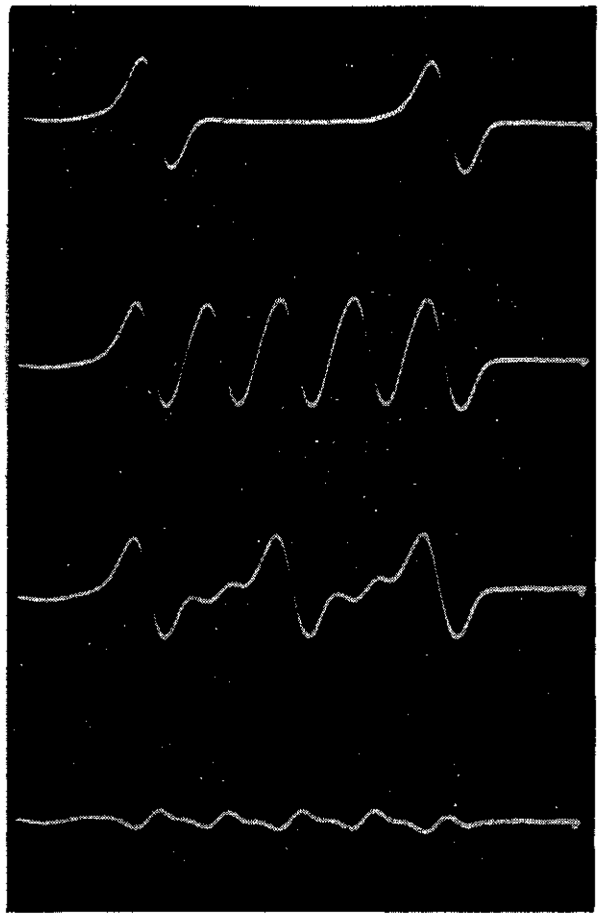

Figure 3.—Oscilloscope waveforms.

4. Auxiliary Electronic Equipment.

A block diagram of the equipment necessary to operate the magnetic drum in conjunction with the computer is shown in Figure 4. This comprises an amplifier unit, input unit, output unit, position selector unit, and drum sequence unit. The basic functions provided by these units are as follows:

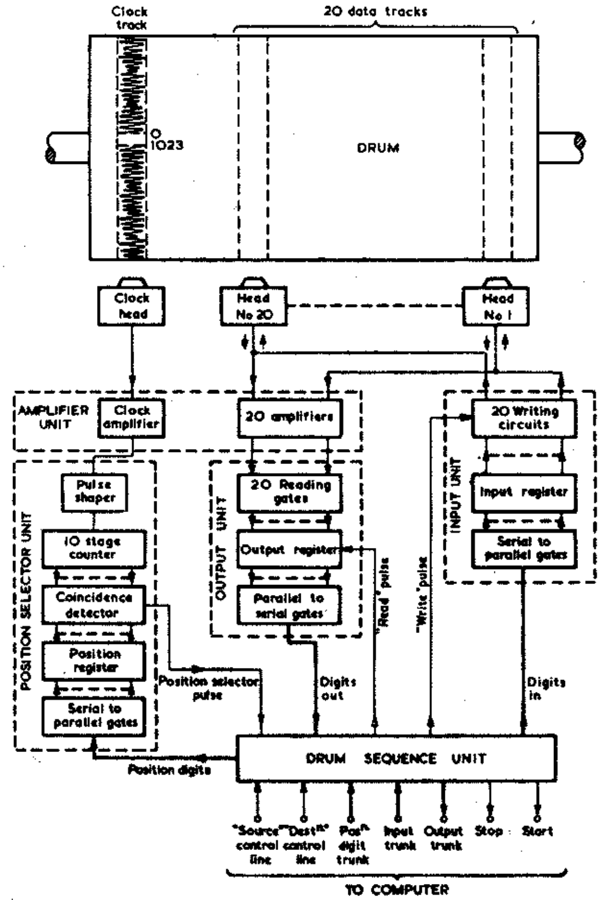

Figure 4.—Block schematic of electronic equipment.

The input unit contains a static register employing 20 flip-flops in which a number to be recorded is held while awaiting the passage of the desired recording position past the heads. Since numbers are transmitted from the computer in the form of a serial train of digits, a " serial to parallel " gating system is used to read the digits into the input register. This gating system is described further in Sub-section 4 (c). The static register prepares a row of recording thyratrons to deliver the appropriate positive or negative pulses to the heads.

6. Cohen, A. A. and Keye, W. R., " Selective Alteration of Digital Data in a Magnetic Drum Memory," Proc. I.R.E. Convention, March, 1948.

The position selector unit contains a 10 stage binary counter which counts the intervals of the clock track starting from zero in the clock-track gap. Opposite the counter is a 10 digit position register in which the serial number of a desired storage position is placed (10 binary digits can specify 1024 different positions). Equality of the contents of the counter and register is detected by a coincidence circuit which emits a pulse (the position selector pulse) each time the desired position passes the heads.

The purpose of the amplifier unit is self-explanatory. It is connected to the output unit which contains a row of 20 reading gates, a 20 digit output register and a set of parallel to serial gates.

Contact with the computer is established through the drum sequencing unit which acts in conjunction with the main computer sequencing unit to determine the correct sequence of operations whenever a drum transfer is called for. For an understanding of the functioning of the magnetic drum storage system it is not necessary to go into details of the functioning of the computer itself. These details may be found, if required, in reference 2. It will suffice to state here that all units of the computer receive data on a common trunk line called the "input trunk" and transmit data outwards on an "output trunk", the two trunks being electrically joined at suitable intervals. The particular pair of units which are to transmit and receive at any instant is determined by the control unit which energizes a particular pair of control lines called the source and destination lines. In the case of a reference to the store a 10 digit number specifying the particular store position involved is also transmitted on the "position digit trunk".

Whenever a transfer to the drum is called for, the following cycle of events occurs:

1. The "drum destination" control line is energized by the computer controls.
2. All drum registers are cleared to zero (clearing lines not shown on diagram).
3. The position digits are transmitted to the position register.
4. The number appearing on the input trunk is passed to the input register.
5. The computer sequencing unit is stopped.
6. On receipt of the next available position selector pulse a trigger is sent to the writing circuits. (Depending on the rotational phase of the drum this may occur any time up to 10 milliseconds after setting up the input register.)
7. The computer is restarted and the computer controls de-energize the drum destination line.

Similarly, when a transfer out of the drum is called for, the following sequence of events takes place.

1. The "drum source" control line is energized by the computer controls.
2. The drum registers are cleared.
3. The position digits are transmitted to the position register.
4. The computer sequencing unit is stopped.
5. On receipt of the next available position selector pulse the reading gates are opened allowing the contents of the desired position to enter the output register.
6. The computer sequencing unit is restarted.
7. The contents of the output register are transmitted to the output trunk.
8. The drum source control line is shut down when the transfer to the desired destination is completed.

In the following sections some circuit details, which are of general interest, are given. As the circuits of the drum sequencing unit cannot be readily described without going into details about the computer itself, that particular unit will not be described further in this paper.

(*a*) *Position selector unit.*

Before passing to a description of this unit it will be necessary to give a few details of time relationships applying in the Mk. I Computer. Digits making up a number are transmitted at a spacing of 3 microseconds. The least significant digit designated d_1 appears first on the digit trunk and the most significant designated d_{20} appears last. Thus a complete number is transmitted in 60 microseconds. For reasons connected with the coding of instructions in the machine, the 10 digits making up a store position reference are transmitted in the d_{11} to d_{20} positions but in this case the d_{11} digit is considered to have unit value.

Figure 5 shows the basic circuit of the counter and position register. Input from the clock track amplifier is in the form of a train of square waves obtained by operating the last stage as a limiting amplifier. The wavetrain is repeated once each drum revolution and contains 1024 waves of 9.7 microseconds period with a gap of about 150 microseconds between start and finish. The negative-going edges of the waveform are used to trigger a blocking oscillator V1A which generates a train of clock pulses. In addition a train of clock pulses delayed by 6 microseconds is available at the output of the delay line DL1.

A second blocking oscillator V2B is normally cut off by rectifying the clock pulse train using diode V2A. However, the diode load R1C1 has a time constant such that the bias on V2B decays to zero in the 150 microsecond gap allowing V2B to execute a single oscillation. A positive pulse of some 5 μsec. duration is then generated across the cathode resistor of V2B and serves as a counter zeroing pulse. The counter is of conventional design and employs 10 flip-flops identical with V4 and 10 interstage buffer diodes identical with V3 to ensure that each stage is triggered only by the negative-going edge of the waveform at the plate of the previous stage. The left-hand grid returns of the flip-flops are connected in common to the counter zeroing pulse lead so that the counter is cleared to zero in the clock track gap and goes through a complete binary count 0000000000 to 1111111111 i.e., 0 to 1023 during each revolution.

Opposite the rows of counter flip-flops there is another row of 10 flip-flops identical with V6 which constitute the position register. At the start of a transfer this register is cleared to zero by a pulse on the common grid return line. The incoming train of 10 position digits is separated out by a row of 10 serial-to-parallel gates identical with V5.

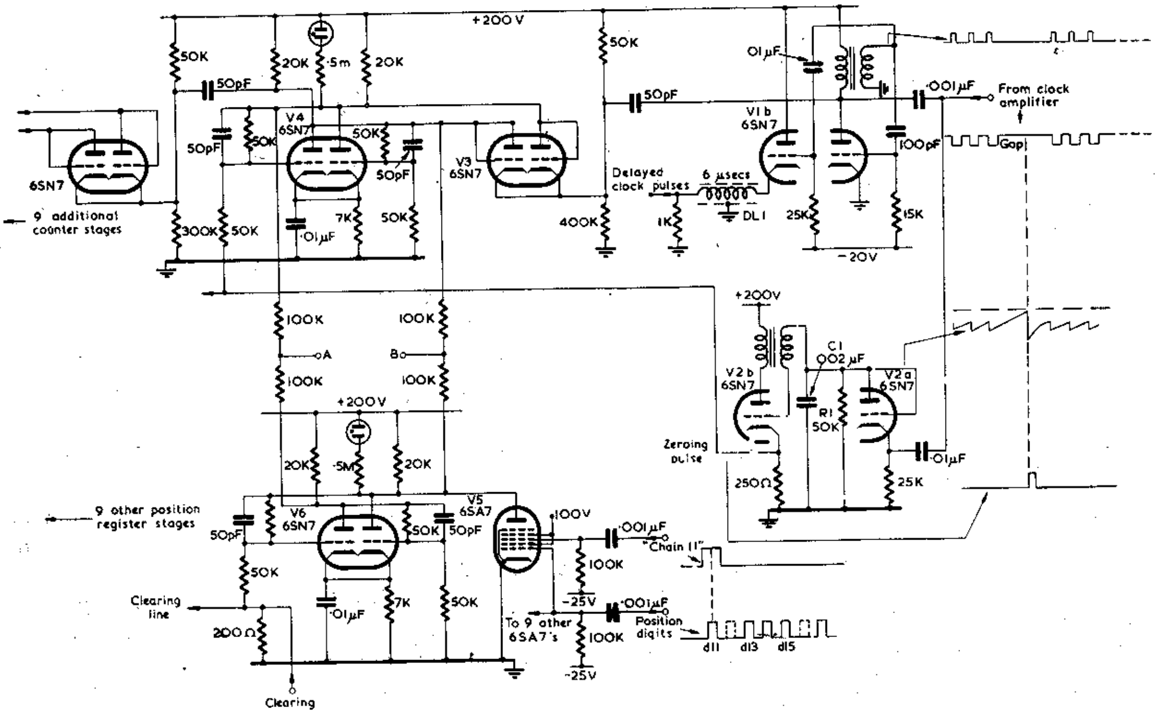

Figure 5.—Circuit of counter and position register.

Separation is performed with the aid of pulses termed " chain pulses " which are available from the main computer timing unit on 20 separate outlets. " Chain 1 " pulses are repeated at 60 microsecond intervals and coincide with the d_1 digit of a digit train, " chain 2 " pulses coincide with a d_2 digit and so on. Here the digit train occupying positions d_{11} to d_{20} is applied in common to the first grids of the separator valves while in the case of V5, " chain 11 " pulses are applied to its third grid. Thus V5 will pass current only if the d_{11} digit is unity and in that case the negative pulse at the plate of V5 will set the flip-flop V6 to the 1 state. The remaining flip-flops are set in a similar fashion.

Coincidence between the configurations of the counter and register is detected by the circuit shown in Figure 6. This circuit is similar to one which has previously been described by Booth.[7] Here the twin triodes V1 . . . . .V10 have their cathode potentials fixed at 140 volts and have a common plate load resistor. Their grid potentials are determined by the " summing " resistors R_s which are cross-connected between the plates of the counter and register flip-flops. The potential at the plate of a flip-flop is either 80 volts or 160 volts, depending on its setting, so that if, for instance, the extreme right-hand counter and register flip-flops are both holding 0 or both holding 1 the grids of V1 will both assume a potential which is the mean of 80 and 160 volts, i.e., 120 volts and both grids will be cut off. If the counter and register flip-flops have opposite configurations, one grid of V1 will rest at 80 volts while the other will tend to rise to 160 volts but will be held at 140 volts when that particular triode is fully conducting. A similar condition applies to the remaining valves V2 to V10 and all triodes will be cut off only for the 10-microsecond interval during which coincidence occurs along the complete row of counter and register flip-flops. The common plate potential then rises to 300 volts and a 10-microsecond coincidence pulse is developed.

As the counter goes through its cycle varying numbers of the triodes V1 to V10 are switched on at any one instant, and the waveform on the common plate lead shows a stepped pattern before and after the coincidence pulse. Furthermore the phase of the leading edge of the latter pulse relative to the adjacent clock pulse is not stable owing to time delays in the counting chain. Therefore, to obtain a more accurately timed pulse, the primary coincidence pulse is used to " turn on " the third grid of V11, while the first grid of the latter valve is " turned on " by the delayed clock pulse train. The delay of this pulse train is such that only one clock pulse is overlapped by the primary coincidence pulse, as shown in Figure 6 and there is an adequate safety margin for variation in the delay of the latter pulse. Thus V11 conducts only for about 2 microseconds giving a clean negative pulse which is inverted and amplified and fed out as a position selector pulse.

(*b*) *Amplifiers.*

The amplifier unit carries 21 3-stage resistance-coupled amplifiers which are of conventional design and need not be described in detail. Their response is adjusted to cut off sharply below 10 kc/s in order to minimize hum pick up troubles. An input of 5 millivolts peak to peak is delivered to the amplifiers by the heads which have an impedance of 30 ohms. Use of an input transformer giving a step up ratio of say 30:1 would permit of the elimination of one of the amplifier stages. Since a single

7. Booth, A. D., " The Physical Realization of an Electronic Digital Computer," Electronic Engineering, 22, 1950, 492.

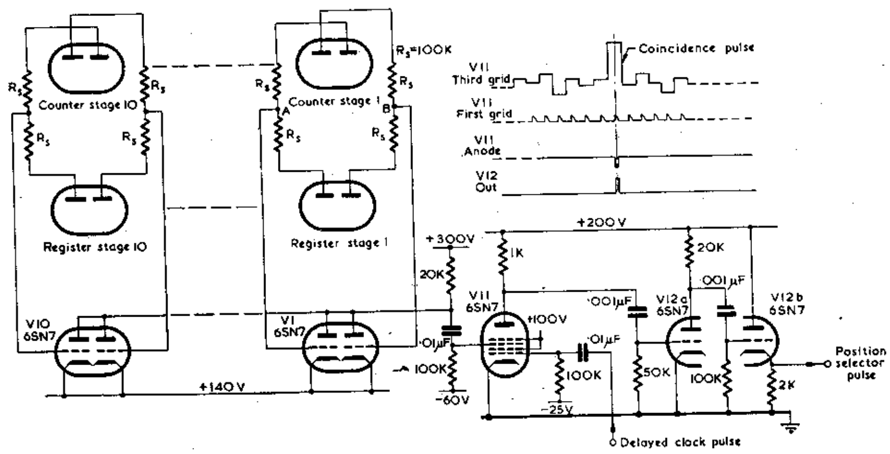

Figure 6.—Circuit of coincidence detector.

head is used for reading and recording, the writing pulses are unavoidably applied directly to the amplifier inputs (through a 5000-ohm stopper resistance) and cause a transient overload. However, the amplifiers recover full sensitivity in 1 millisecond, well before any subsequent reading-out operation may be called for.

(c) *Input unit.*

The input unit comprises 20 groups of 4 valves as shown in Figure 7. Here one of the digits in the incoming digit train is passed to the input register flip-flop V2 through the series-parallel gate valve V1 whose action is identical with that described previously in connection with the position selector unit. A power supply of negative polarity is used with the flip-flop V2 and with the component values indicated one plate stands at a potential of —20 volts while the other stands at —120 volts. These potentials set the bias on the control grids of the two thyratrons V3 and V4 to which is applied a common 50-volt trigger pulse. Thus if the register flip-flop holds a 0, V4 will fire and the condenser C2 will discharge through the head delivering a positive current pulse of approximate half sine wave shape and duration 1 microsecond. Alternatively if the register holds a 1, V3 fires and the condenser C1 delivers a negative current pulse to the head. It will be apparent that when V3 is triggered the resulting negative current pulse appearing across the recording head will drop the cathode potential of V4 to such an extent that its relative grid-cathode potential will become momentarily zero. V4 might therefore be expected to fire and cance the pulse delivered by V3, but this does not occur since V4 is only weakly triggered for a small fraction of a microsecond while the firing delay of a 2D21 under these conditions is 2 or 3 microseconds.

(d) *Output unit.*

Figure 8 shows the essentials of the output unit. Here the position selector pulse is fed in common to the first grids of a row of 20 valves identical with V1 while the individual head amplifier outputs are fed to their third grids. When reading out the content of a specified storage location V1 will pass current only if a 1 digit is present in this location as will be apparent from the waveforms of Figure 2. In this case the flip-flop V2 (previously cleared) will be set to the 1 state. V2 sets the bias on the third grid of V3 which will be cut off if V2 is in the 0 state and " on " if V2 is in the 1 state. The first grid of this valve is also turned " on " periodically by " chain 1 " pulses. The plates of V3 and 19 other identical valves forming a parallel-to-serial gate system are connected in parallel to a 1500 ohm load resistor so that a negative pulse train which is the serial representation of the number held in the output register flip-flops will appear on the common plate lead, and will be repeated at 60 microsecond intervals. This pulse train is inverted by V4 and sent to the sequence unit, whence it is transmitted to the computer at the appropriate time.

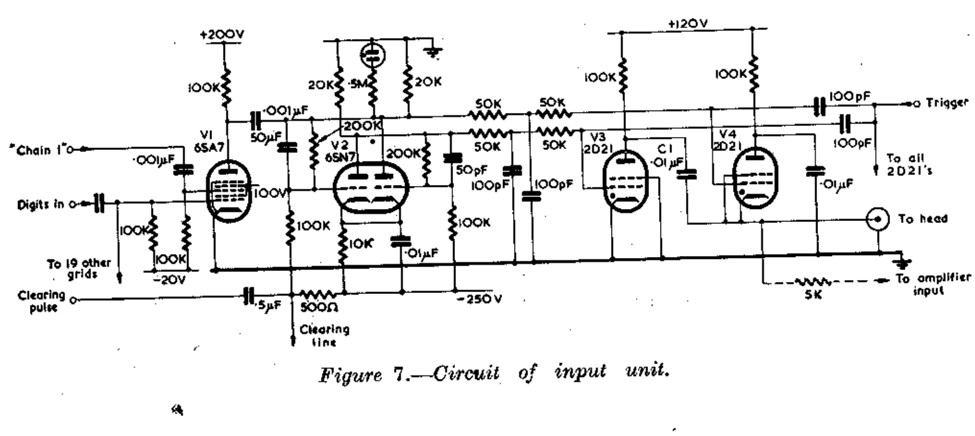

Figure 7.—Circuit of input unit.

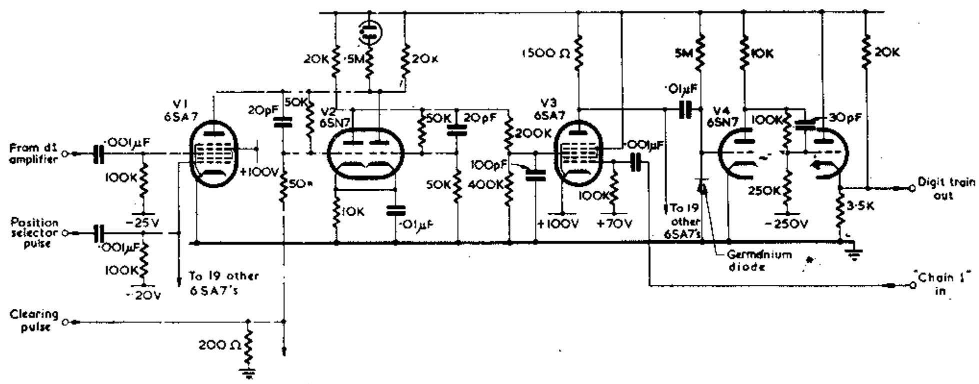

Figure 8.—Circuit of output unit.

(*e*) *Valve requirements.*

A total of some 280 valves is used in the above units and this number could be cut down to 200 by eliminating the input, output and position registers and sharing certain registers which have a similar function in the main computer. However, the provision of separate registers has led to flexibility in testing the experimental system.

It is now planned to increase the drum capacity to 4096 numbers by adopting a 9-inch drum with 40 tracks and 2048 digits per track. The larger drum will require the addition of only some 20 extra valves to the existing circuitry.

5. System Performance.

At the time of writing the drum system has been operating for about 6 months with a very good serviceability record. Retention of the stored information during shut-downs has proved a valuable feature since work on any major programme is liable to extend over a period of not less than a week allowing for time spent in routine maintenance work, testing the programme, and the local problem of power blackouts.

The present method of feeding data into the store, pending construction of a high speed punched tape reader, employs Hollerith punched cards, fed through a card reader. Numerical data are converted into binary form and stored on the drum under the control of a short programme. Time spent in reading in 500 decimally punched numbers amounts to about ¼ hour plus a certain amount of preparatory work in stacking cards etc. This includes time occupied in converting the numbers to binary form. The advantages of carrying out this operation once only as opposed to the several times which would be necessary if the contents of the store were lost at each shut-down will be readily appreciated. Furthermore there is usually sufficient space left on the drum for storing the working programme and at the start of each period of operating the computer the programme can be transferred to the high speed store in a few seconds under the control of a special switch which slightly modifies the machine cycle. Here again a few minutes are saved by avoiding the necessity of re-reading the programme from the original punched cards.

Prior to being put into computing service the magnetic drum unit was connected up to run on a self-contained test cycle for several weeks. The cycle was such that an initial number was read into position 0 and the contents of position 0 were then transferred to position 1 with a left shift of 1 digit position. Next, the contents of position 1 were similarly transferred to position 2, and so on, 50 transfers being effected every second. On reaching position 1023 its contents were transferred with a left shift to position 0 in order to maintain the cycle. This cycle ensured that every storage position was tested and every stored digit was altered periodically, means being provided to detect any error in the number being currently transferred.

The test proved a valuable one in revealing the initial weaknesses of the system, resulting from such things as a recording head with a border-line performance, gain variations in amplifiers etc. When these matters had been attended to the number of transfers successfully effected in between faults was found to average about 10^6 i.e. 2×10^7 digits transferred. Faults were usually due to some indeterminate agency, usually suspected of being a line-voltage surge, causing one of the digits to be wrongly written-in to or read-out of one of the storage positions.

6. Conclusions.

Magnetic drums of the type described above have many advantages when high storage capacity is required and a moderate access time can be tolerated. Enlargement of the storage capacity to the extent which future computing trends are likely to call for involves no fundamental problems. Thus, enlargement can be carried out either by increasing the drum diameter or by putting more sets of tracks on to a drum of the same diameter.

If access time is to remain unchanged the first approach demands an increase in peripheral speed and consequently in cell scanning rate. Since centrifugal stress at the presently-adopted speed is quite low, the limit on speed increase is set mainly by deterioration in the performance of the recording heads at the higher scanning frequencies. Some tests on the present design of recording heads have indicated that it should perform satisfactorily at cell scanning rates up to 300 kc/s, i.e., 3 times the present rate of 100 kc/s. The increased storage capacity obtained by enlarging the drum diameter is obtained very economically since it requires only a small enlargement of the position selector unit.

If it becomes desirable to provide additional groups of tracks the length of the drum can be increased readily. However the number of heads must be increased proportionately and extra equipment to switch between the groups of heads must be provided. The latter function can be readily performed by relays without significant increase of access time since the change-over between track groups may be expected to occur comparatively rarely.

It is of interest to compare the mode of organizing the magnetic drum storage system described above with that adopted at Manchester University[8] where the magnetic drum supplements a high-speed "Williams tube" store. Here the drum operates in the serial mode and the 64 word content of any track can be transferred in one revolution to the high speed working store. Since the time of transfer is short compared with the time taken to process the block of data thus transferred it is possible to store instructions on the magnetic drum while realizing a high overall computing speed. Such a scheme permits the use of a high-speed store of modest capacity but the price paid would seem to be the complication of fitting programmes into such a block structure.

In the case of the C.S.I.R.O. machine there is at present adequate storage capacity for instructions in the high speed store and the operation of the drum store is more flexible in that there is complete freedom of transfer between the drum and any computing register as well as between the drum and the high speed store. Should occasion arise to deal with a programme of length exceeding the available high speed storage capacity it is possible to store the excess instructions on the magnetic drum, and transfer them as required under the control of a short auxiliary programme. This would admittedly be a relatively slow process but would be effective enough to deal with an occasional contingency.

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Appendix I

Programme Involving Numerical Storage on the Magnetic Drum.

As an example of a simple programme which involved storage of a table of numbers on the magnetic drum, a Fourier synthesis programme is discussed. This programme reduced to a calculation of

$$f(xy) = \sum_{h} \sum_{l} A_{hl} \cos (hx + ly),$$

where A_{hl} took 250 values corresponding to 250 pairs of values of the harmonic numbers h and l. The A_{hl}'s were stored in even-numbered locations on the drum while the h's and l's were stored as 10 digit numbers in the odd-numbered locations, h taking the lower half of a location and l the upper half. The value of f(xy) had to be calculated at 2500 points in the xy plane. Each step in forming the partial sum represented by the above equation involved traversing a loop of about 60 instructions of which two were concerned with the extraction of h, l and A_{hl} from the drum. The rest were concerned with the formation of $hx + ly$, calculating $\cos (hx + ly)$ etc. The process of extracting an instruction from the high speed store decoding it and carrying out the specified transfer takes an average of 2.2 milliseconds when the magnetic drum is not involved, and an extra 6 milliseconds when it is. Thus the time taken to traverse a loop of 60 instructions not involving the drum is 132 milliseconds and in the above example the two drum extractions add 12 milliseconds. In this case, therefore, the magnetic drum adds 9 per cent. to the computing time, a figure which is of small practical significance.

In another programme for the calculation of an auto-correlation function the values of the function to be correlated were stored on the magnetic drum and the main calculation involved a loop of 30 instructions of which two were drum extractions. Here the increase in computing time due to drum extraction amounted to 18 per cent., a figure which again is not serious.

8. Williams, F. C., Kilburn, T. and Thomas, G. E., "Universal High Speed Digital Computers: A Magnetic Store," Proc. I.E.E. **99**, Pt. II, 1952, 94.

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