COMMONWEALTH OF AUSTRALIA

Commonwealth Scientific and Industrial Research Organization

Division of Radiophysics

MERCURY DELAY LINE MEMORY

C.S.I.R.O. COMPUTER

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1 INTRODUCTION

The memory unit of the C.S.I.R.O. Electronic Digital Computer has been modified to use the interspaced system which was described briefly in an earlier report.[1] This system effectively doubles the storage capacity of the memory. The modifications are chiefly in the gating circuits associated with the input and output to the memory, but there have been a few changes in the circulating loops themselves.

The block diagram of a memory loop remains unchanged (see Figure 1 of reference 1), but the common memory trunks have different signals applied to them. The clock trunk pulses are now spaced 1·5 instead of 3·0 microseconds apart; the input trunk pulses are the same as before but are delayed by 1·5 microseconds when being read into the interspaced position; the clearing trunk signal, instead of being a single pulse one word long, is now a train of 20 single digit pulses in the correct position to clear out the direct or interspaced pulses as required. When the line selector of any loop is active then the contents of that loop, both direct and interspaced, are gated on to the output trunk, and the appropriate pulses must be selected before being gated on to the computer output trunk.

Each circulating loop selected by a line selector signal provides two memory lines containing 16 twenty digit words. The P18-2-X and P18-2-Y interspacing signals, operated by one digit in the order code applying to the memory, select the particular line required, i.e. the direct or the interspaced. As far as the computer and the operator are concerned, these two lines are completely independent of each other.

To improve the accessibility of the equipment, it has been mounted in two separate cabinets, placed back to back.

correctly. These tests are designed to check the functioning of the store under the more extreme operating conditions, with the assumption that if it operates satisfactorily under these conditions it will also perform correctly under all other conditions. However these tests may fail to indicate some faults, such as rare intermittent shorts in valves, and these will have to be found by special testing.

It should be noted that faults indicated when testing one function may be due to failure of some other function which is used in this testing. For this reason a system of double checking must be used to determine exactly what the fault is.

To test reading in and holding, the extreme conditions occur when reading in sequentially either a single digit or all twenty digits. Faults may be readily observed by subsequently reading sequentially out of the store into the D-register. Any faults will then show up as flickering digits on the D-register monitor. A useful intermediate check, which sometimes shows up faults not apparent in the above, is to read in to all memory positions from the sequence register and again check by reading out of store into D.

It is also necessary to check that there is no interference between the interspaced and direct lines within each loop. This may be done by reading in to the interspaced positions only and observing, by use of D, whether any pulses have been read into the direct positions. Again, clearing of the interspaced positions should not affect the direct positions.

Clearing may be checked by reading zeros into the memory holding all twenty digits in all positions and also by reading the sequence register over a full store and checking that no extraneous digits are left.

Read out must be checked for correct read out pulse position, as well as presence of pulses and the absence of spurious digits. The most critical check of timing is to subtract the contents of the memory to an arithmetical register, such as D. Incorrect timing will cause some digits to be missed.

6 CHECKING

It is clearly not possible to give a checking procedure to discover the causes of all the possible faults which may be disclosed by the testing procedure. However the general method to be used may be indicated.

The nature of the fault will usually indicate the particular unit or units which are causing the trouble, e.g. if loop 2 (lines 4 and 5) will not hold digits while other loops will, then one of the units within this loop must be faulty. Once the fault is traced to a unit, the signals may be followed through that unit until the exact cause of the fault is found. In examination of a signal the following points should be watched for: presence or absence of the signal, incorrect timing, intermittent signal, spurious signals, low amplitude, slow rise or fall time of pulses, presence of 50 c/s modulation, incorrect D.C. level, or change in amplitude of pulses along a series.

In the checking of a particular loop the following points should be checked first with reference to Figure 6: amplifier output pulses, clocking gate output, electrical delay line input and output and circulator output. When a loop is being specially tested, e.g. when it is first put into service, or when we are looking for a noisy tube, it is sometimes helpful to break the loop by removing V_1, or again to break the connection from the circulator to the line driver and connect the circulator output of a correctly operating loop to the line driver input. The latter procedure enables the response of the loop to a varying number of pulses to be examined. One loop may also be tested by short routines stored in other loops.

Typical failures which have occurred are open circuit inductances, germanium diodes with low back resistance or open circuit, heater to cathode shorts in valves, change in resistor values, open and short circuit capacitors, intermittent cable connections, noisy or microphonic valves (particularly 6AC7 and KT61).

APPENDIX I
VOLTAGE LEVELS

No signal condition

(a) Line driver (Figure 5 of reference 1)

		Pin	Volts
V_1 (6SJ7)	Suppressor	3	- 45
"	Screen	6	+100
"	Plate	8	+180
V_2 (6AC7)	Cathode	5	+ 2
"	Screen	6	+150
"	Plate	8	+175
V_3 (6V6)	Cathode	8	+ 6
"	Screen	4	+200
"	Plate	3	+200

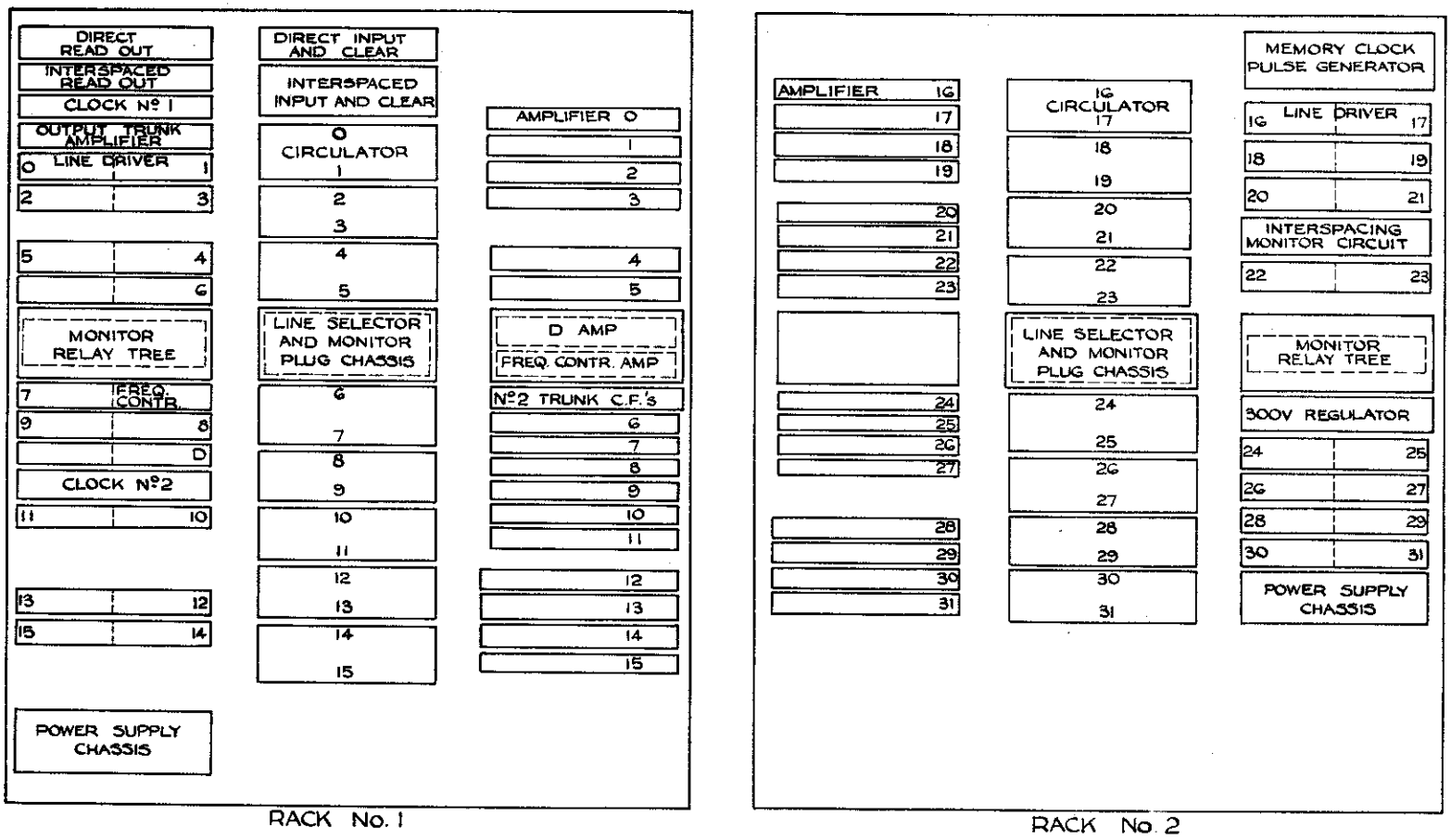
(b) Circulator (Figure 7 of reference 1)

V_1 (KT61)	Grid	5	- 18
V_2 (6SN7)	Cathode	3 & 6	+ 50
V_3 (KT61)	Grid	5	+ 48
"	Plate	3	+ 95
V_4 (KT61)	Cathode	8	+ 20
V_5 (KT61)	Cathode	8	+ 20
"	Grid	5	+ 6

(c) Line amplifier (Full gain)

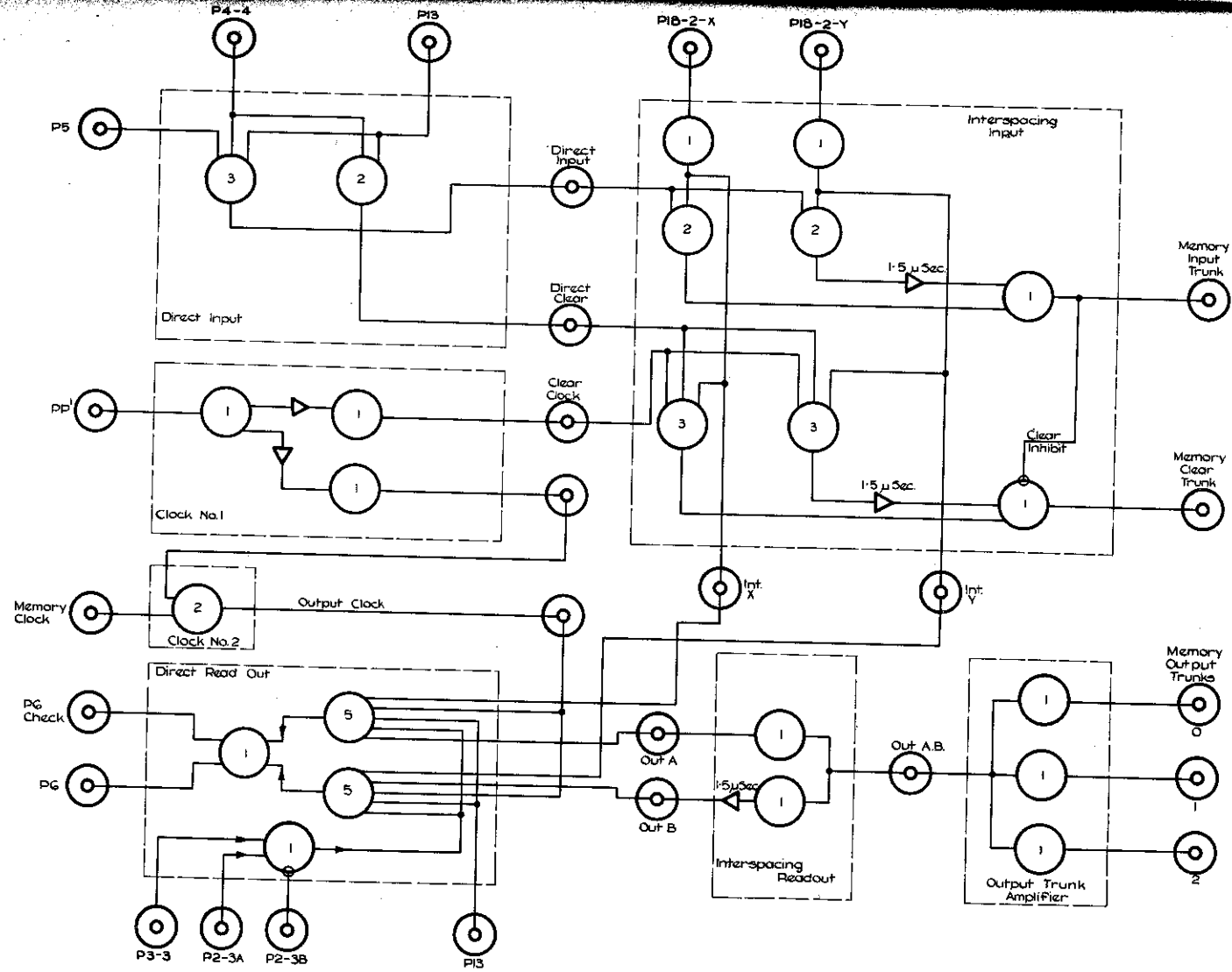
V_1-V_4 (6AC7)	Cathode	5	+ 2·0
"	Screen	6	+150
"	Anode	8	+190
V_5 (6AC7)	Cathode	5	+ 1·0
"	Screen	6	+150
"	Anode	8	+120
V_6 (6V6)	Cathode	8	+ 18
"	Screen	4	+200

LIST OF FIGURES



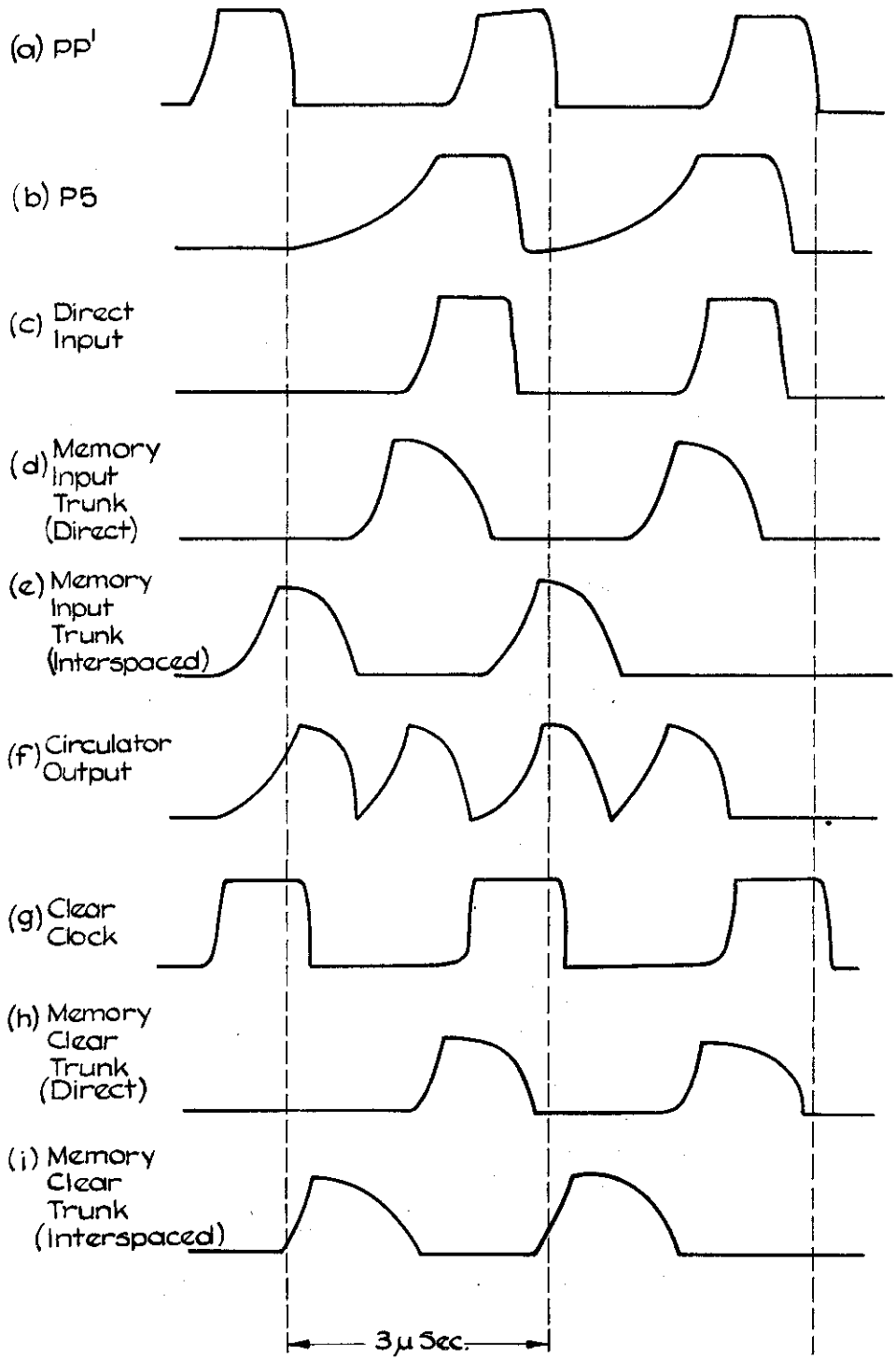
MEMORY CABINET LAYOUT

FIG. 1



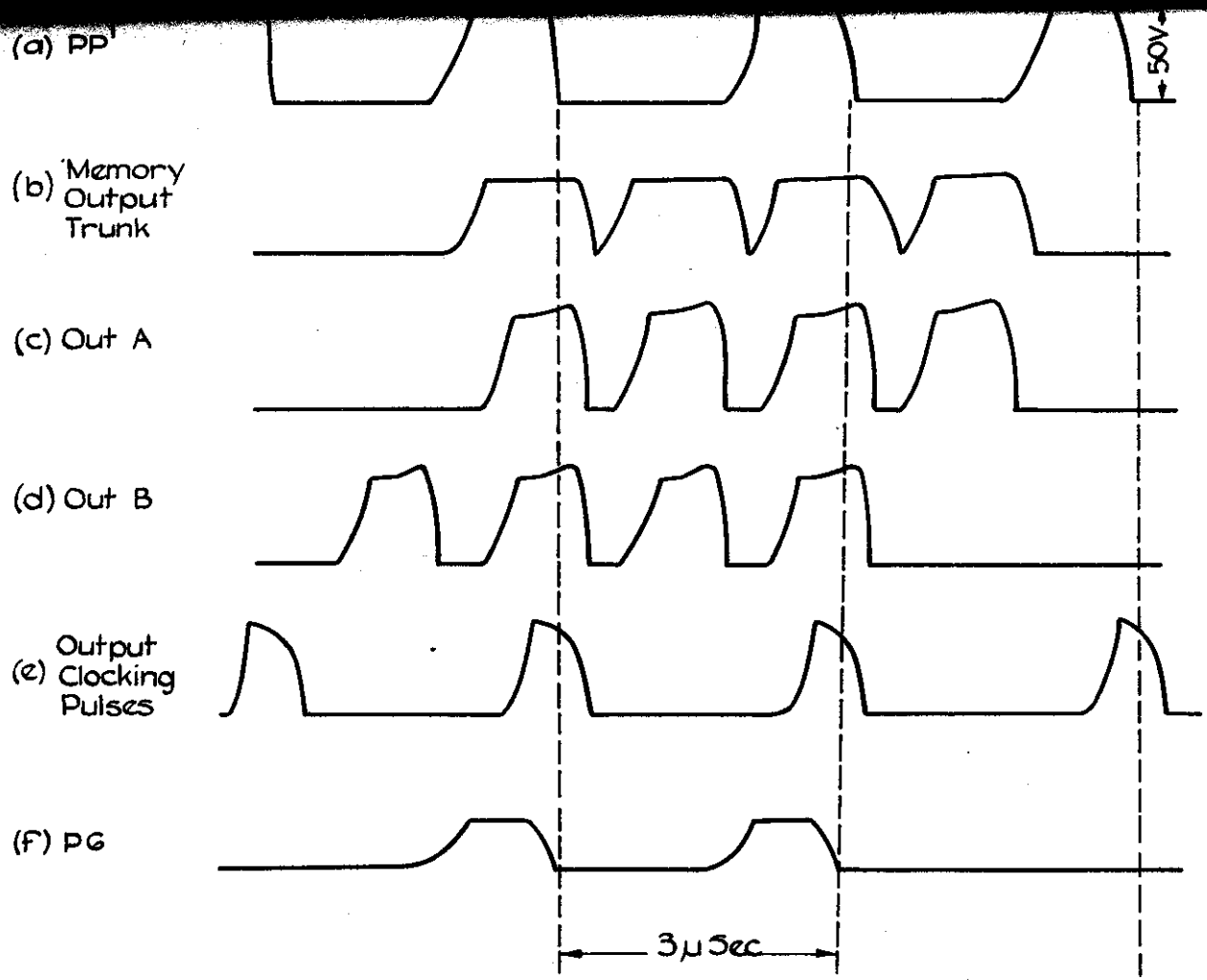
MEMORY INPUT OUTPUT GATING

FIG. 2



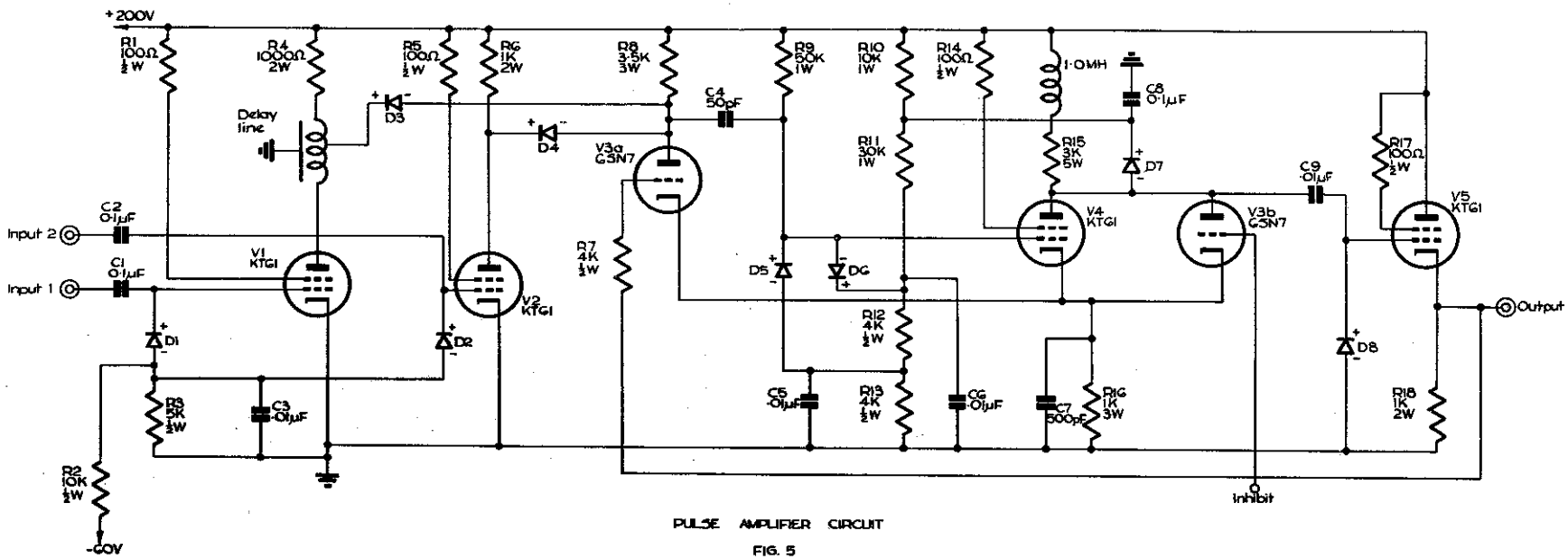
MEMORY INPUT GATING PULSES

FIG. 3



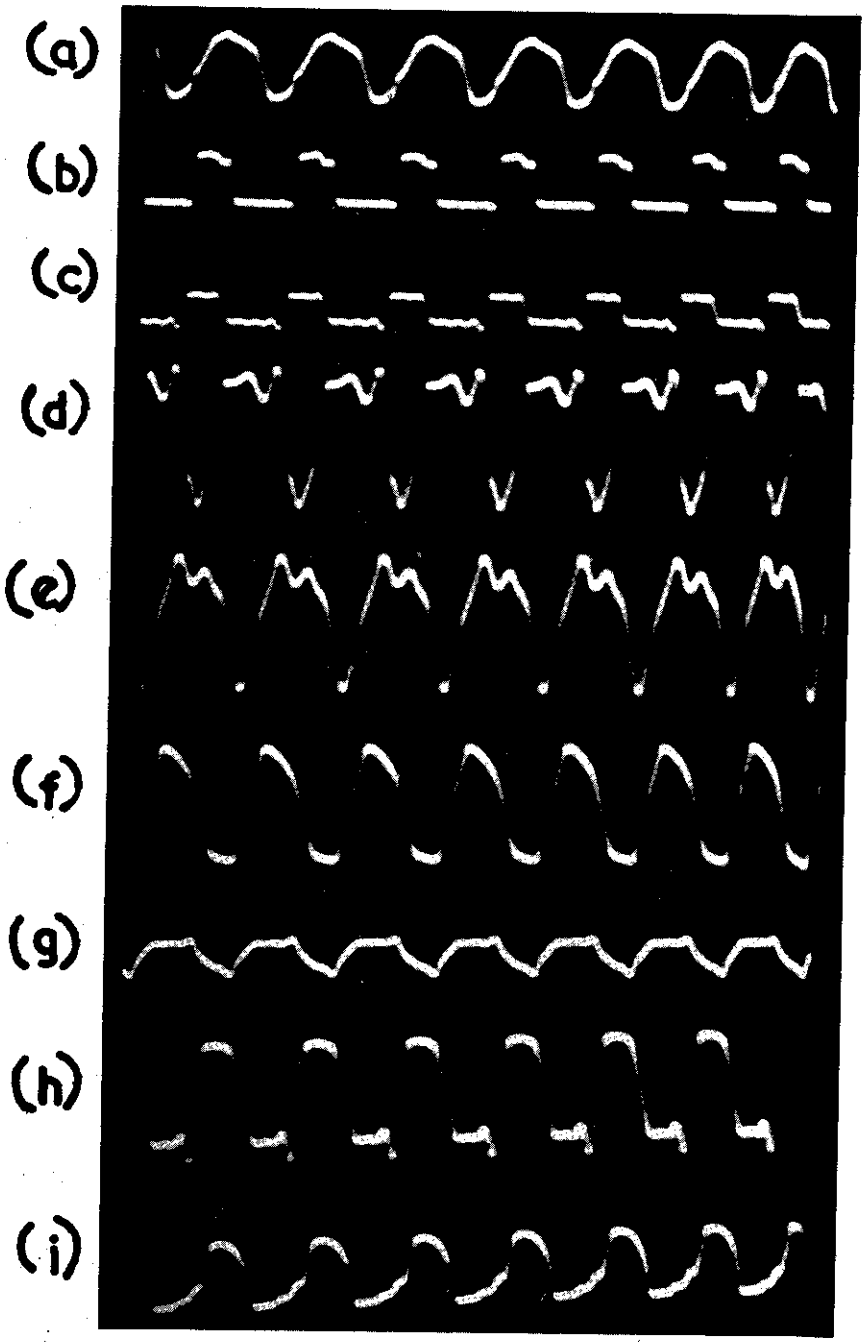
MEMORY OUTPUT GATING PULSES

FIG. 4



PULSE AMPLIFIER CIRCUIT

FIG. 5



CIRCULATOR WAVEFORMS

FIG. 6

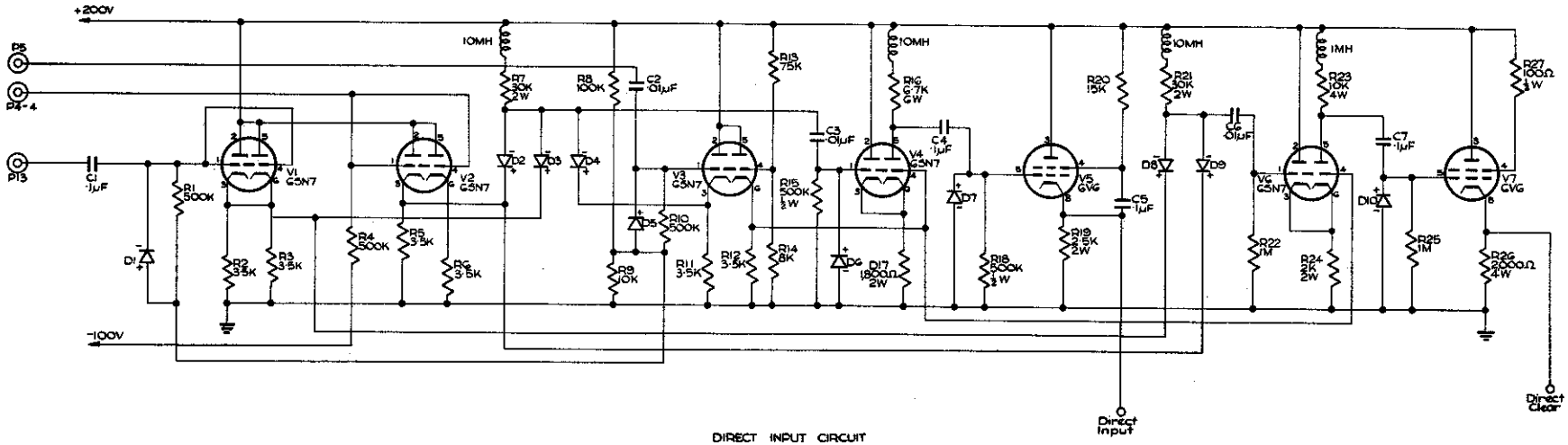
with the base containing the mercury delay lines suspended in between the cabinets. Air is kept moving through the racks by way of air ducts mounted on top of the racks, and driven by an exhaust fan. There are 16 circulating loops (i.e. 32 memory lines) mounted in each rack together with the clocking, gating and monitoring chassis. The locations of the various chassis in the racks are shown in Figure 1.

It will be observed that throughout the memory the practice of splitting circuits up into small units, comprising about seven valves, has been followed. While this does increase the number of interconnections between chassis, it considerably simplifies wiring and assembly, testing and servicing of the circuits. Power is brought into each of the chassis through octal sockets and plugs connecting to outlets provided at points in the memory cabinets.

2 INPUT AND OUTPUT GATING

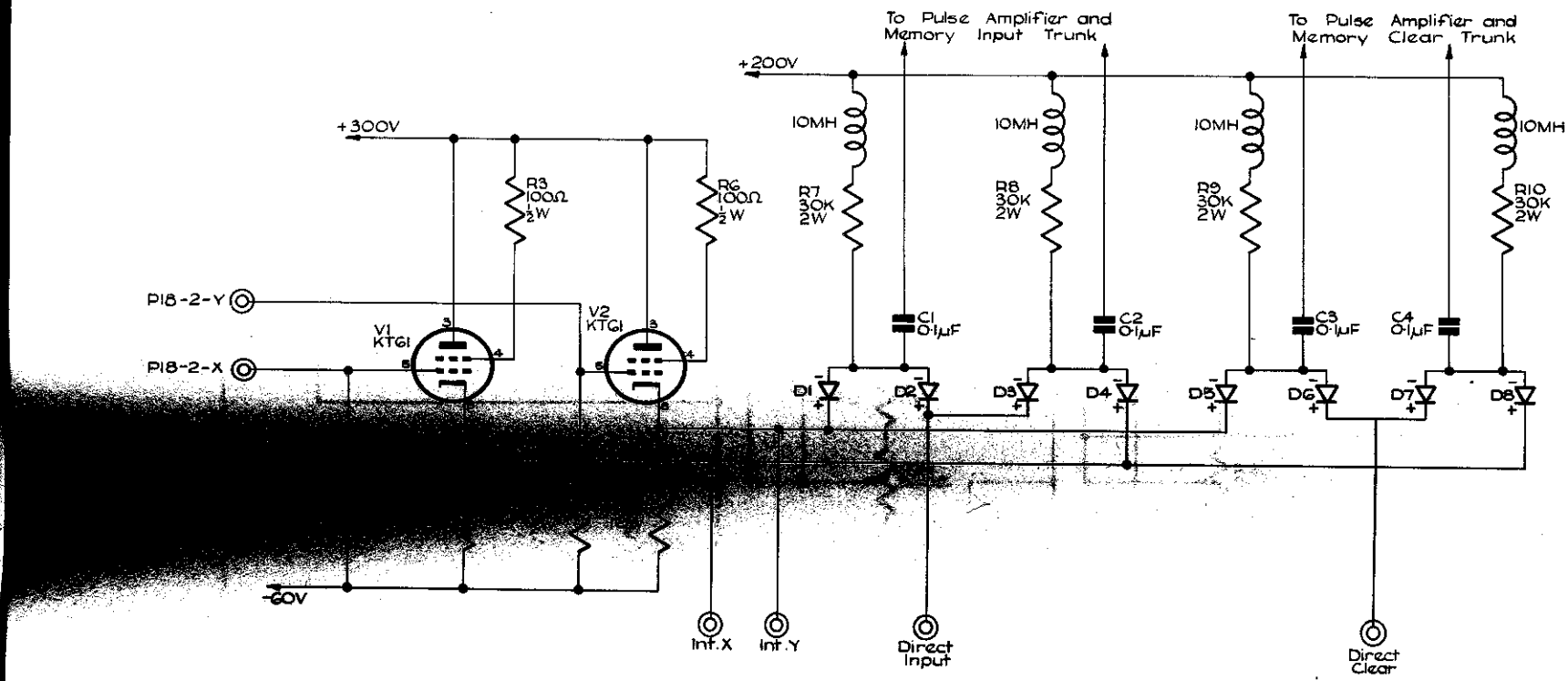
The logical circuit of the input and output gating of the memory is shown in Figure 2. The associated pulse waveforms are shown in Figures 3 and 4. In the direct input chassis digit pulses are gated from the computer input trunk P5 by the memory destination signal P4-4 and the time selector pulse P13, to give the direct input pulses. P4-4 and P13 also operate the second gate whose output is the direct clear pulse, which is a minor cycle in length.

If the digit pulses are to be read into the direct position in the loop, then the P18-2-X signal gates the direct input pulses straight on to the memory input trunk. If they are to go into the interspaced position, P18-2-Y will gate the direct input pulses through a 1·5 microsecond delay line before they go on to the trunk. The direct clear pulse is used to gate clock pulses (3 microseconds apart) which P18-2-X or P18-2-X again allow either to pass directly on to the memory clear trunk or to be delayed by 1·5 microseconds before going to the trunk. The clear clock pulses are generated by delaying PP' pulses to give the proper time position for correct clearing to occur in the circulator.

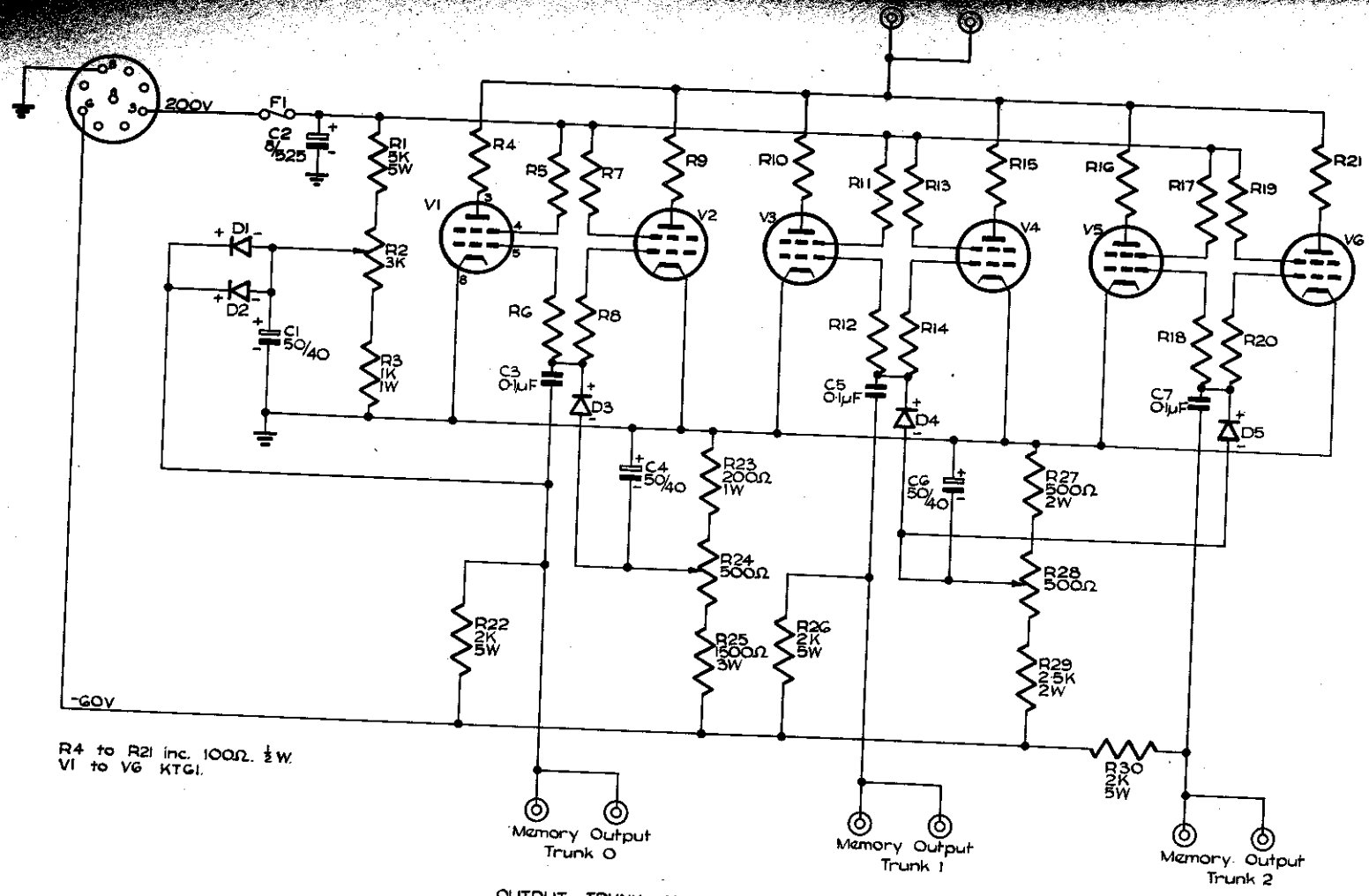


DIRECT INPUT CIRCUIT

FIG. 7



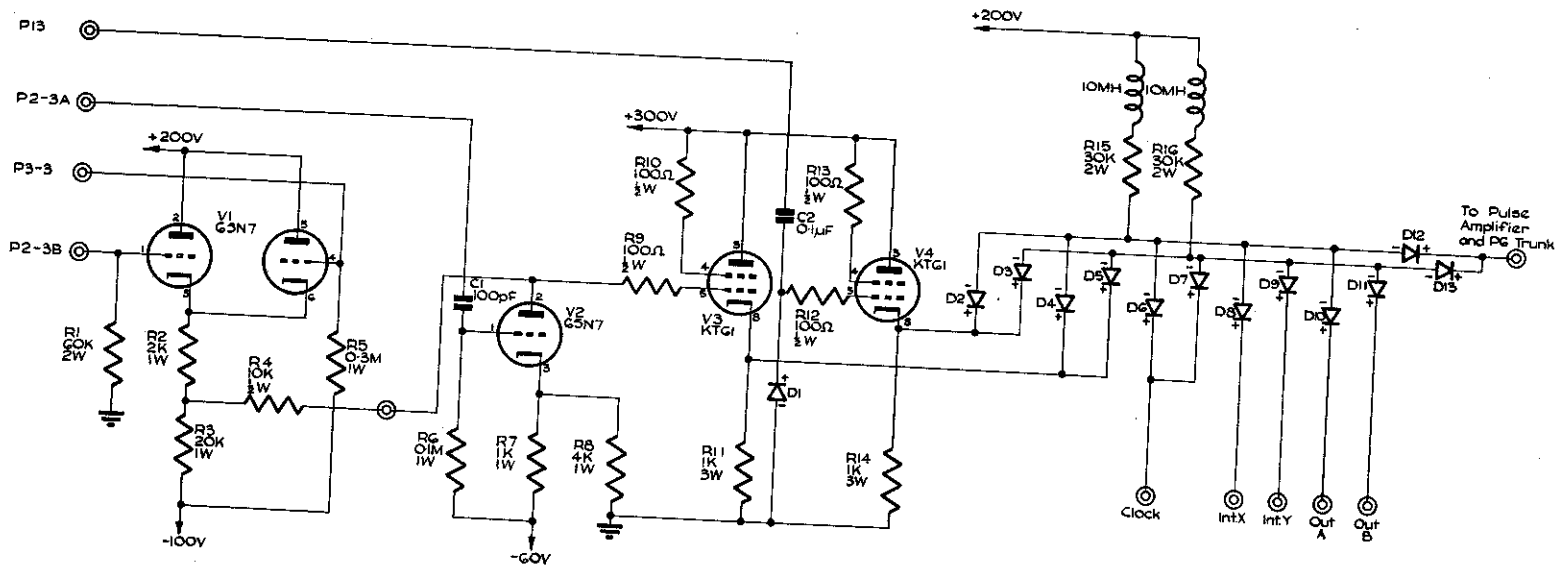
INTERSPACING INPUT CIRCUIT
FIG. 8



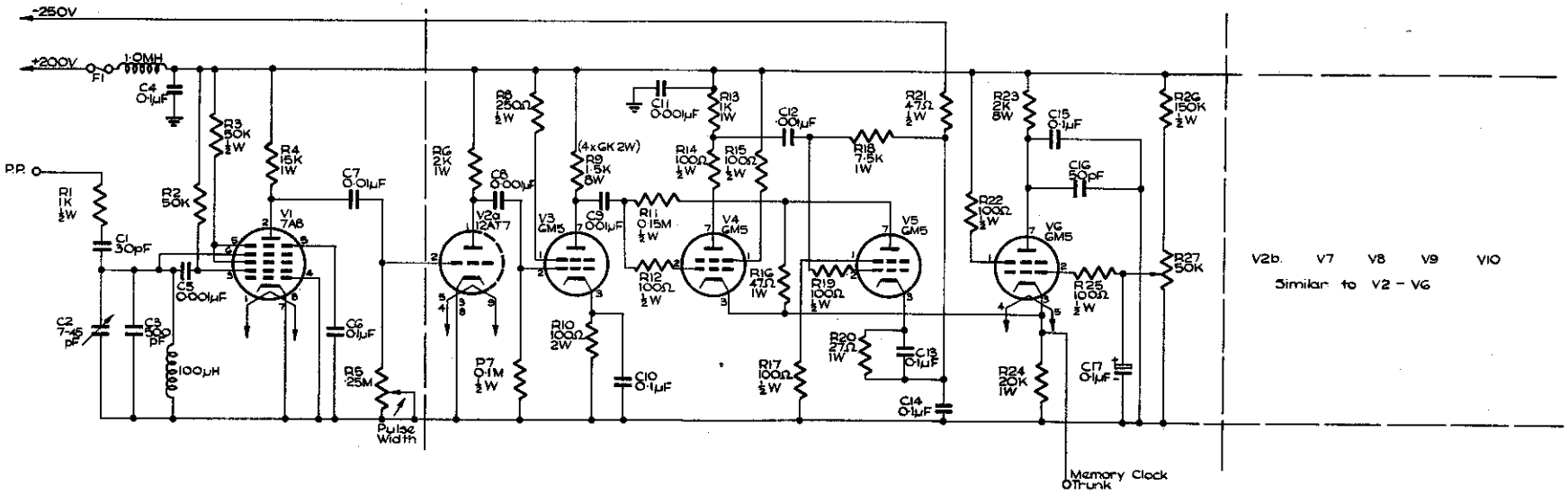
R4 to R21 inc. 100Ω. ½ W.
V1 to V6 KTG1.

OUTPUT TRUNK AMPLIFIER

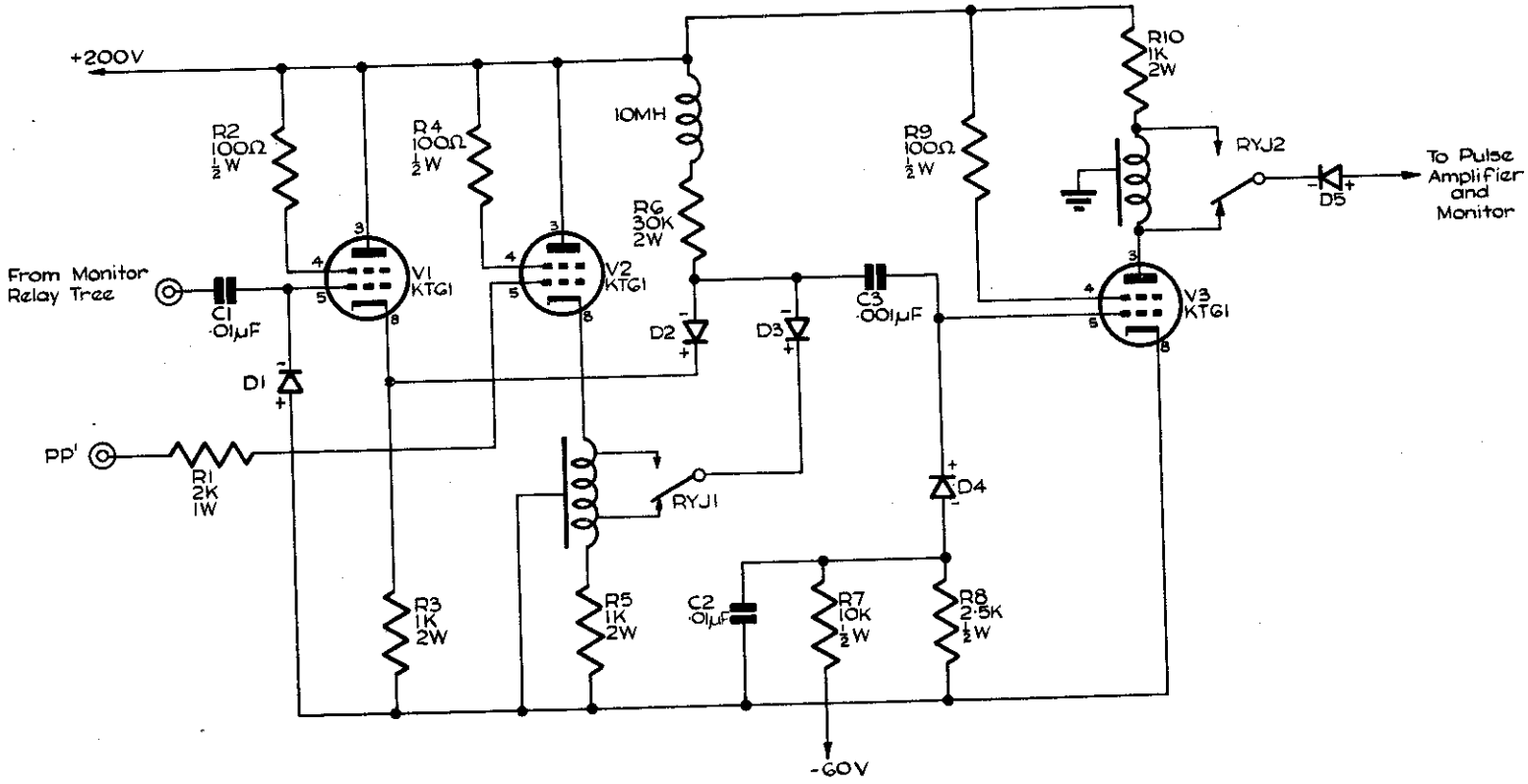
FIG. 9



DIRECT READ OUT CIRCUIT
FIG. 10



MEMORY CLOCK PULSE GENERATOR
FIG. 11



INTERSPACING MONITOR CIRCUIT

FIG. 12

When a pulse is being read into the memory, there is no need to clear out a pulse which may already be circulating in that position; the clearing pulse will simply disturb the loop to no good purpose. For this reason the memory input trunk pulses are used to inhibit the clear trunk pulses. However, the clear pulses are earlier than the input pulses and so this inhibition is not complete.

The P18-2-X and P18-2-Y cathode followers in the interspacing input chassis are also used to drive the diode gates in the direct read out chassis. The connection is via the interspacing X and Y lines.

Whenever the line selector of a loop is activated, the contents of that loop are gated on to the memory output trunk. This trunk is divided into three sections, one for loop 0, one for loops 1 to 15 and one for loops 16 to 31. Loop 0 is inactive only when information is being read in or out of other lines. Thus the contents of loop 0 are being read out on to its output trunk most of the time, and it is convenient for checking purposes to keep it separate from the output of other loops. Separate output trunks are used for loops 1 to 15 and 16 to 31 simply to reduce the stray capacitance, and so keep pulse rise and fall times as low as possible.

These output trunks are connected to amplifiers with a common output connection in the output trunk amplifier chassis. The interspacing read out chassis provides two outputs, out A and out B, the latter delayed by 1·5 microseconds. These are connected to a pair of diode gates, in the direct read out chassis, which are also driven by P3-3 of P2-3B signals, either of which calls on memory as a source, interspacing X and Y, P13 and also clock pulses. The latter serve to gate out only the interspaced pulses on the out A line, or the delayed direct pulses on the out B line. This is necessary because both interspaced and direct loop pulses are present on the out A and out B lines. These output clocking pulses must be less than 0·5 microsecond long to prevent break through from pulses adjacent to the required pulse positions. It is convenient to generate them by using delayed PP' pulses to gate alternate memory clock pulses which are of the correct duration and timing for this output clocking.

The output of the diode gate selected by the interspacing X and Y signals is amplified before being passed to the main computer output trunk P6. A P6 check point is also provided for distinguishing pulses being read out of the memory from those coming from other parts of the computer.

The P2-3 A signal is used to inhibit spurious read out from memory due to the slow fall time of the P-3-3 signal.

3 CIRCUITS

3.1 Pulse amplifier

Throughout the memory, use has been made of the pulse amplifier whose circuit is shown in Figure 5. This is the same circuit as used in the circulator. The complete circuit as shown is not always used, some functions not being required in certain cases. The valves V_1 and V_2 provide for two separate inputs with a common output. An electrical delay line may be placed in either V_1 or V_2 anode to delay either signal. The diode D_5 limits the amplitude of the pulse on V_4 grid and ensures a uniform output pulse width independent of the succession of pulses. D_5 is only necessary when the pulse repetition rate is 700 kc/s, i.e. where the circuit handles pulse trains containing both direct and interspaced digits. Without D_5 a single pulse is wider than those in a long train. Again the catching diode D_7 is only used when it is desired to limit the amplitude of the output pulse and ensure a flat top to the pulse. V_{3b} allows the output to be inhibited by a signal applied to its grid.

The properties of this circuit, which determined its design, are that the output pulse is substantially independent of the input pulse over a range of width and amplitude; the output pulse width and rise and fall times are adequate for the interspaced pulse spacing of 1·5 microseconds, and finally, the output pulse is independent of the succession of pulses.

The valves V_1 and V_2 are normally below cut off to remove any break through from preceding diode gates. The input pulse causes D_3 or D_4 to conduct and lower the potential of V_{3a} anode. This negative step is transferred to V_4 grid by C_4. V_4 is cut off, which allows its cathode potential to fall and its anode to rise. The consequent

rise in the V_5 output potential allows V_{3a} to conduct and bring its anode potential down causing regenerative action. The diode D_5 conducts when the V_4 grid potential falls to about 25 volts. The fall in V_{3a} anode cuts off the diodes D_3 and D_4 and so isolates the amplifier proper (V_{3a} and V_4) from the input pulse. V_4 remains cut off until C_4 is charged up again through R_9, the time constant $C_4 R_9$ determining the output pulse length. When V_4 grid rises above its cut off, the reverse regenerative action occurs, V_4 anode potential falling and its cathode rising causing V_{3a} to be cut off and increasing V_4 grid potential even further. The upper excursion of V_4 grid is limited by conduction of D_6.

During inhibition V_{3b} conducts and holds V_4 anode potential down, even if V_4 is cut off. This inhibition or clearing function is critical with regard to the bias applied to the V_{3b} cathode. With the circuit shown in Figure 5 the optimum point is with 50 volts on the cathode and about 25 volts on the grid. If the bias is too large then the inhibition action is not complete, the V_{3b} plate current being insufficient to hold V_4 anode down when V_4 is cut off. If the bias is too low, then V_{3b} plate current is too large and the back edge of the resulting negative pulse at the anode causes a positive pulse -- due to the D.C. restorer action of D_8 - to appear on the output and give rise to spurious pulses in the following pulse position.

3.2. Circulator

There have been two changes in this circuit to improve its operation in the interspaced system. A catching diode is used to limit the pulse amplitude in V_3 grid (Figure 7 reference 1) in the pulse amplifier. The second change is the replacement of the half 6SN7 (V_6) valve in each circuit, driving the common output trunk, by a KT61. This improves the output trunk pulse amplitude and rise and fall times, which are more critical in the interspaced system. A minor change is the connection of the circulator output to the monitor relay tree through a 1000 ohm resistor. The latter prevents the large capacity of the lead to the monitor from affecting the output pulse. The voltage levels at different

points in the circulator, the line driver and line amplifier are given in Appendix I.

3.3 Direct input circuit

This circuit, shown in Figure 7, consists of a triple diode gate driven by 6SN7 cathode followers for the direct input signal and a double diode gate driven by the same cathode followers for the direct clear signal. 6SN7 cathode coupled amplifiers driving 6V6 cathode followers are used as output stages.

3.4 Interspacing input circuit

This chassis contains two sections, one driving the memory input trunk, and one driving the memory clear trunk. Part of the circuit is shown in Figure 8; the pulse amplifiers are as shown in Figure 5. In the first section, we have two double diode gates driven by the direct input cathode follower and the two KT61 interspacing cathode followers. The second clear section is similar, using two triple diode gates with clock pulses determining the clearing pulse position. Both the pulse amplifier circuits have a 1·5 microsecond delay line in the interspaced signal path.

3.5 Output trunk amplifier

Each of the three output trunks is connected to two KT61's operating in parallel, as shown in Figure 9. The anodes of all six KT61's are connected together. It was found necessary to use two KT61's to obtain fast rise time of the pulses into the low impedance (1000 ohm) delay line connected to the KT61 anodes in the interspacing read out chassis. With only one KT61 the rise time of the pulses along a train became progressively slower and caused a shift in pulse position and consequently gave incorrect memory read out.

3.6 Interspacing read out circuit

This circuit simply consists of two pulse amplifiers with their inputs taken from points 1·5 microseconds apart on a delay line driven from the output trunk amplifier. The two outputs are connected to the diode gates in the direct read out chassis.

3.7 Direct read out circuit

The memory may be called on as a source by either P3-3 or P2-3B. These two signals are combined using two cathode followers with a common cathode load (V_1 in Figure 10). The output drives V_3 cathode follower which in turn drives the diode gates. The P2-3A signal is differentiated by C_1 and R_6 so that memory read out is inhibited for a short period after the beginning of P2-3A and so prevents spurious read out due to the slow fall time of the P3-3 signal.

3.8 Memory clock trunk pulse generator

The memory clock pulses are 0·5 microsecond wide, spaced 1·5 microseconds apart and are locked accurately in phase with the PP' pulses. The first clock circuit used frequency doubling circuits driven by PP' pulses, but it was found difficult to produce uniform pulses; there was always a difference in amplitude or timing between pulses immediately following PP' pulses and those in between PP' pulses.

The present circuit, shown in Figure 11, uses a 7A8 transitron oscillator which is synchronized by injecting a small PP' signal on to the oscillator grid. The phase of the memory clock pulses, relative to PP' pulses, can be set accurately by adjusting the trimmer C_2 across the oscillator tank circuit. The 7A8 output is not sinusoidal, but has large peaks which are amplified in the 12AT7 and 6M5 to provide large amplitude pulses of the correct width. The pulse width is set by the bias control potentiometer R_5 in the grid of the 12AT7. The output consists of a modified cathode follower circuit[2], with V_5 operating as the cathode load and V_6 as a low impedance source for setting the base level of the clock trunk. This is adjusted so that there is no clock break through in the circulator clocking gate. Apart from the 7A8 oscillator, the circuit is duplicated with the outputs connected together to provide a low impedance for driving all the circulators.

Clearing of the store is effected by a relay in each rack momentarily short circuiting the memory clock pulses but leaving the trunk base level unchanged. The circulating

pulses then fail to pass the clocking gate and so the loop is left empty.

3.9 Interspacing monitor circuit

The output of the monitor relay tree[2] contains both the direct and interspaced pulses from the selected loop. The interspacing monitor circuit, Figure 12, selects either the direct or interspaced pulses for display on the monitor tubes. Selection is carried out by a double diode gate driven by the monitor relay tree output and by delayed PP' pulses. The position of these latter pulses is determined by the relay contact RYJ1 and the taps on the delay line; the taps are selected so that in one position of RYJ1 the direct pulses are gated, while in the other the interspaced are chosen. The relay RYJ is operated by a switch on the control panel. The output of the diode gate is amplified in V3, which drives a second delay line. The contact RYJ2 provides for delay of the direct pulses so that they are in the same time position as the interspaced pulses when they go to the monitor tubes.

3.10 General

The common memory trunks are connected to diode gates in all 32 circulator circuits. A short circuit, due to faulty tube etc., in any one of these circuits could cause damage to a large number of the germanium diodes used. To prevent such occurrences the 200 and 300-volt lines have fuses in each circulator chassis. A similar precaution has been taken in the line-driver chassis. The 200 and 300-volt lines also have main fuses and switches in each memory cabinet.

The KT61 valve is used widely in the memory. Since it has a high trans-conductance (9000 micrometres) and a large plate current, it is necessary to have stopper resistors (about 100 ohms is usually adequate), in the screen circuit and mounted directly at the socket, to prevent parasitic high frequency oscillations. The most critical circuit in this regard is the circulator line selector KT61, since the leads from the line selector output are long and are bunched together. A 0·01 microparsec bypass condenser on the 300-volt high tension lead to these valves also helps to prevent parasitics. In some circuits, such as the output

trunk amplifier, the precaution of placing oscillation stopper resistors in the grid, screen and plate leads has been taken.

Coupling condensers have usually been made 0·1 microfarad picopacks so as to eliminate difficulties due to changes in the D.C. level causing variations in pulse amplitudes along a series of pulses.

All switching relays have 0·1 microfarad condensers placed across their coils to prevent radiation interference when the relay circuits are opened. This radiation can cause pickup in the mercury delay line amplifiers.

4 MERCURY DELAY LINES

There is very little to add to the earlier discussion.[1] Regarding the lacquering of the monel tubing, this is done by plugging the ends of the tubes and filling with ordinary clear duco lacquer. The excess lacquer is drained out while the tube is rotated, leaving an even coating along the tube. The tube must be allowed to dry out completely over a period of some days.

Extreme care must be taken to see that the quartz crystal is not placed under any flexing strain when it is mounted between the two blocks of the end cell; otherwise the crystal will be cracked. To guard against this, the lead backing block must be given an accurately flat surface and there must be an adequate clearance between the edge of the crystal and the surrounding polystyrene insert.

When the attenuation of a delay line becomes excessive, owing to accumulation of scum in the mercury, it is not always necessary to disassemble the end cell for cleaning. It is often sufficient to clean the face of the crystal by rubbing over lightly with cloth soaked in carbon tetrachloride and then refill the line with clean mercury. After refilling, it has been noticed that a line may exhibit high attenuation for some hours; this is probably owing to air bubbles trapped in the mercury and slowly escaping.

5 TEST PROCEDURE

When the computer is switched on, a memory test procedure as outlined below should be gone through to ensure, as far as possible, that all the store functions are performed