Digital Design Verification Training

DLD Task: 4-bit ALU

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Revision History

Revision Number	Revision Date	Revision By	Nature of Revision	Approved By
1.0	12/08/2024	S. M. Sarmad	First Draft	

TABLE OF CONTENTS

1. Task Statement

Design and implement a 4-bit Arithmetic Logic Unit (ALU) in SystemVerilog that performs a variety of arithmetic and logical operations on two 4-bit signed operands. The ALU should support the following operations, each associated with a specific opcode:

- Addition
- Subtraction
- 2's Complement
- Increment
- Decrement
- 1-bit Left Circular Shift
- Bitwise OR
- Bitwise AND
- Bitwise XOR
- Identification of the Greater Operand
- Output of Either Operand

The ALU should correctly identify carry and overflow conditions.

The inputs to the ALU will be two 4-bit operands (*operand_a*, *operand_b*) and a control signal representing the operation to be performed (*opcode*). The outputs will include the 4-bit result (*result*), a carry flag(*carry_out*), and an overflow (*overflow*) flag.

Your design must be synthesized for Nexys A7 board, with a focus on optimizing area and power. Additionally, the design should be thoroughly verified with a comprehensive testbench that includes test cases for all supported operations and corner cases.

2. Deliverables

- **SystemVerilog Code**: Implementation of the ALU with the specified input and output names.
- **Testbench**: A comprehensive testbench covering all operations and verifying the correctness of the ALU.
- **Project Files**: All project files necessary for synthesis and simulation.
- **System Block Diagram**: High-level overview of the system.
- **RTL Diagram**: Detailed RTL schematic of the ALU.
- **Area, Timing, and Power Reports**: Synthesis reports, including area, timing, and power metrics of the design for the Nexys A7 board. Identify the critical and fmax.

3. Evaluation Rubric

Category	Criteria	Points	Description
Design Specification	Compliance with specified operations (addition, subtraction, etc.)	10	ALU supports all the required operations with correct opcodes and functionality.
	Correct identification of carry and overflow conditions	4	Accurate detection of carry and overflow in relevant operations.
	Proper use of standardized input/output names	4	Consistency with the specified input/output names (**operand_a**, **operand_b**, **opcode**, **result**, **carry_out**, **overflow**).
Code Quality	Code organization and readability	3	Code is well organized, commented, and easy to follow.
	Modular design and reusability	3	Design is modular, making it easier to reuse and modify components.
Synthesis and Optimization	Synthesis for Nexys A7 board	5	Successful synthesis targeting the Nexys A7 board.
	Area optimization	5	Efficient use of FPGA resources, demonstrated by the area report.

	Power optimization	5	Power-efficient design, as evidenced by the power report.
Verification	Completeness of the testbench	6	Testbench covers all operations and edge cases, including corner cases.
	Accuracy of the simulation results	4	All test cases pass with correct results, including handling of carry, overflow, and edge conditions.
	Handling of corner cases	4	ALU correctly handles all identified corner cases.
Deliverables	Inclusion of all required deliverables	3	All specified deliverables (HDL Design, testbench, project files, diagrams, reports) are submitted.
	Quality of the System Block Diagram	3	System block diagram is clear, accurate, and well-documented.
	Quality of the RTL Diagram	3	RTL diagram accurately represents the ALU design and is well-documented.
Report	Accuracy and clarity of reports	5	Reports are detailed, accurate, and provide clear insights into area, timing, and power metrics.

Extra Features	Implementation of additional features or optimizations	3	Any additional features, optimizations, or innovative approaches beyond the basic requirements.
Viva	Understanding of ALU design concepts	15	Demonstrates a deep understanding of ALU design, including operations, opcodes, and corner cases.
	Ability to explain design choices and optimizations	10	Clearly explains the rationale behind design choices, optimizations, and handling of edge cases.
	Response to technical questions	5	Provides accurate and insightful responses to technical questions related to the ALU design and its synthesis for the Nexys A7 board.