NUST CHIP DESIGN CENTRE

Digital Logic Design

Lab Manual # 08
Combinational Circuits using System Verilog

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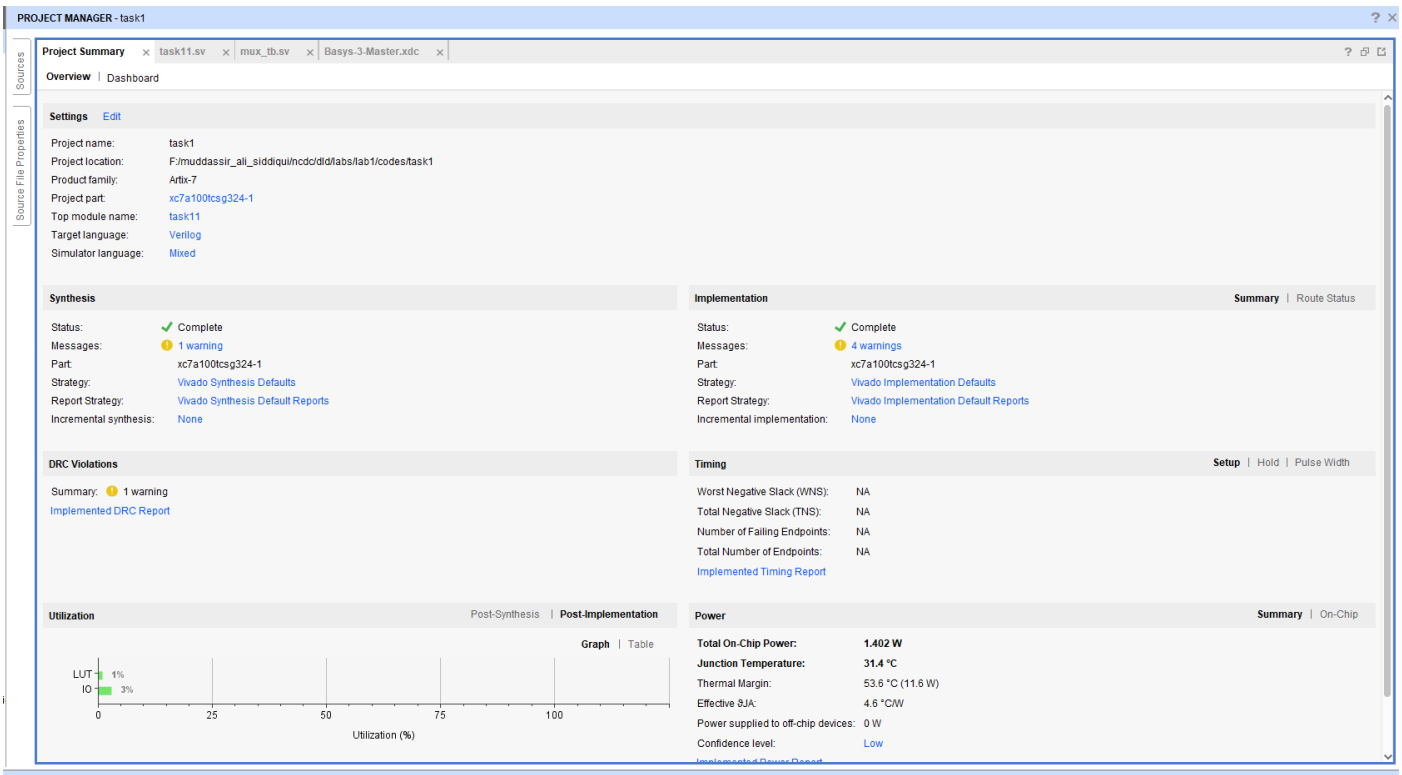
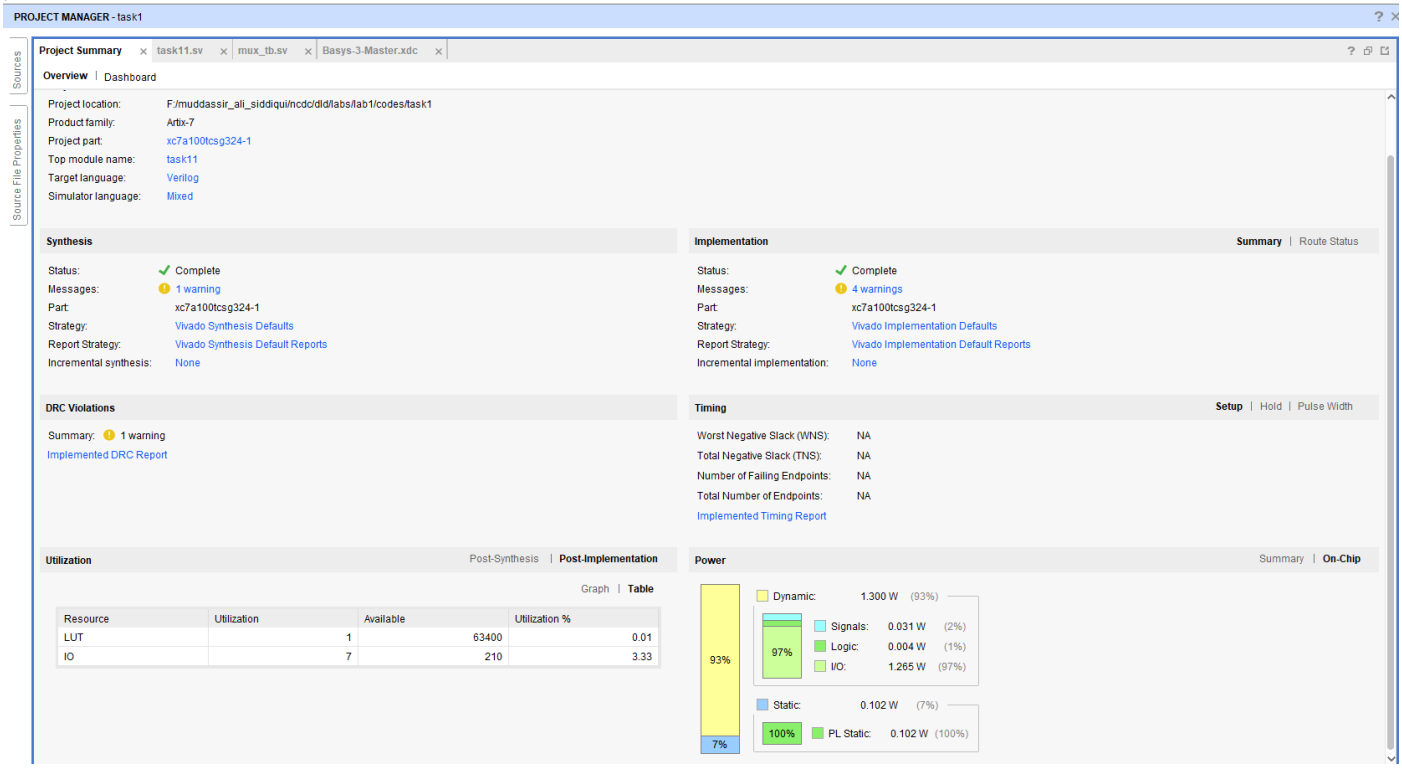
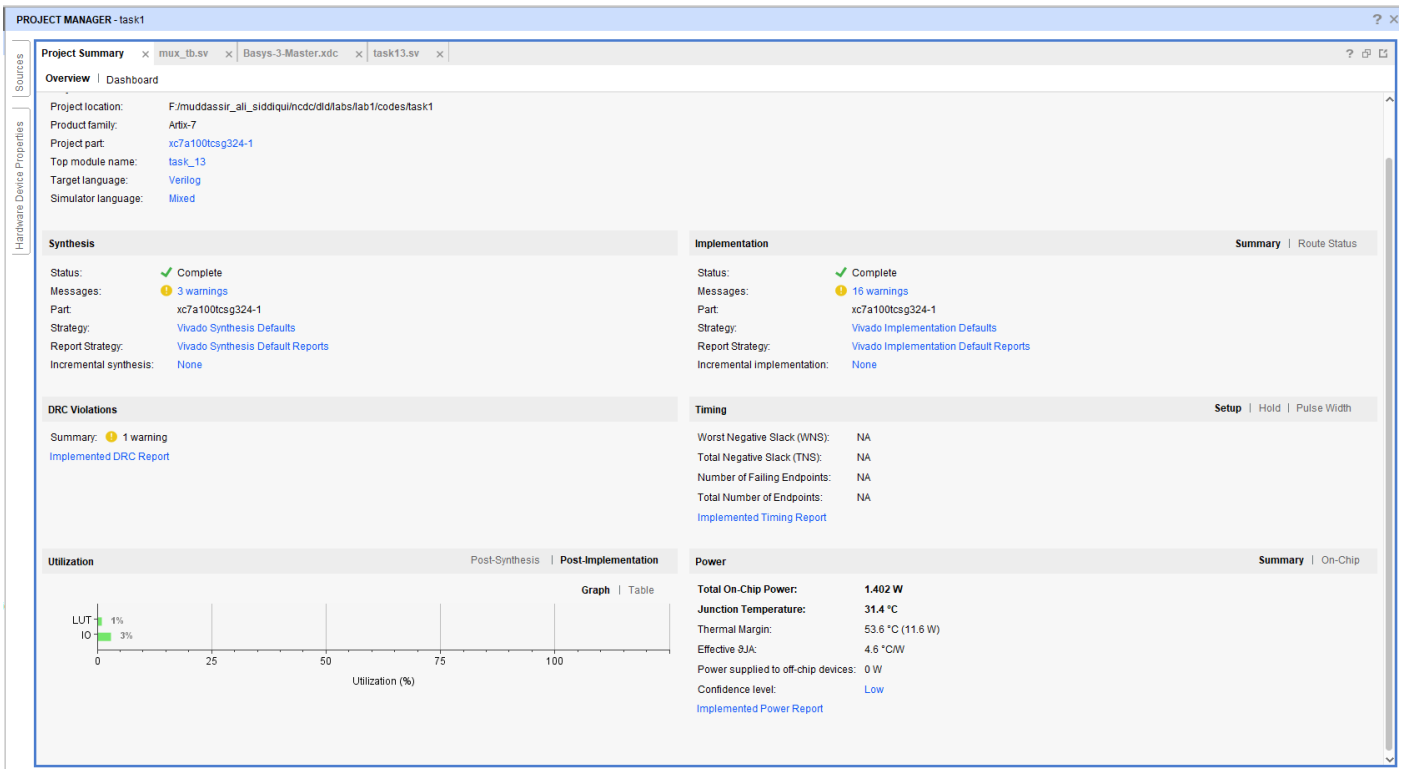
Instructor	*Sir Musaddiq Hussain & Sir Bilal*
Date	*30th July 2025*

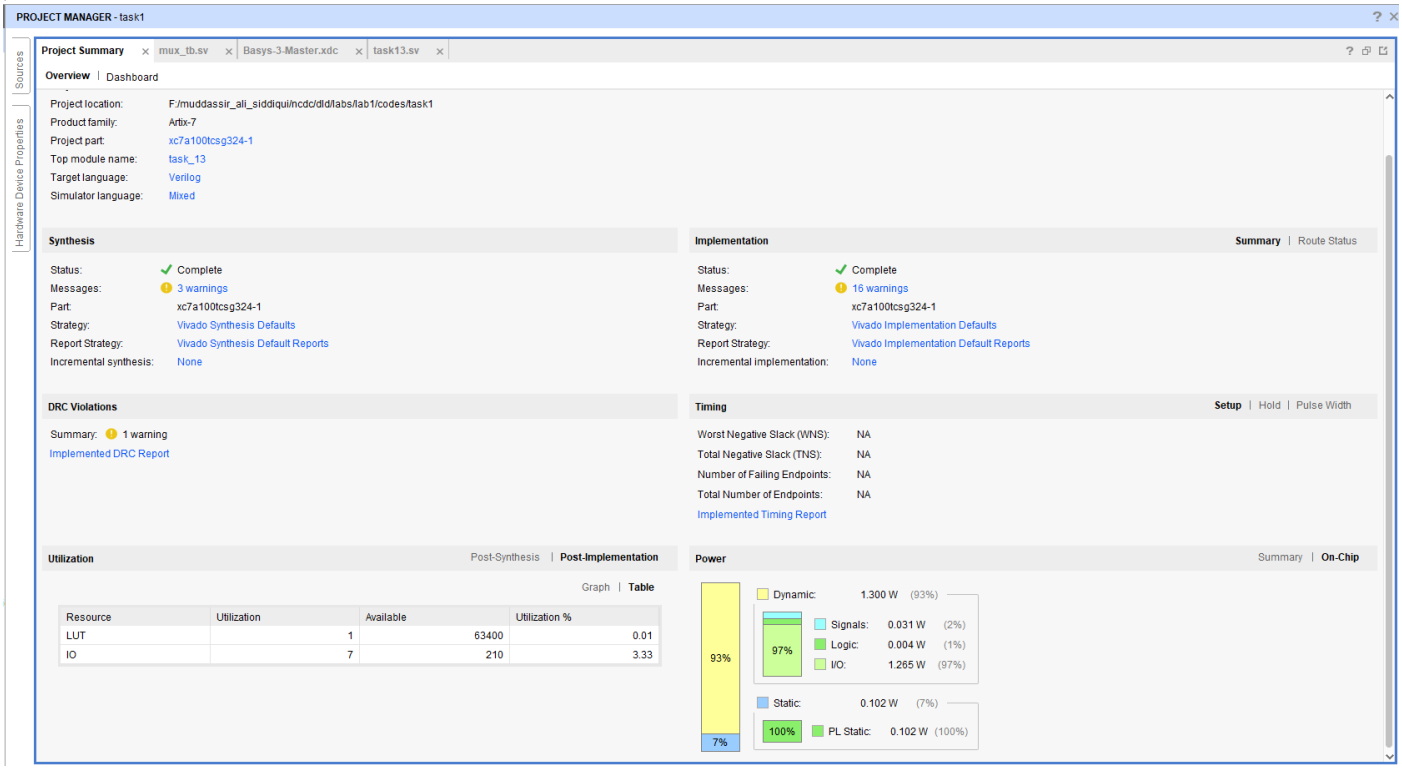
1. In-Lab Tasks: (Write your lab task & screenshots here)

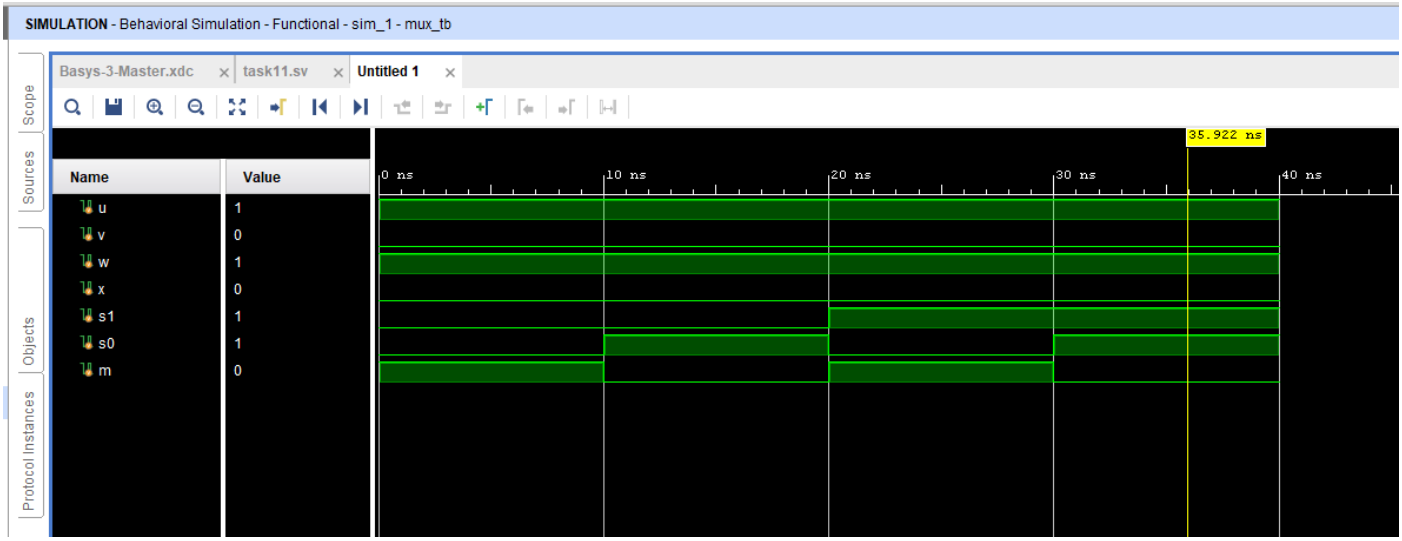
i. Task 1:



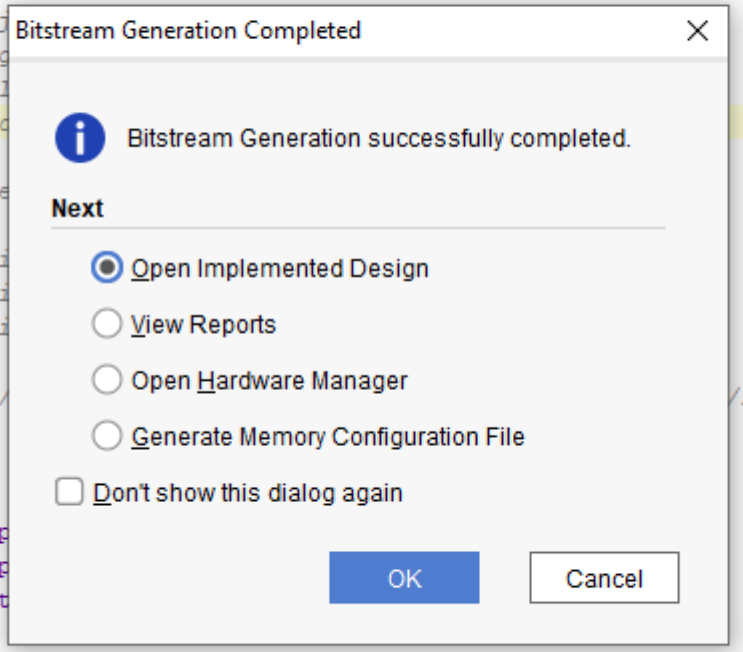


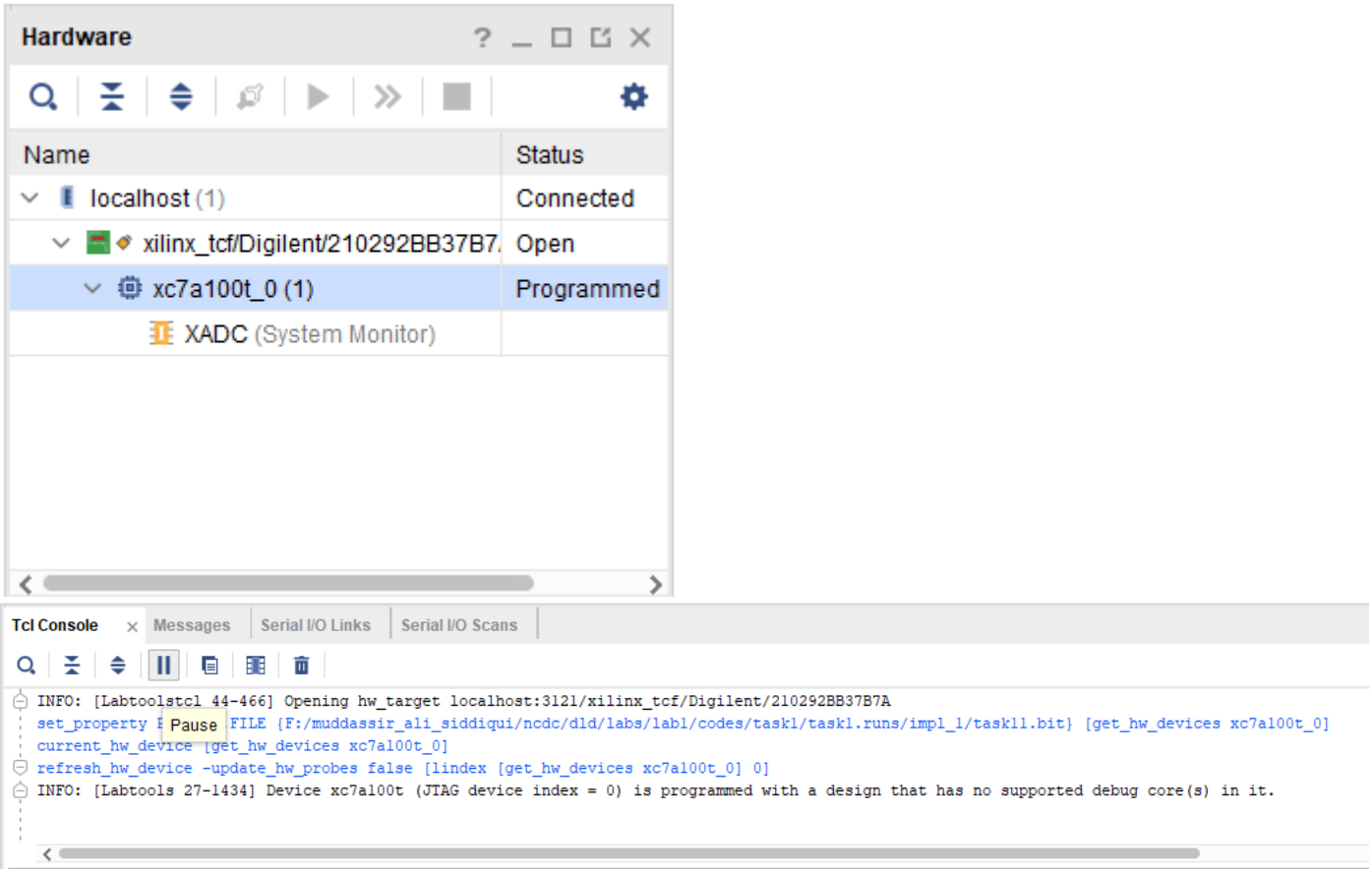

PROJECT MANAGER - task1
Project Summary
mux_tb.sv
Basys-3-Master.xdc
task13.sv
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task1
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: task_13
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 3 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 16 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
IO 3%
0
25
50
75
100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 1.402 W
Junction Temperature: 31.4 °C
Thermal Margin: 53.6 °C (11.6 W)
Effective ϑJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report

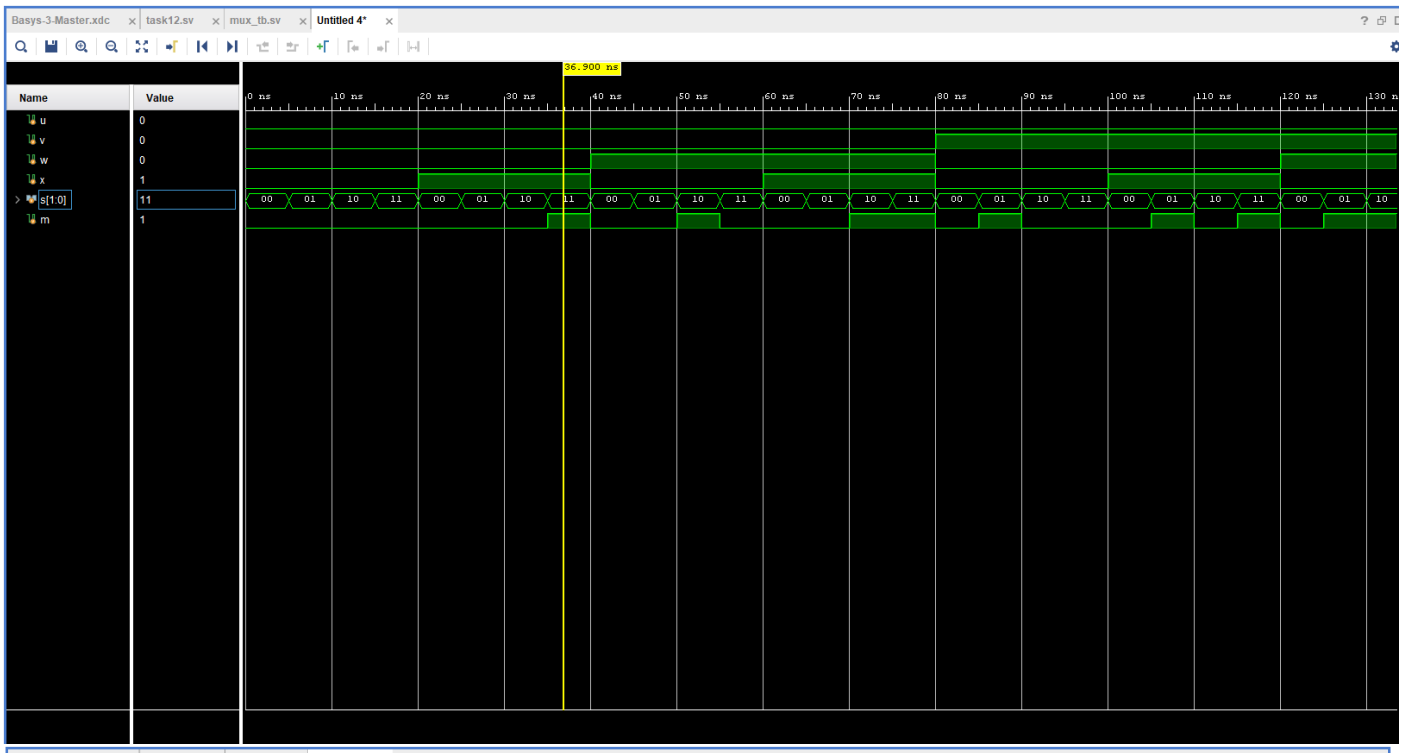

PROJECT MANAGER - task1
Project Summary
mux_tb.sv
Basys-3-Master.xdc
task13.sv
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task1
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: task_13
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 3 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 16 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource | Utilization | Available | Utilization %
LUT | 1 | 63400 | 0.01
IO | 7 | 210 | 3.33
Power
Summary | On-Chip
93%
7%
Dynamic: 1.300 W (93%)
97%
Signals: 0.031 W (2%)
Logic: 0.004 W (1%)
I/O: 1.265 W (97%)
Static: 0.102 W (7%)
100%
PL Static: 0.102 W (100%)

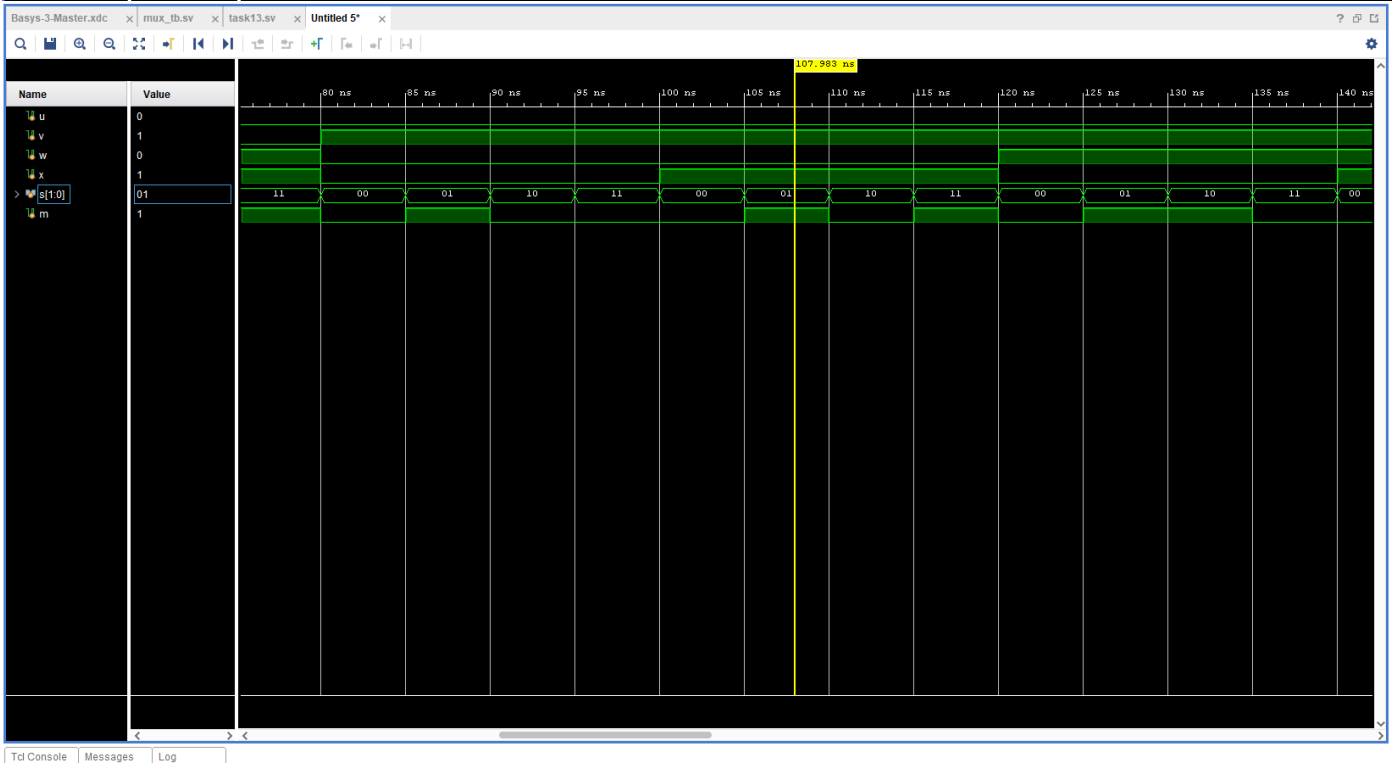



```
1  //`timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 07/28/2025 08:20:20 PM
7  // Design Name:
8  // Module Name: task11
9  // Proj
10 // Targ
11 // Tool
12 // Desc
13 //
14 // Depe
15 //
16 // Revi
17 // Revi
18 // Addi
19 //
20 //////
21
22
23 module
24     inp
25     inp
26     out
27 );
28     logic n0, n1, n2, n3, s0n, s1n;
29
30     not (s0n, s0);
```

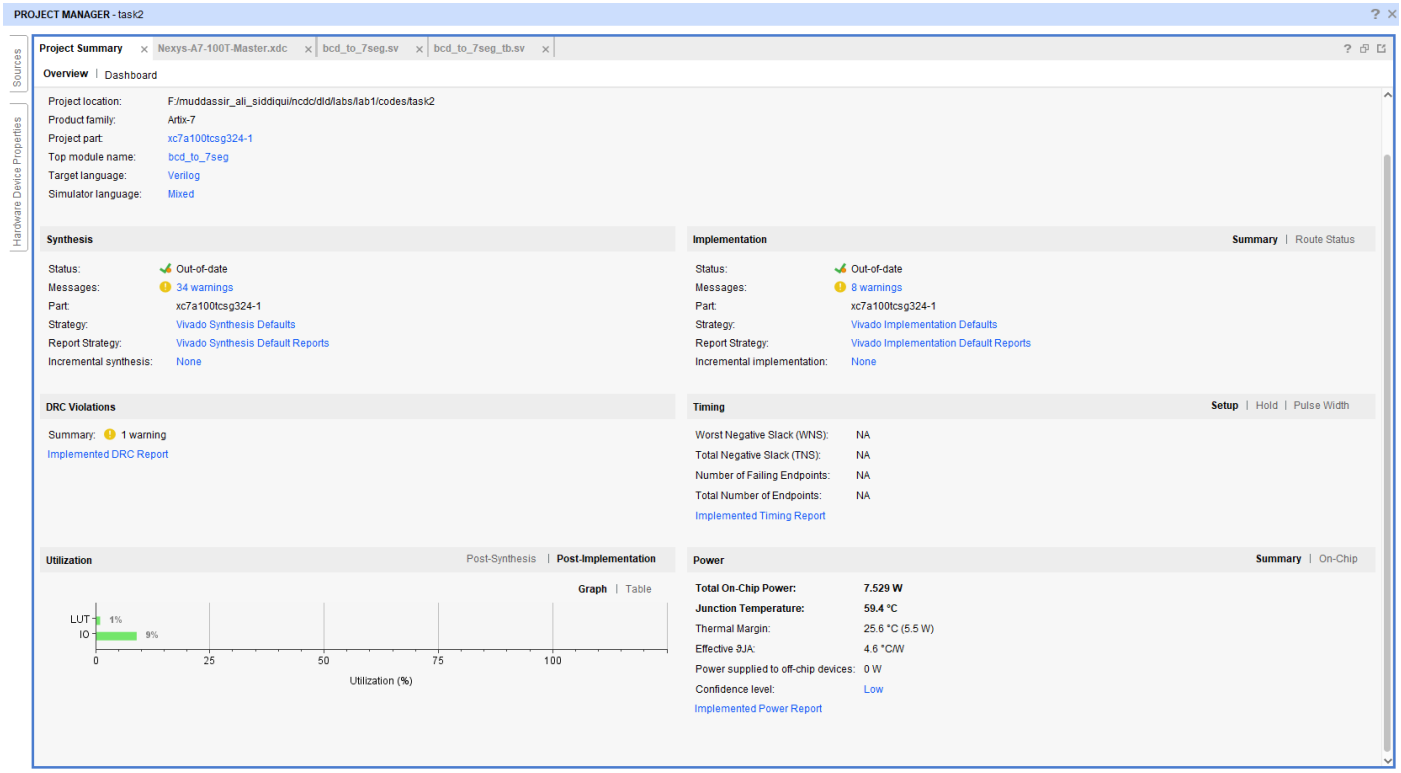


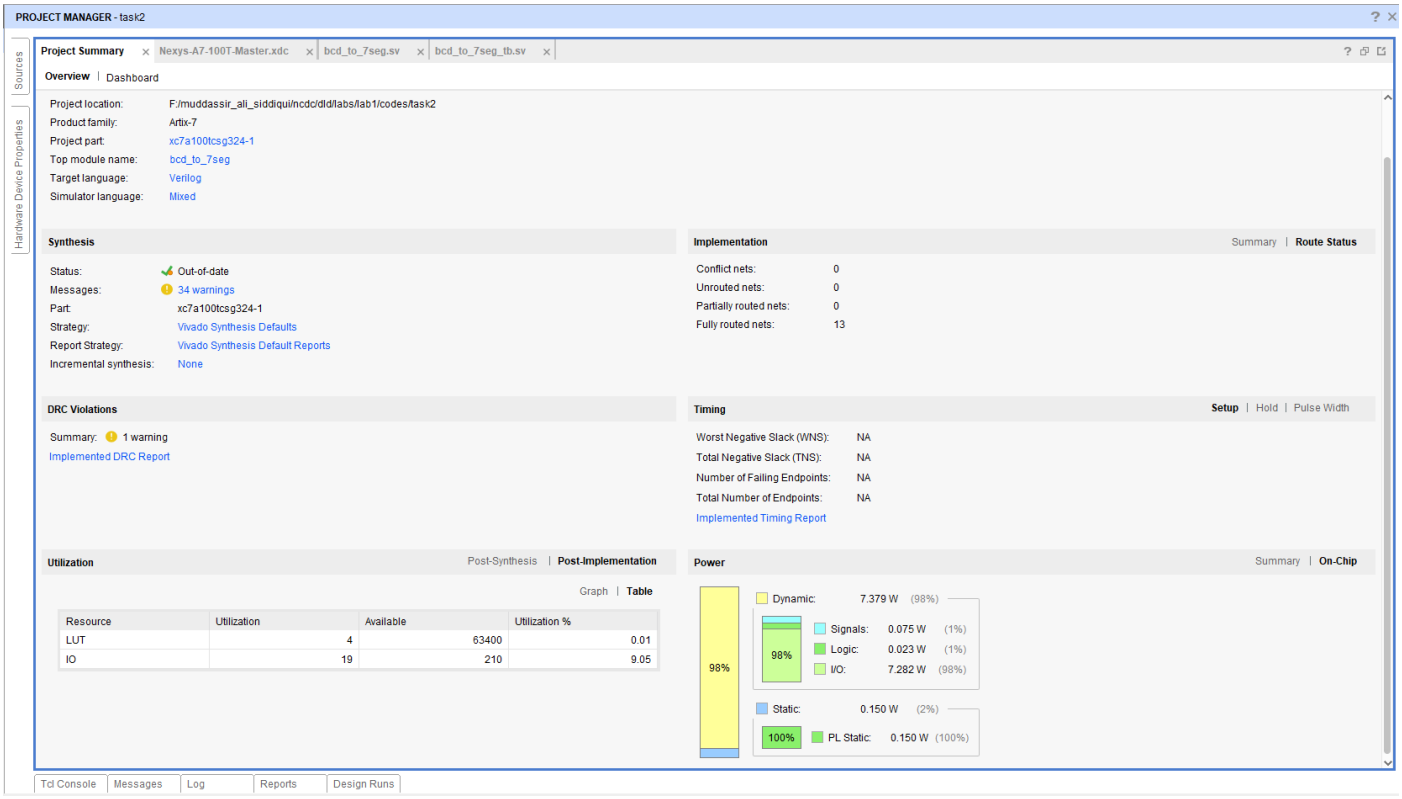

Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210292BB37B7
Open
xc7a100t_0 (1)
Programmed
XADC (System Monitor)
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
Pause
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210292BB37B7A
set_property PROGRAM.FILE {F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task1/task1.runs/impl_1/task11.bit} [get_hw_devices xc7a100t_0]
current_hw_device [get_hw_devices xc7a100t_0]
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7a100t_0] 0]
INFO: [Labtools 27-1434] Device xc7a100t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.

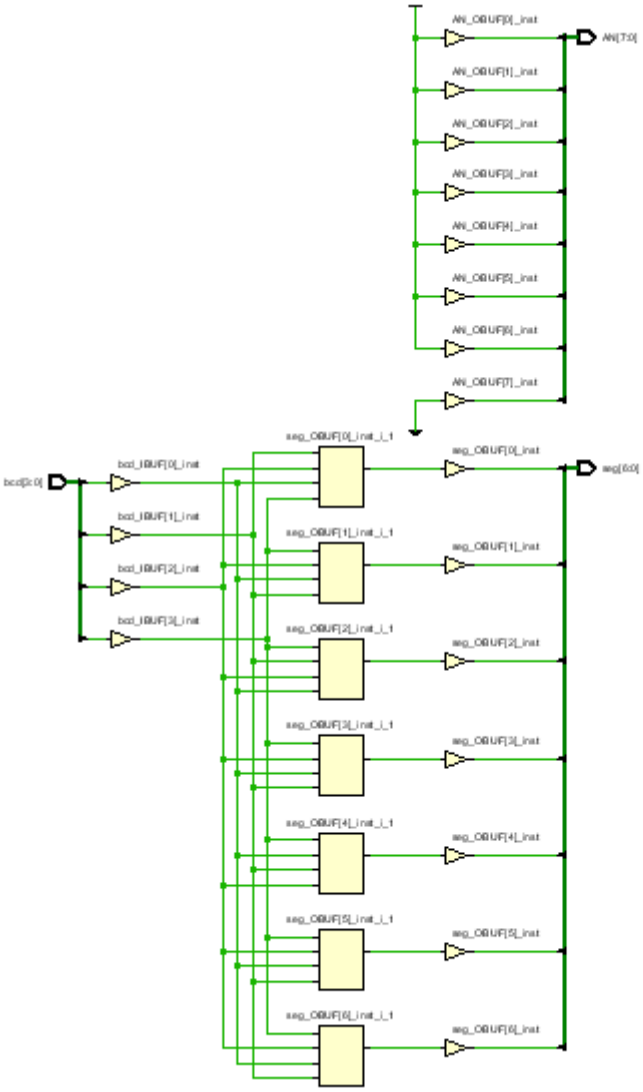

Basys-3-Master.xdc
task12.sv
mux_tb.sv
Untitled 4*
Name
Value
u
v
w
x
s[1:0]
m
0
0
0
1
11
1
36.900 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
100 ns
110 ns
120 ns
130 n
00 01 10 11 00 01 10 11 00 01 10 11 00 01 10 11 00 01 10 11 00 01 10 11 00 01 10

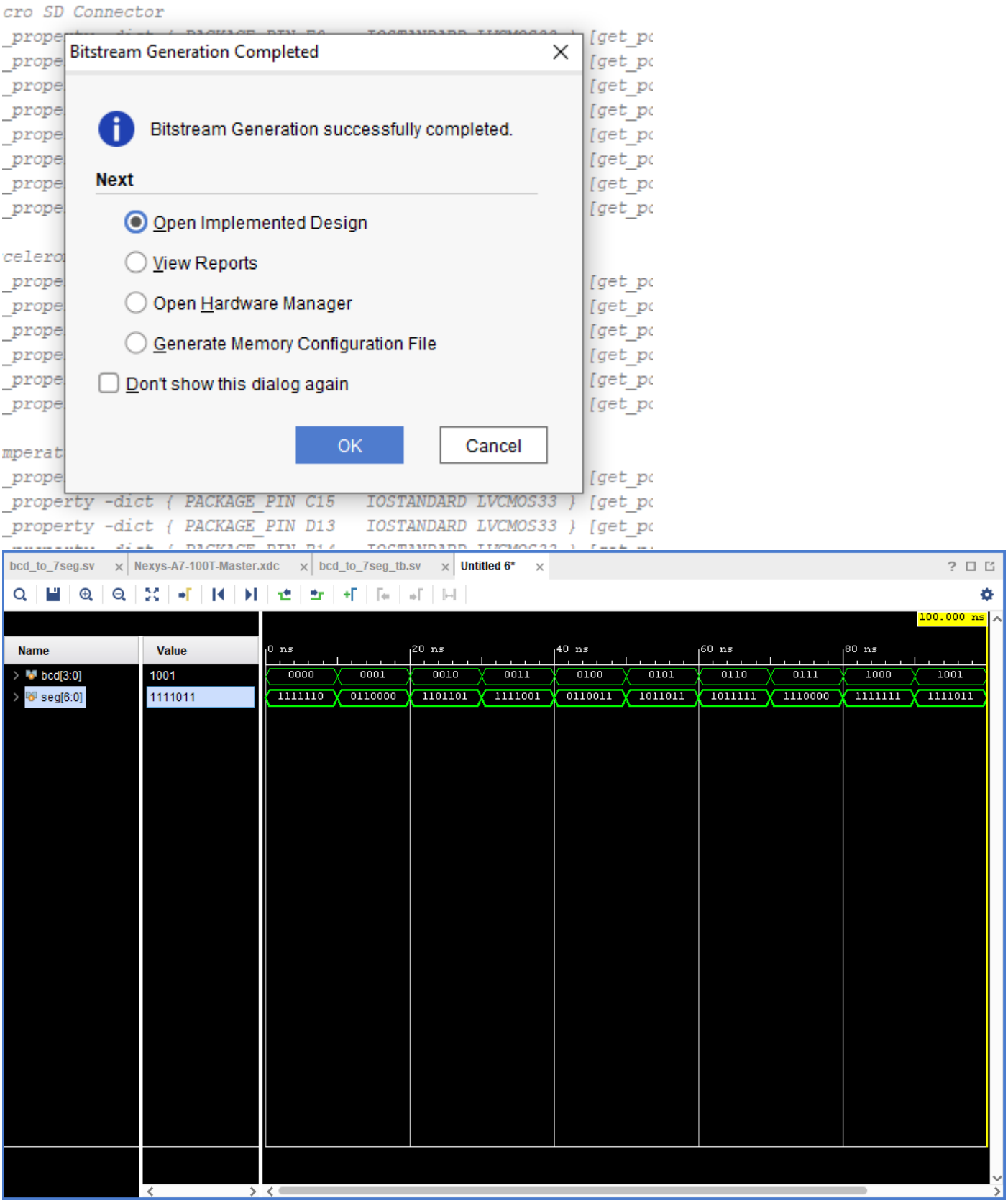

Basys-3-Master.xdc
mux_tb.sv
task13.sv
Untitled 5*
Name
Value
u
v
w
x
s[1:0]
m
0
1
0
1
01
1
107.983 ns
80 ns
85 ns
90 ns
95 ns
100 ns
105 ns
110 ns
115 ns
120 ns
125 ns
130 ns
135 ns
140 ns
11 00 01 10 11 00 01 10 11 00 01 10 11 00
Tcl Console
Messages
Log

ii. Task 2:

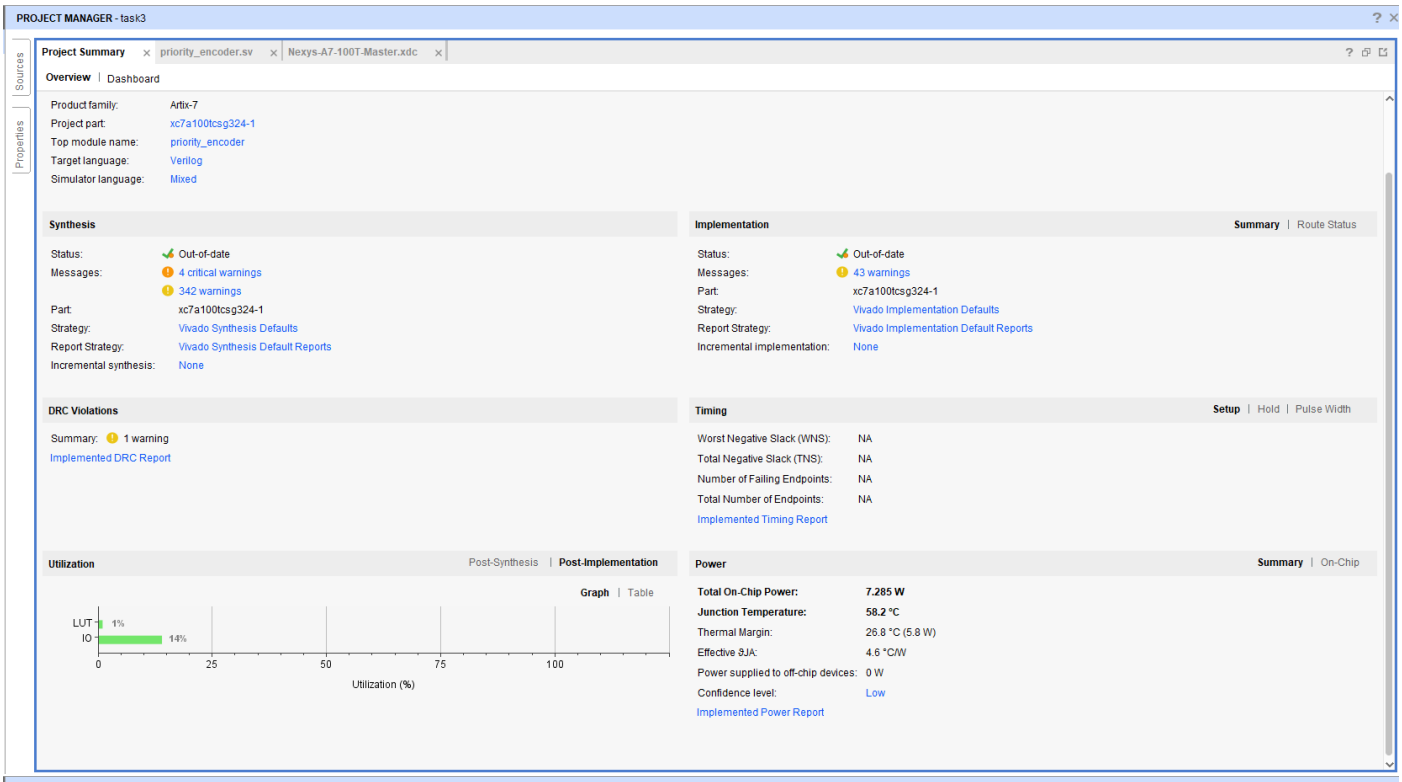

PROJECT MANAGER - task2
Project Summary
Nexys-A7-100T-Master.xdc
bcd_to_7seg.sv
bcd_to_7seg_tb.sv
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task2
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: bcd_to_7seg
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Out-of-date
Messages: 34 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Out-of-date
Messages: 8 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
IO 9%
0 25 50 75 100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 7.529 W
Junction Temperature: 59.4 °C
Thermal Margin: 25.6 °C (5.5 W)
Effective ϑJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report

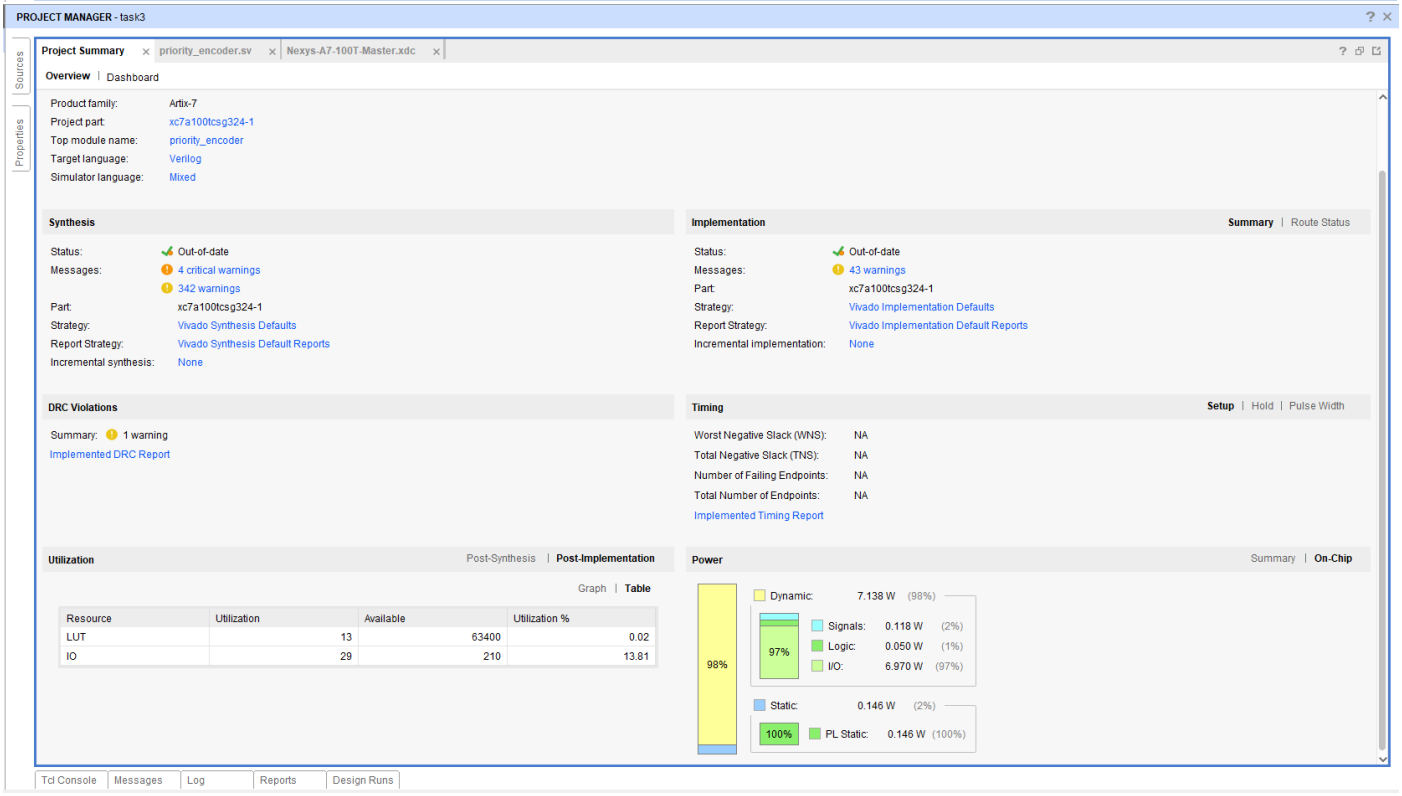

PROJECT MANAGER - task2
Project Summary
Nexys-A7-100T-Master.xdc
bcd_to_7seg.sv
bcd_to_7seg_tb.sv
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task2
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: bcd_to_7seg
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Out-of-date
Messages: 34 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Conflict nets: 0
Unrouted nets: 0
Partially routed nets: 0
Fully routed nets: 13
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 4 63400 0.01
IO 19 210 9.05
Power
Summary | On-Chip
98%
Dynamic: 7.379 W (98%)
98%
Signals: 0.075 W (1%)
Logic: 0.023 W (1%)
I/O: 7.282 W (98%)
Static: 0.150 W (2%)
100%
PL Static: 0.150 W (100%)
Tcl Console
Messages
Log
Reports
Design Runs

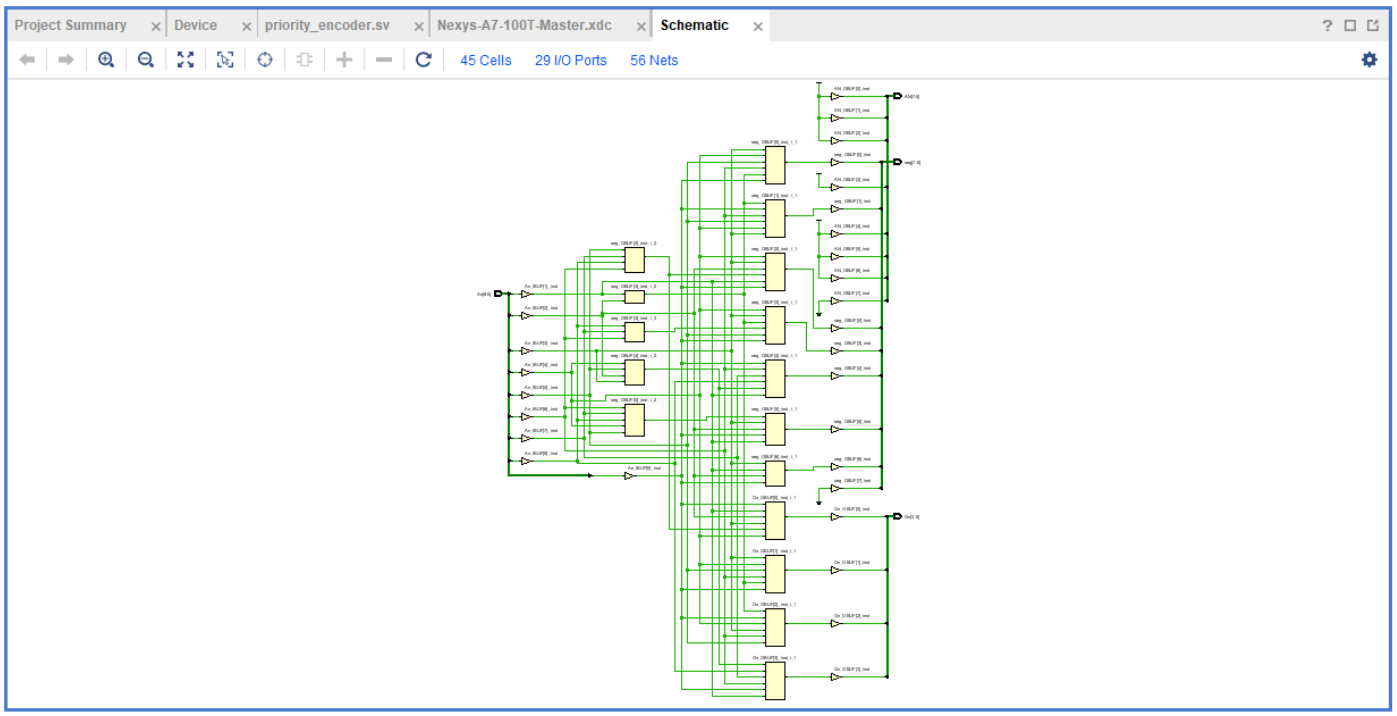


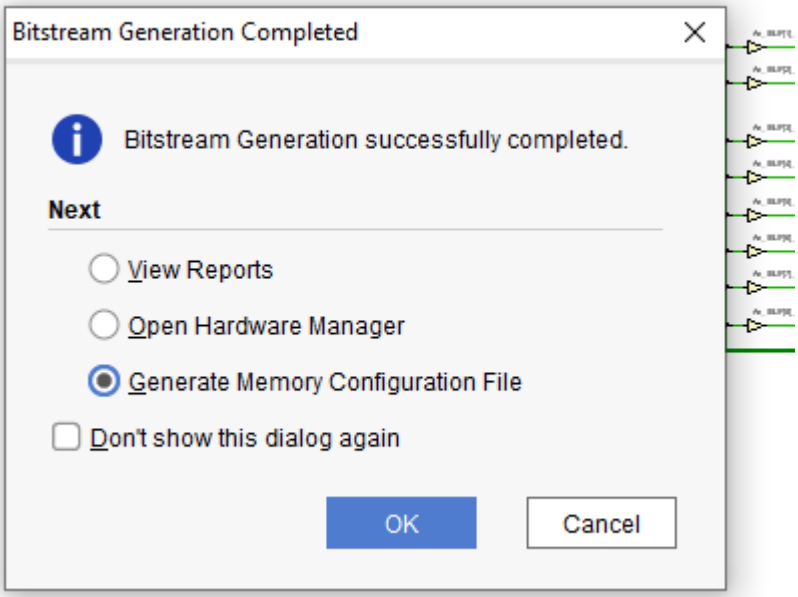

cro SD Connector
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel
_property -dict { PACKAGE_PIN C15 IOSTANDARD LVCMOS33 }
_property -dict { PACKAGE_PIN D13 IOSTANDARD LVCMOS33 }
bcd_to_7seg.sv
Nexys-A7-100T-Master.xdc
bcd_to_7seg_tb.sv
Untitled 6*
100.000 ns
Name
Value
bcd[3:0]
1001
seg[6:0]
1111011
0 ns
20 ns
40 ns
60 ns
80 ns
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1111110
0110000
1101101
1111001
0110011
1011011
1011111
1110000
1111111
1111011

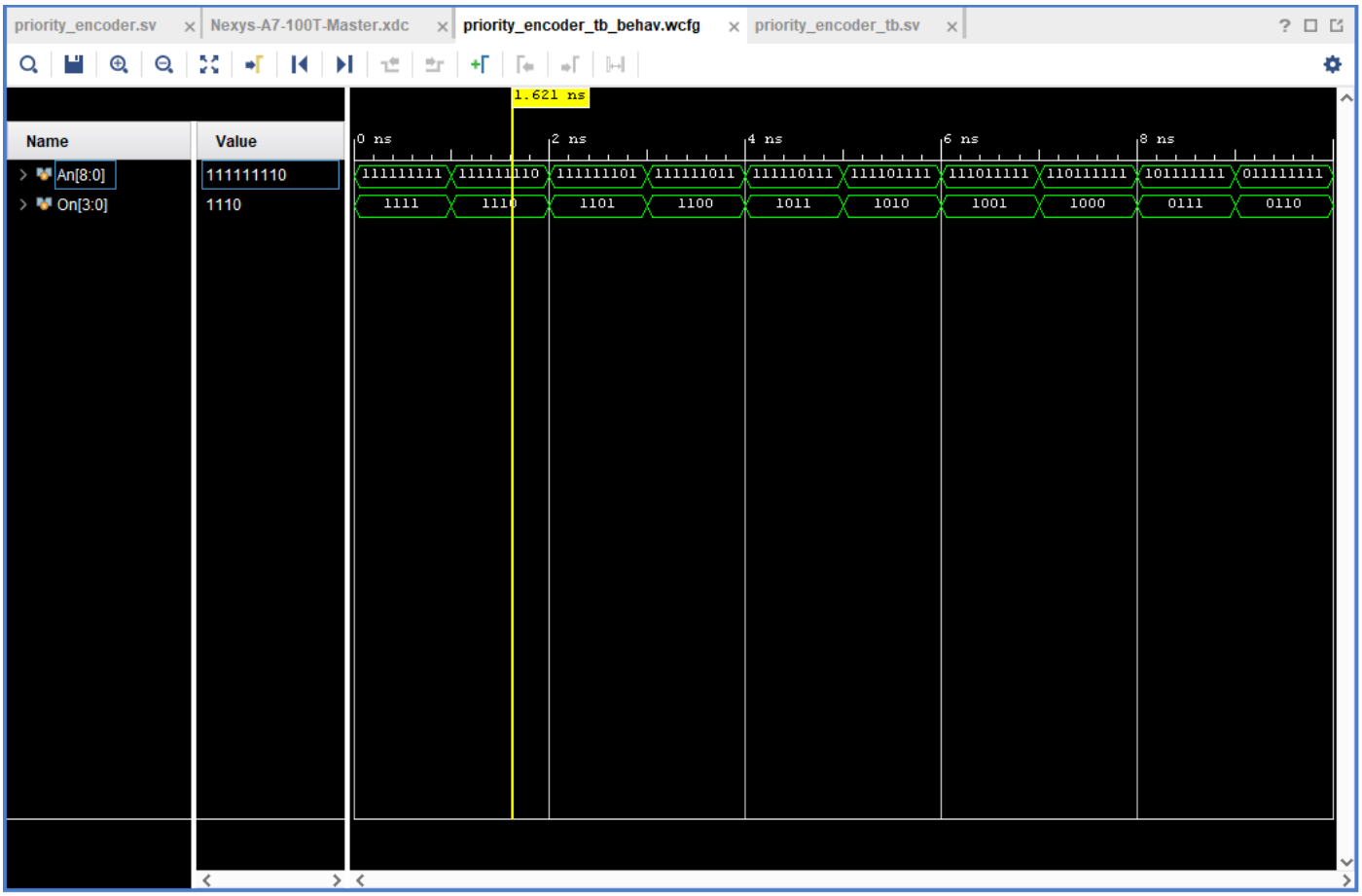
iii. Task 3:


PROJECT MANAGER - task3
Project Summary
priority_encoder.sv
Nexys-A7-100T-Master.xdc
Overview | Dashboard
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: priority_encoder
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Out-of-date
Messages: 4 critical warnings
342 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Out-of-date
Messages: 43 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
IO 14%
0 25 50 75 100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 7.285 W
Junction Temperature: 58.2 °C
Thermal Margin: 26.8 °C (5.8 W)
Effective ϑJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report

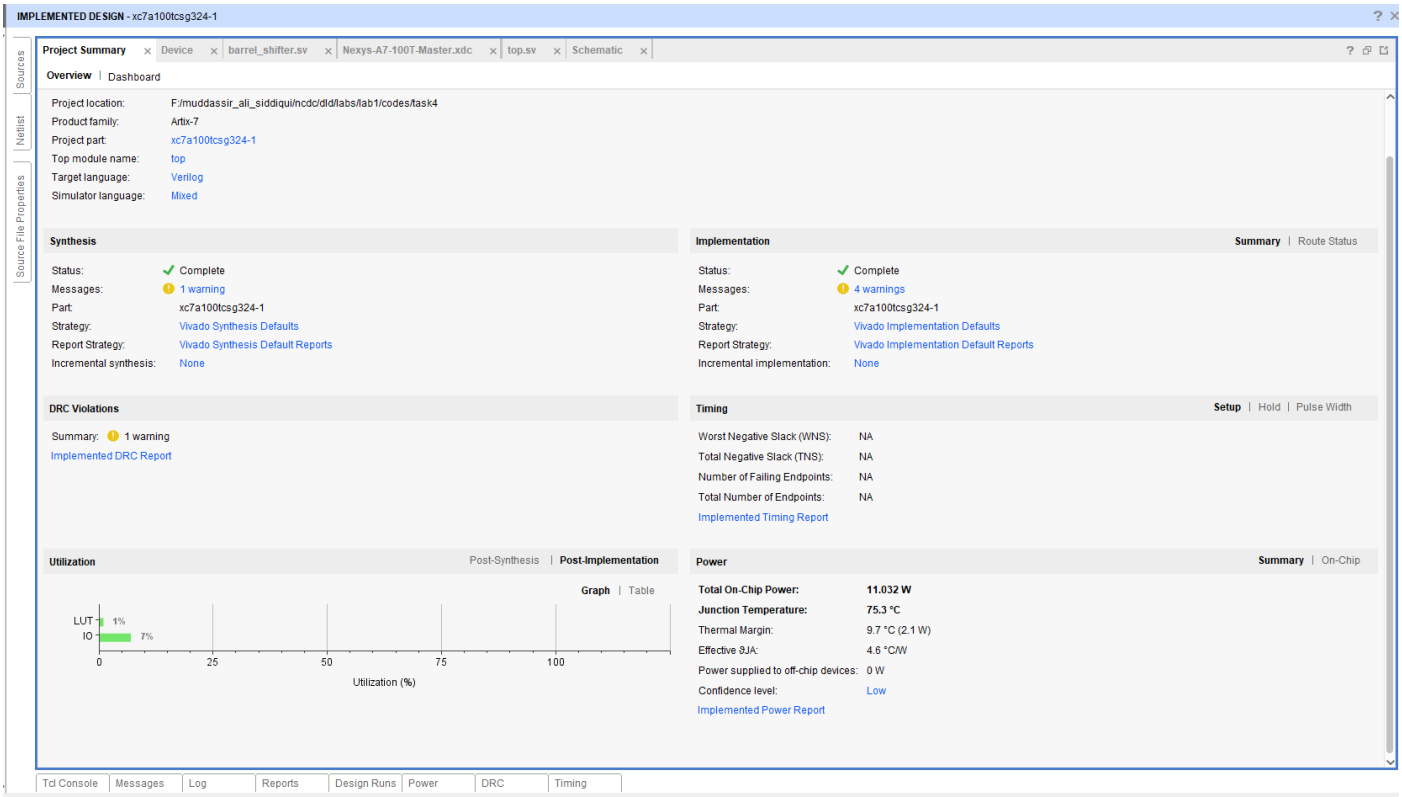

PROJECT MANAGER - task3
Project Summary
priority_encoder.sv
Nexys-A7-100T-Master.xdc
Overview | Dashboard
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: priority_encoder
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Out-of-date
Messages: 4 critical warnings
342 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Out-of-date
Messages: 43 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 13 63400 0.02
IO 29 210 13.81
Power
Summary | On-Chip
98%
Dynamic: 7.138 W (98%)
97%
Signals: 0.118 W (2%)
Logic: 0.050 W (1%)
I/O: 6.970 W (97%)
Static: 0.146 W (2%)
100%
PL Static: 0.146 W (100%)
Tcl Console
Messages
Log
Reports
Design Runs

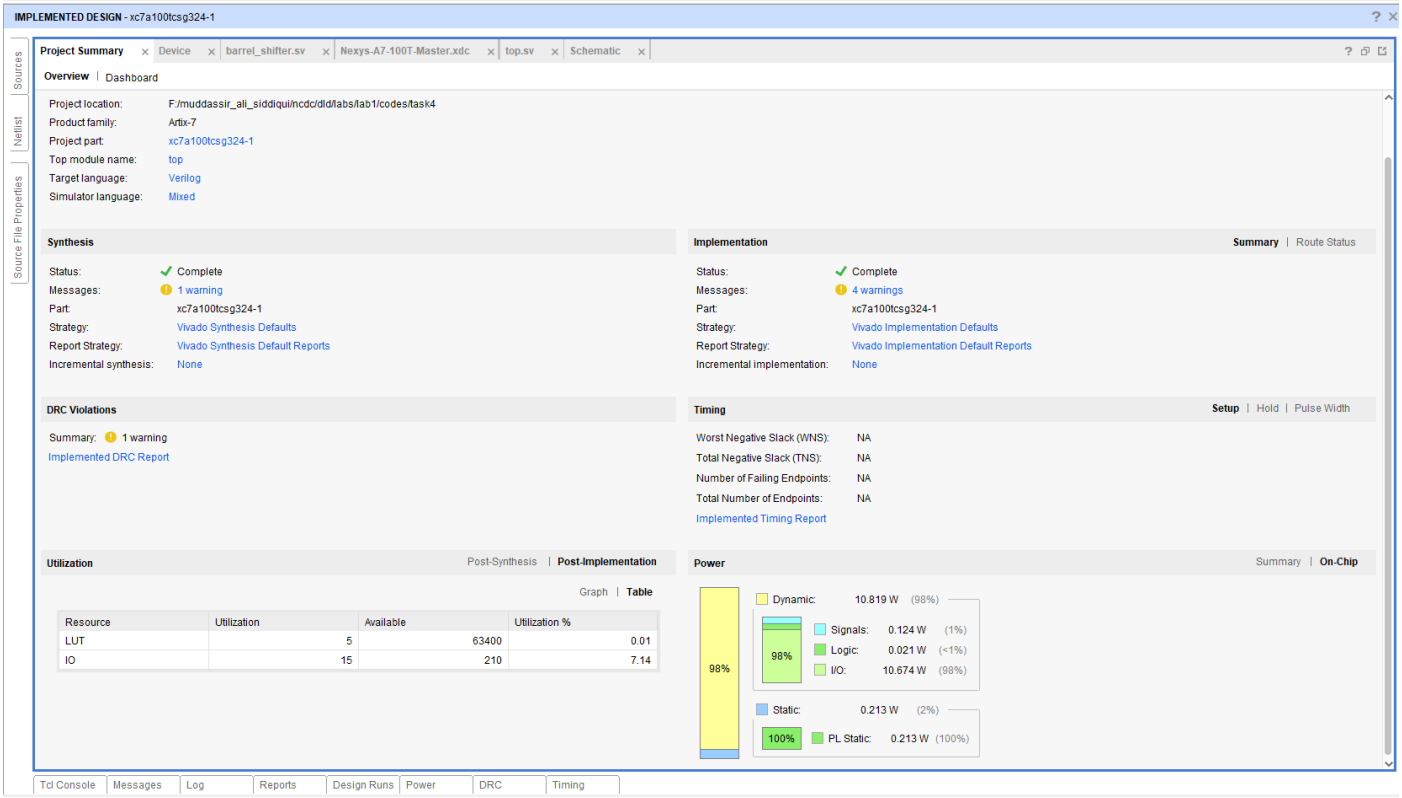

Project Summary
Device
priority_encoder.sv
Nexys-A7-100T-Master.xdc
Schematic
45 Cells
29 I/O Ports
56 Nets

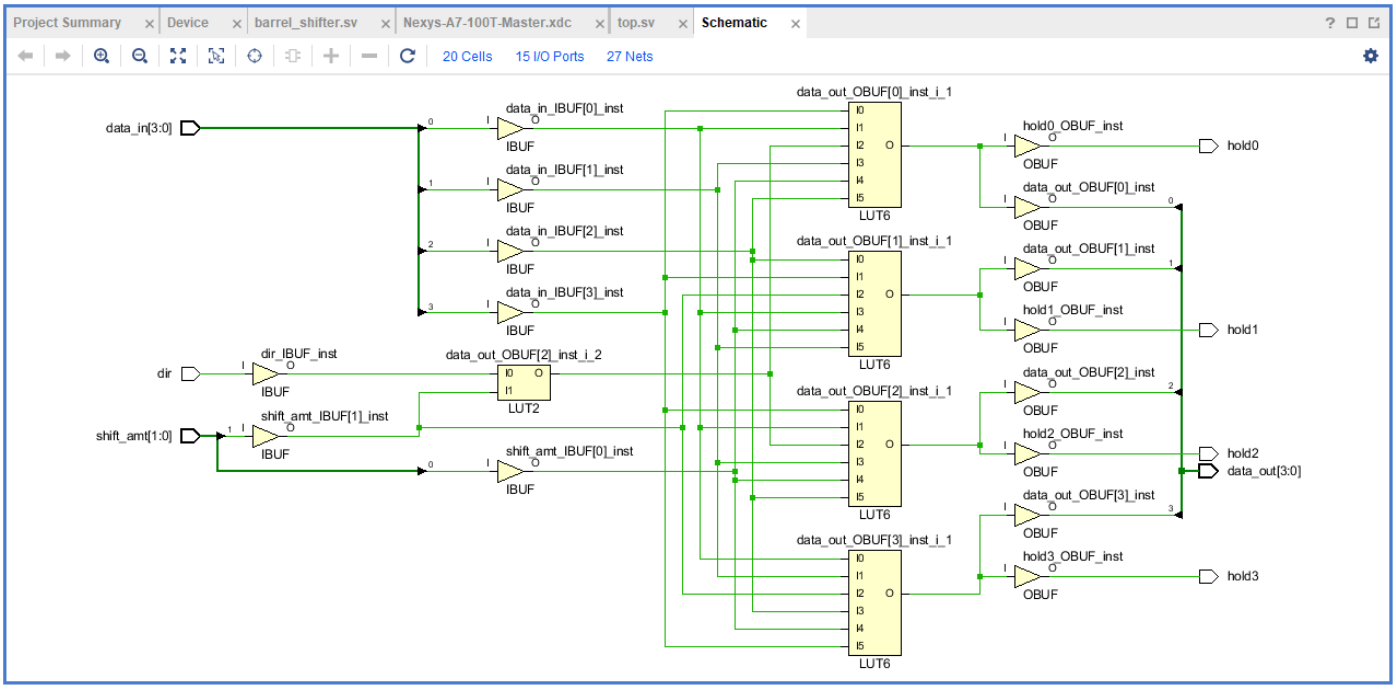

Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel


priority_encoder.sv
Nexys-A7-100T-Master.xdc
priority_encoder_tb_behav.wcfg
priority_encoder_tb.sv
1.621 ns
Name
Value
An[8:0]
111111110
On[3:0]
1110
0 ns
2 ns
4 ns
6 ns
8 ns
111111111
111111110
111111101
111111011
111110111
111101111
111011111
110111111
101111111
011111111
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110

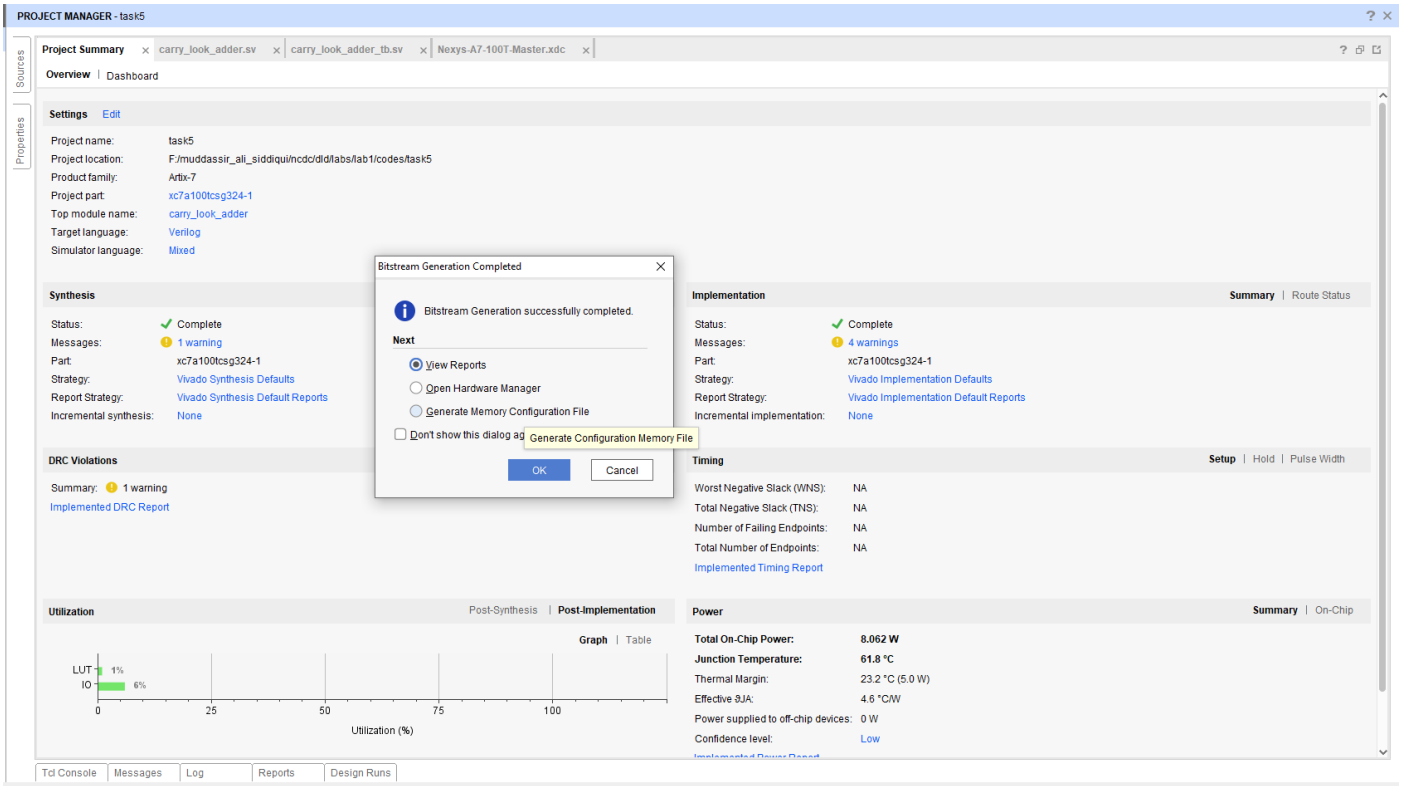
iv. Task 4:

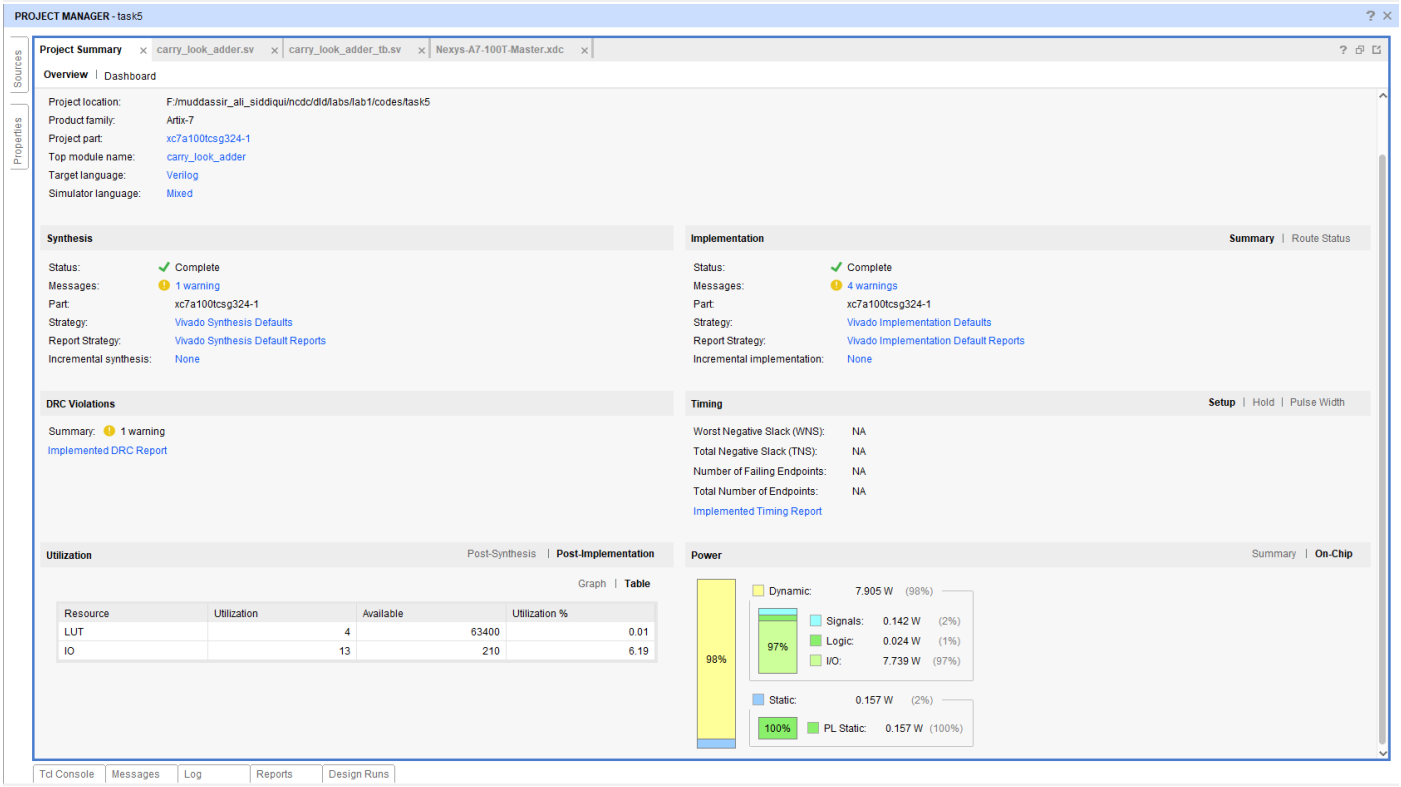

IMPLEMENTED DESIGN - xc7a100tcsg324-1
Project Summary
Device
barrel_shifter.sv
Nexys-A7-100T-Master.xdc
top.sv
Schematic
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task4
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: top
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 1 warning
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 4 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
IO 7%
0 25 50 75 100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 11.032 W
Junction Temperature: 75.3 °C
Thermal Margin: 9.7 °C (2.1 W)
Effective θJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing

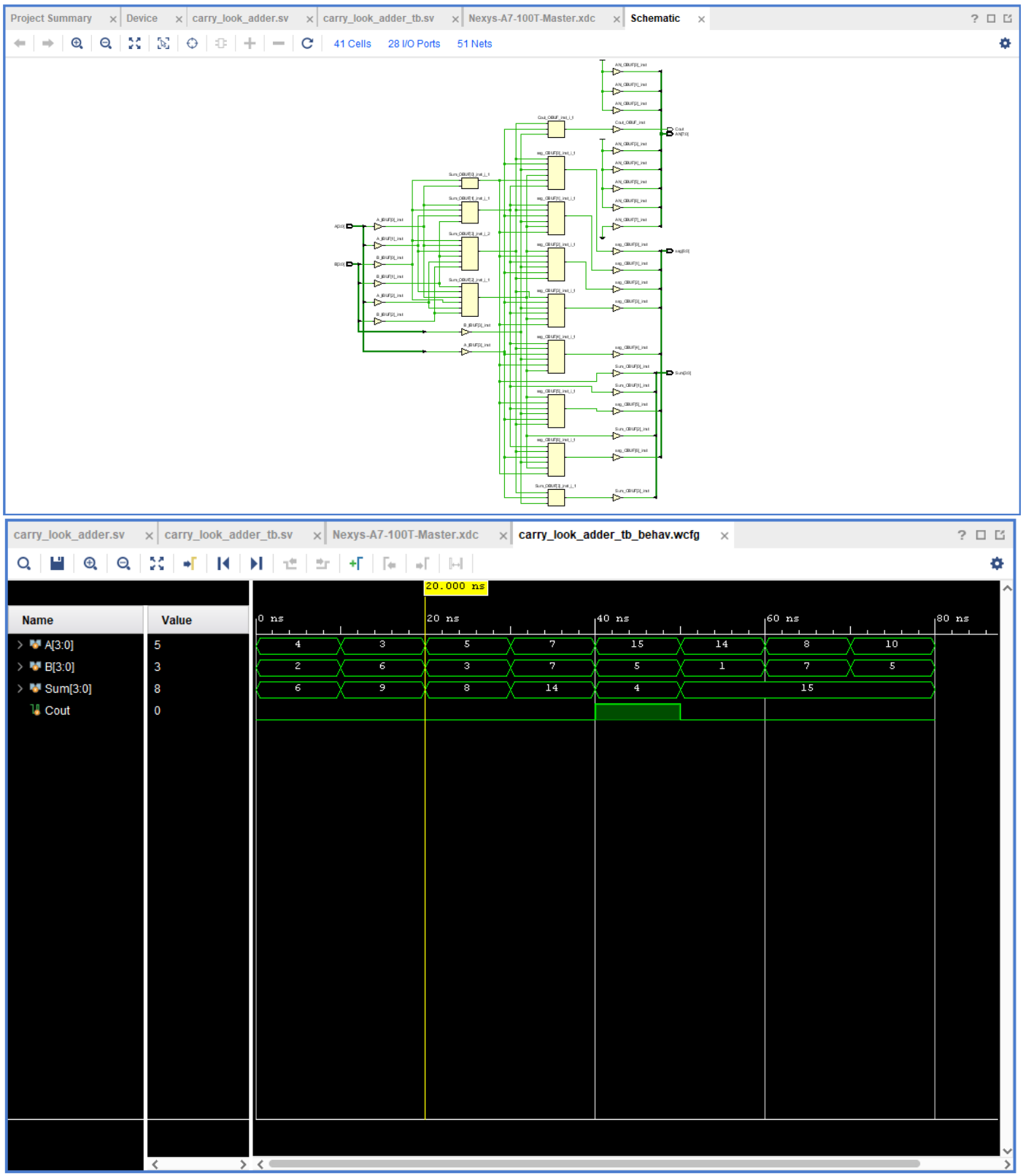

IMPLEMENTED DESIGN - xc7a100tcsg324-1
Project Summary
Device
barrel_shifter.sv
Nexys-A7-100T-Master.xdc
top.sv
Schematic
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task4
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: top
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 1 warning
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 4 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 5 63400 0.01
IO 15 210 7.14
Power
Summary | On-Chip
98%
Dynamic: 10.819 W (98%)
98%
Signals: 0.124 W (1%)
Logic: 0.021 W (<1%)
I/O: 10.674 W (98%)
Static: 0.213 W (2%)
100%
PL Static: 0.213 W (100%)
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing


Project Summary
Device
barrel_shifter.sv
Nexys-A7-100T-Master.xdc
top.sv
Schematic
20 Cells
15 I/O Ports
27 Nets
data_in[3:0]
data_in_IBUF[0]_inst
data_in_IBUF[1]_inst
data_in_IBUF[2]_inst
data_in_IBUF[3]_inst
IBUF
dir
dir_IBUF_inst
shift_amt[1:0]
shift_amt_IBUF[1]_inst
shift_amt_IBUF[0]_inst
data_out_OBUF[2]_inst_i_2
LUT2
data_out_OBUF[0]_inst_i_1
data_out_OBUF[1]_inst_i_1
data_out_OBUF[2]_inst_i_1
data_out_OBUF[3]_inst_i_1
LUT6
hold0_OBUF_inst
hold1_OBUF_inst
hold2_OBUF_inst
hold3_OBUF_inst
data_out_OBUF[0]_inst
data_out_OBUF[1]_inst
data_out_OBUF[2]_inst
data_out_OBUF[3]_inst
OBUF
hold0
hold1
hold2
hold3
data_out[3:0]

v. Task 5:

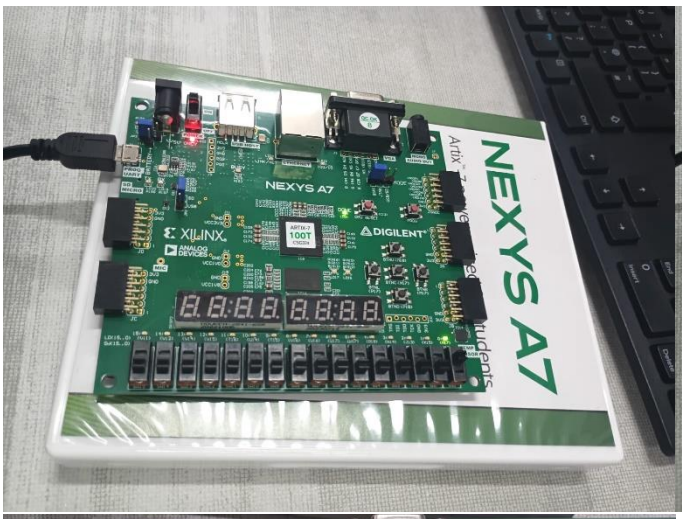

PROJECT MANAGER - task5
Project Summary
carry_look_adder.sv
carry_look_adder_tb.sv
Nexys-A7-100T-Master.xdc
Overview | Dashboard
Settings Edit
Project name: task5
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task5
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: carry_look_adder
Target language: Verilog
Simulator language: Mixed
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog ag
Generate Configuration Memory File
OK
Cancel
Synthesis
Status: Complete
Messages: 1 warning
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 4 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
IO 6%
0
25
50
75
100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 8.062 W
Junction Temperature: 61.8 °C
Thermal Margin: 23.2 °C (5.0 W)
Effective ϑJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Tcl Console
Messages
Log
Reports
Design Runs

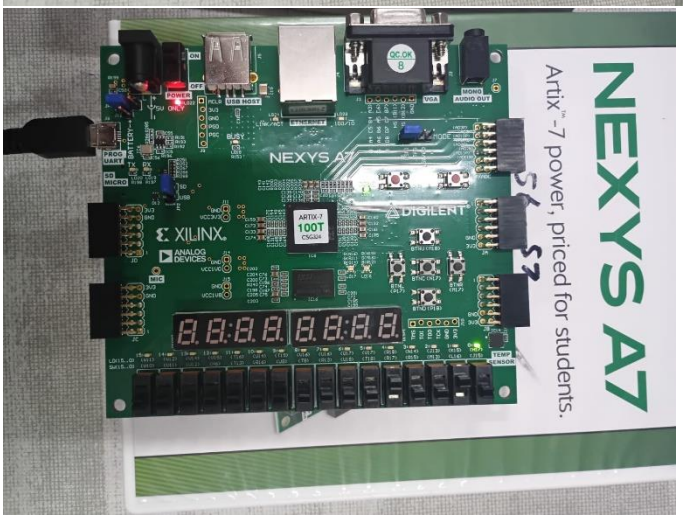

PROJECT MANAGER - task5
Project Summary
carry_look_adder.sv
carry_look_adder_tb.sv
Nexys-A7-100T-Master.xdc
Overview | Dashboard
Project location: F:/muddassir_ali_siddiqui/ncdc/dld/labs/lab1/codes/task5
Product family: Artix-7
Project part: xc7a100tcsg324-1
Top module name: carry_look_adder
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 1 warning
Part: xc7a100tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 4 warnings
Part: xc7a100tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 4 63400 0.01
IO 13 210 6.19
Power
Summary | On-Chip
98%
Dynamic: 7.905 W (98%)
97%
Signals: 0.142 W (2%)
Logic: 0.024 W (1%)
I/O: 7.739 W (97%)
Static: 0.157 W (2%)
100%
PL Static: 0.157 W (100%)
Tcl Console
Messages
Log
Reports
Design Runs


Project Summary
Device
carry_look_adder.sv
carry_look_adder_tb.sv
Nexys-A7-100T-Master.xdc
Schematic
41 Cells
28 I/O Ports
51 Nets
carry_look_adder_tb_behav.wcfg
20.000 ns
Name
Value
A[3:0]
5
B[3:0]
3
Sum[3:0]
8
Cout
0
0 ns
20 ns
40 ns
60 ns
80 ns

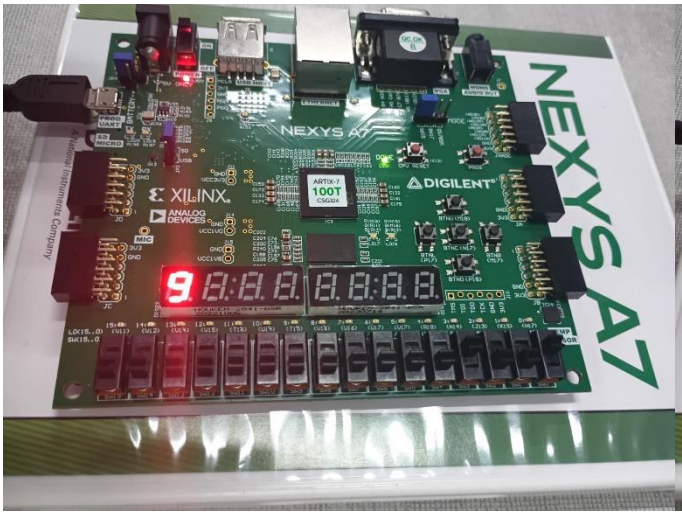
2. FPGA Outputs:

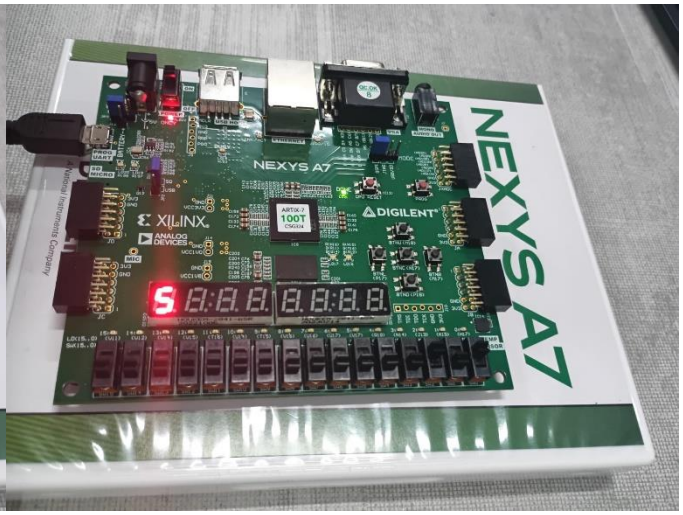
Task 1:



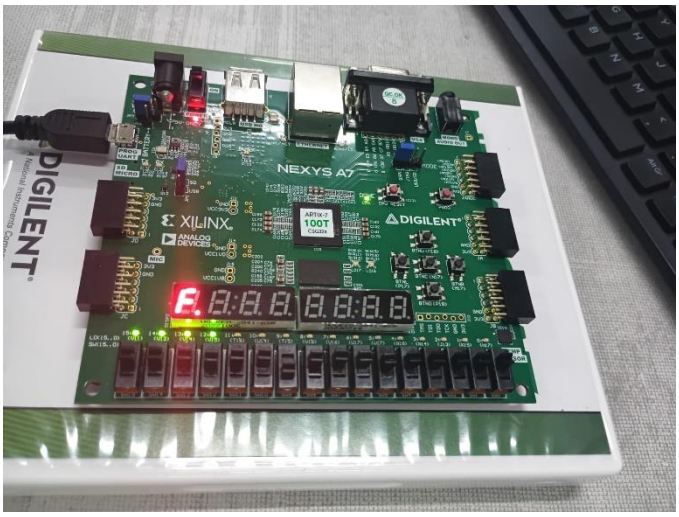


Task 2:

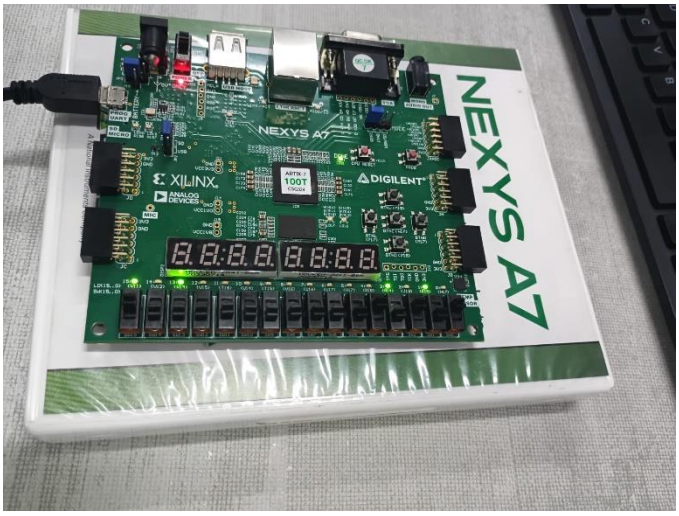




Task 3:



Task 4:



3. Critical Analysis: (Write you critical analysis / conclusion here)

In this lab we design in task 1 mux with 3 different approaches by gate level, case statement and behavioral. In task 2 we convert BCD to seven segment and show output on the FPGA's 7-segment display. In task 3 we perform priority encoder by analyzing the truth table. In task 4 we do barrel shifter left and right by giving the direction to shift. In task 5 carry lookahead adder is performed by me.