



**Digital Logic Design**

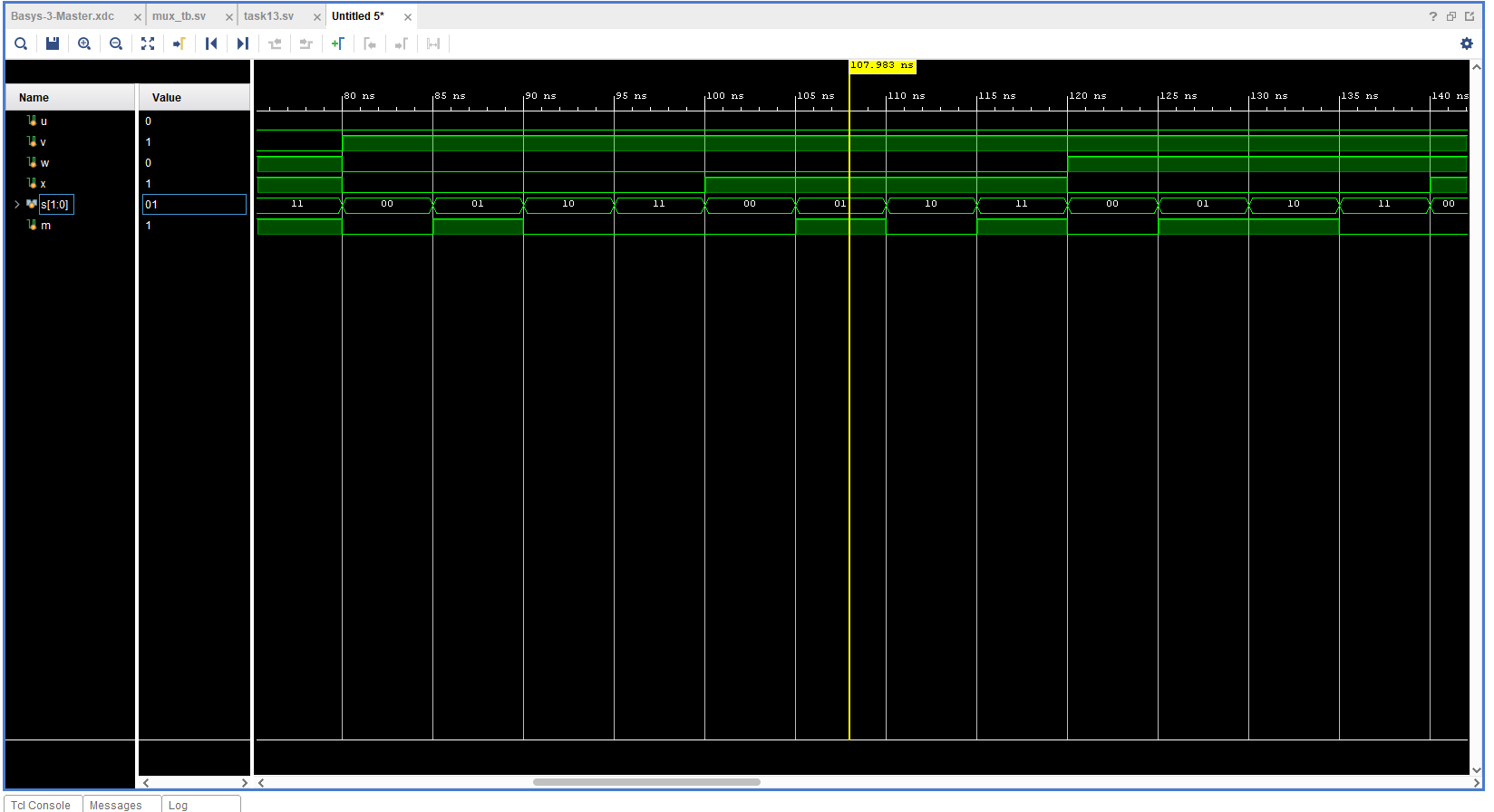
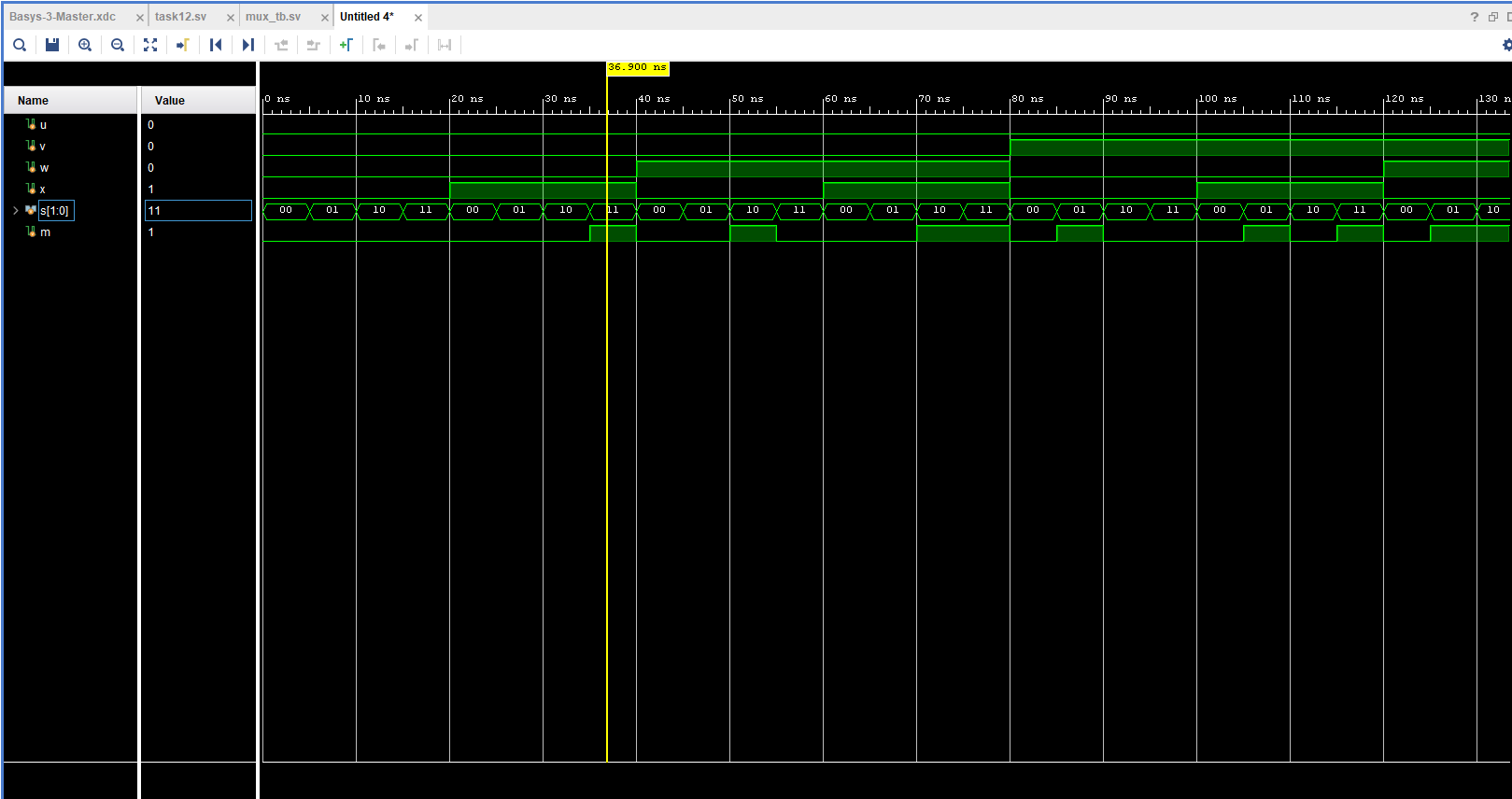
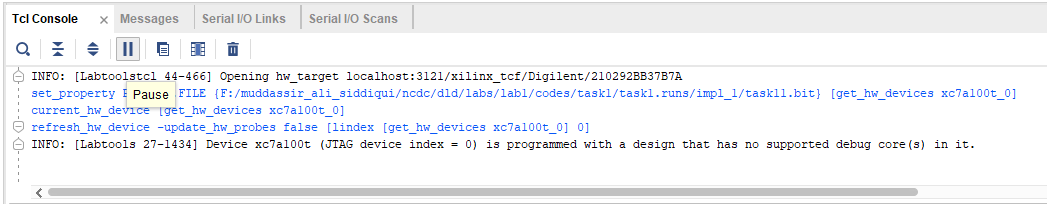
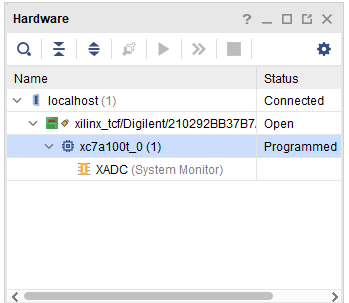
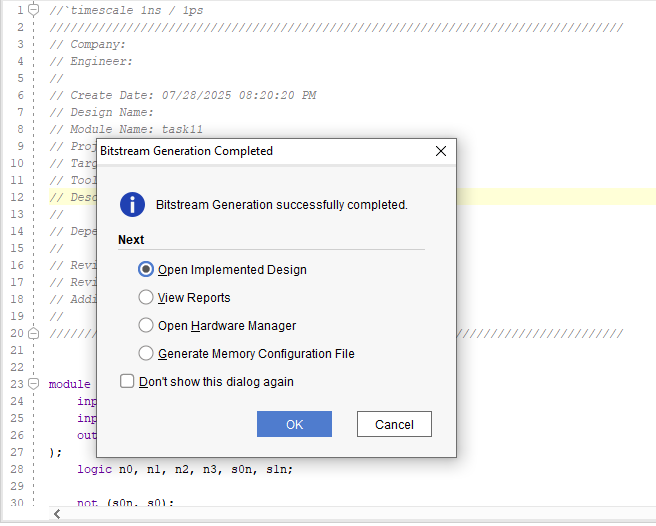
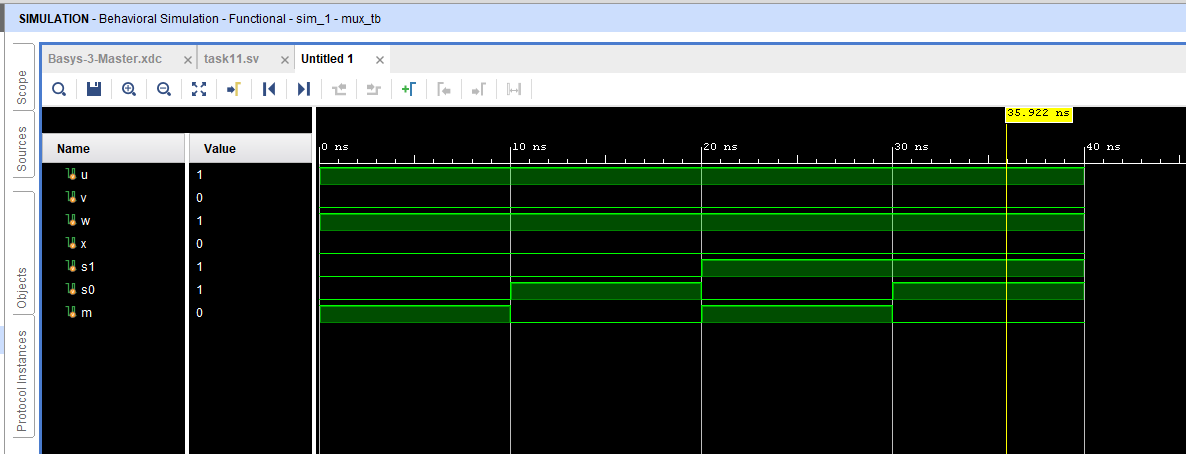
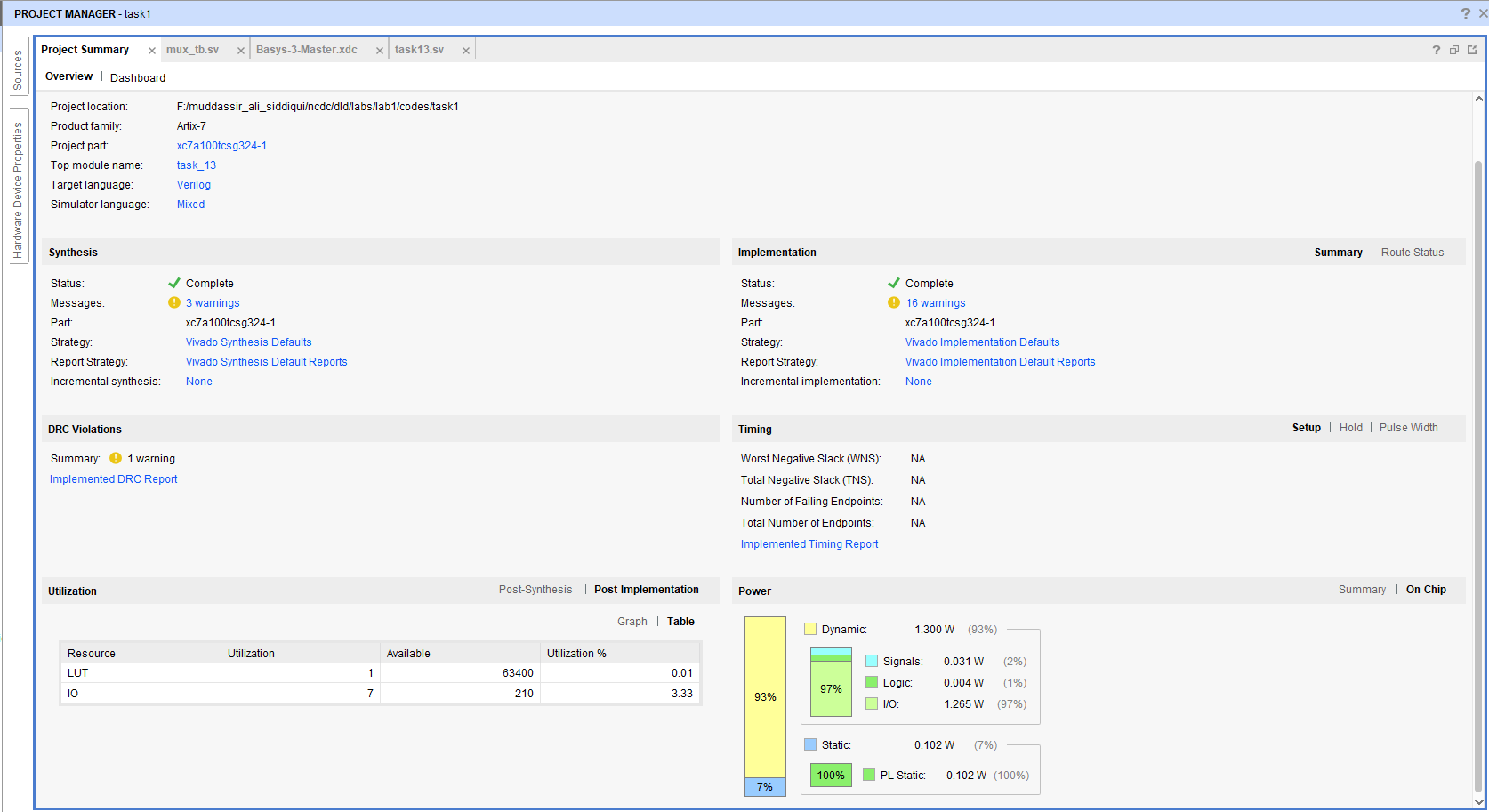
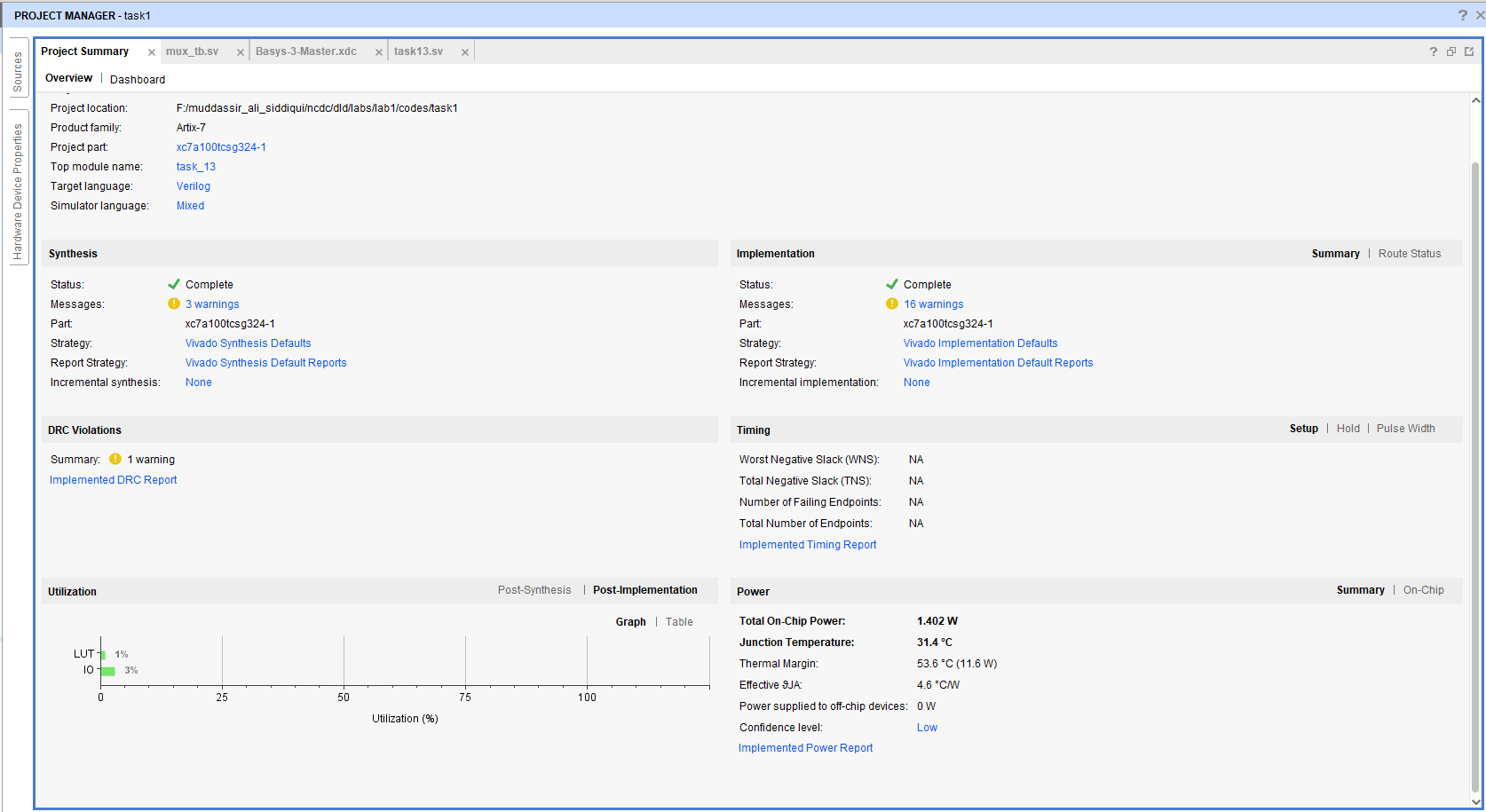
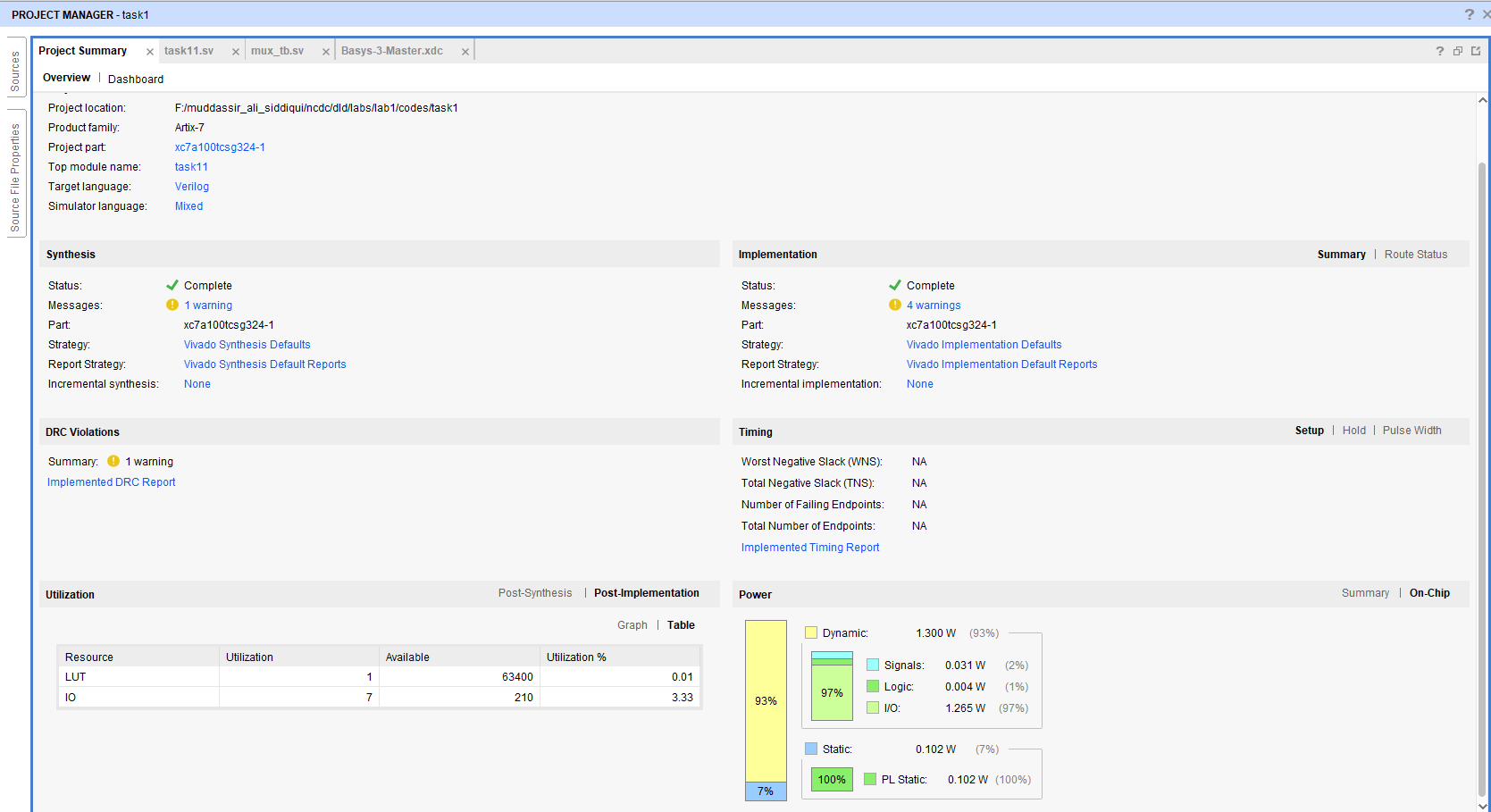
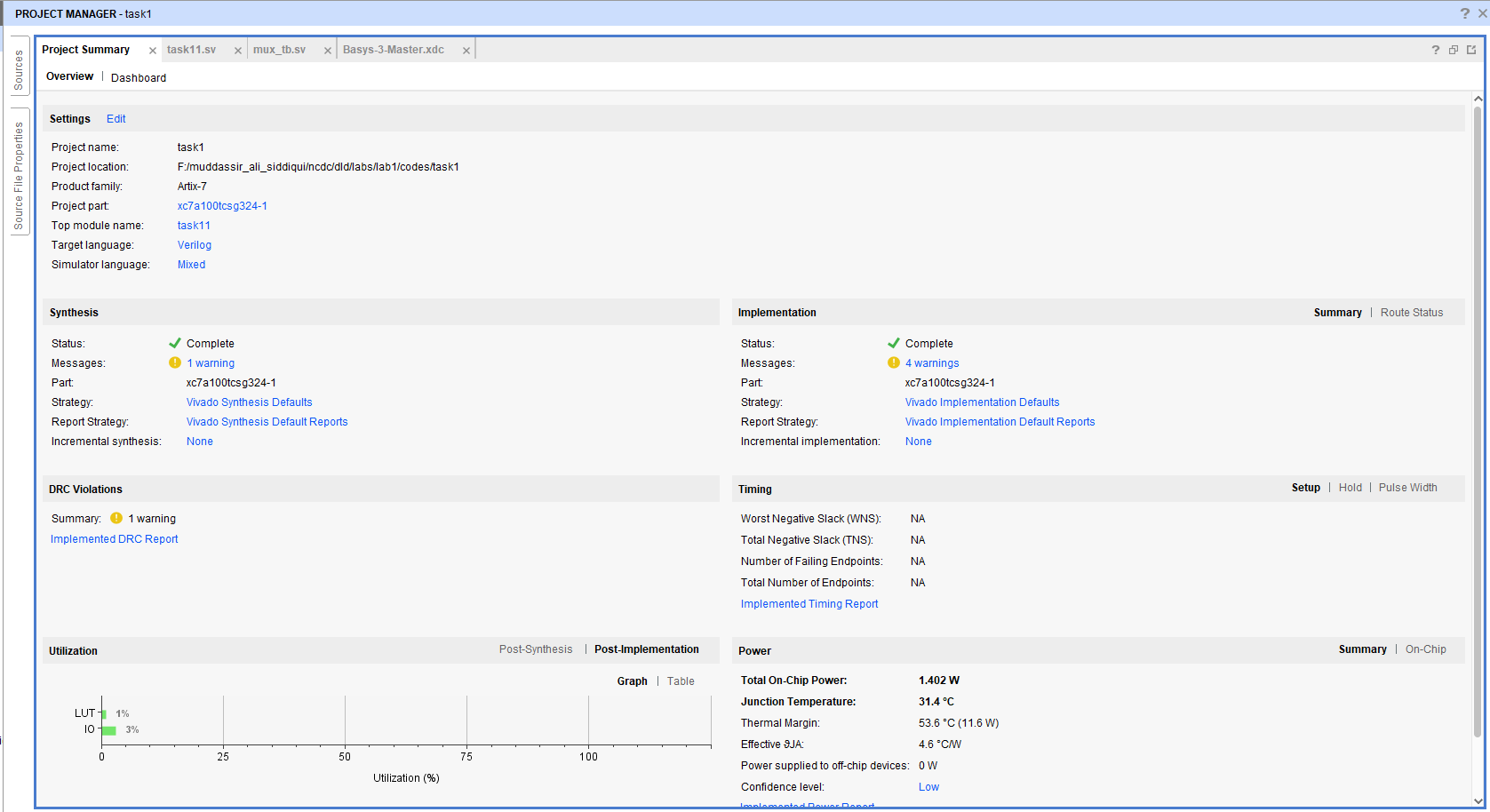
**Lab Manual # 08**

**Combinational Circuits using System Verilog**

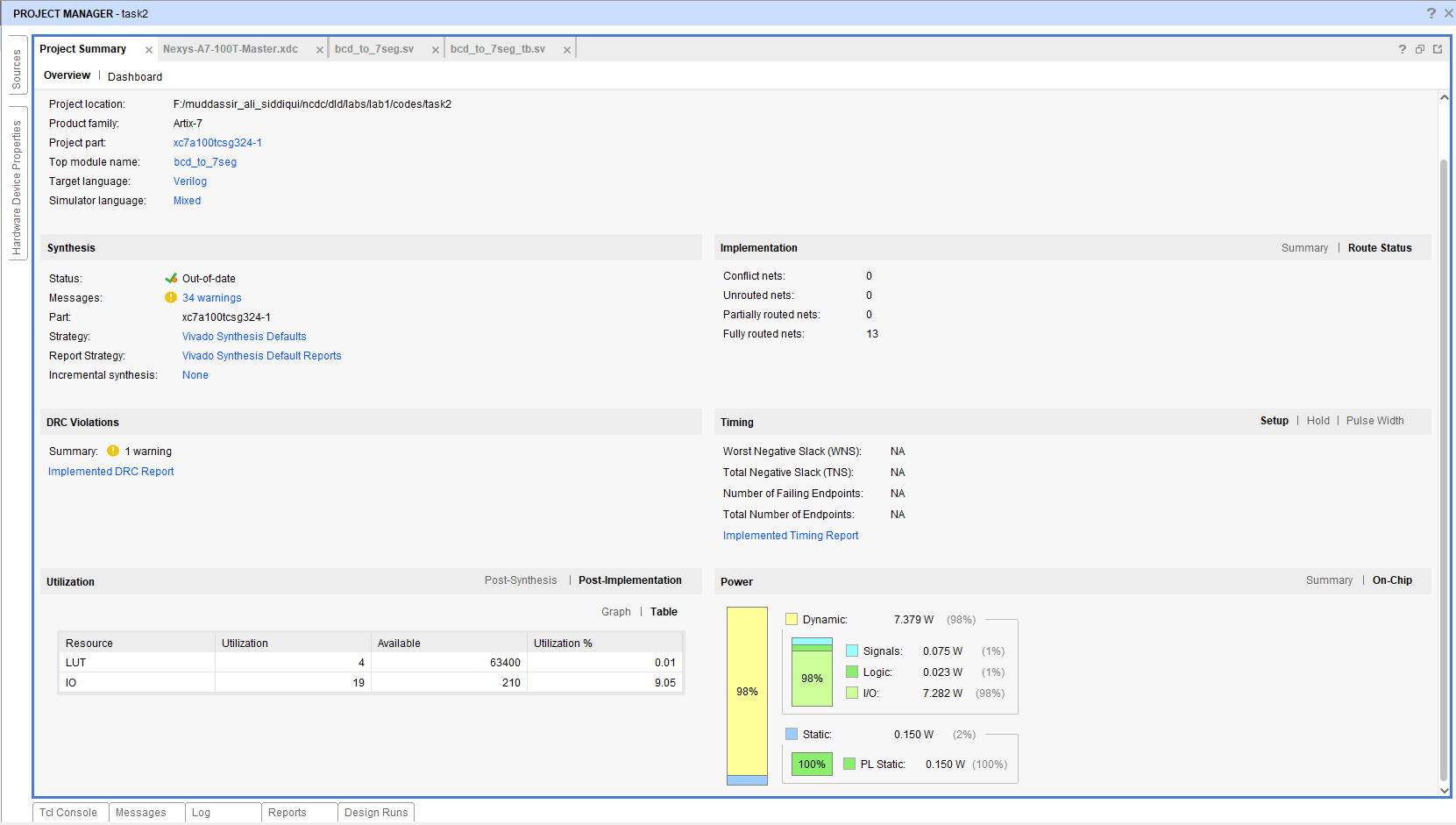
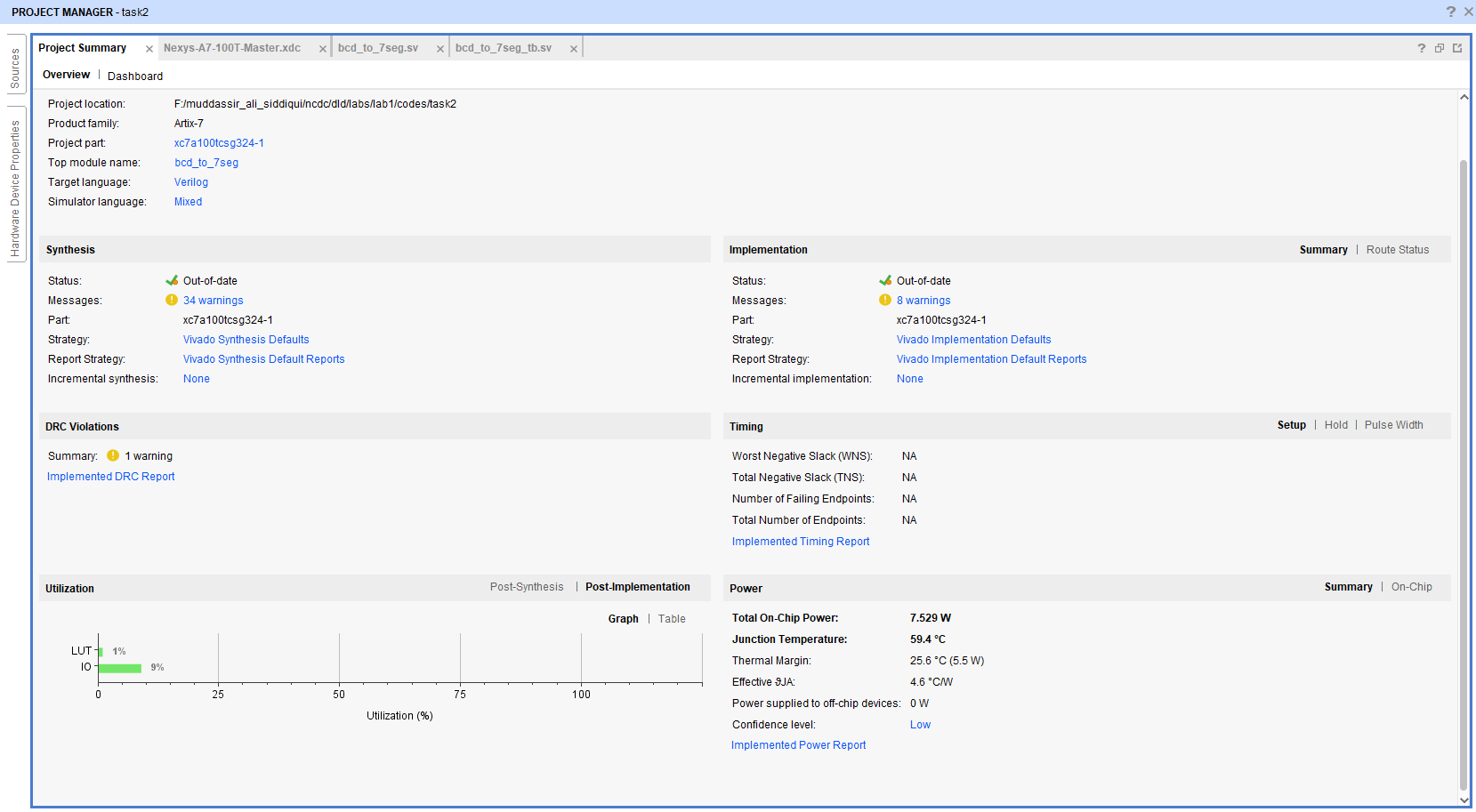
|  |  |
| --- | --- |
| **Name** | *Muddassir Ali Siddiqui* |
| **Instructor** | *Sir Musaddiq Hussain & Sir Bilal* |
| **Date** | *30th July 2025* |

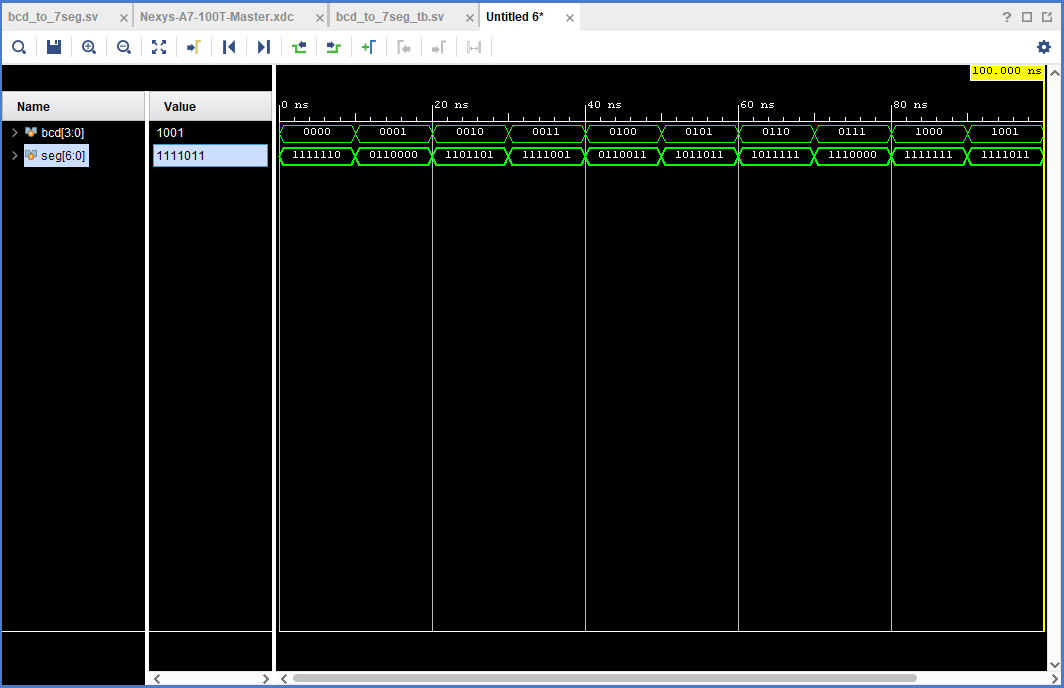
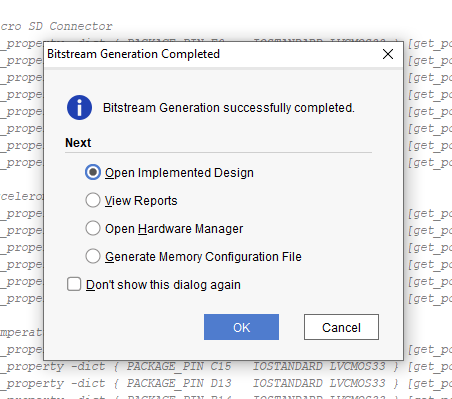
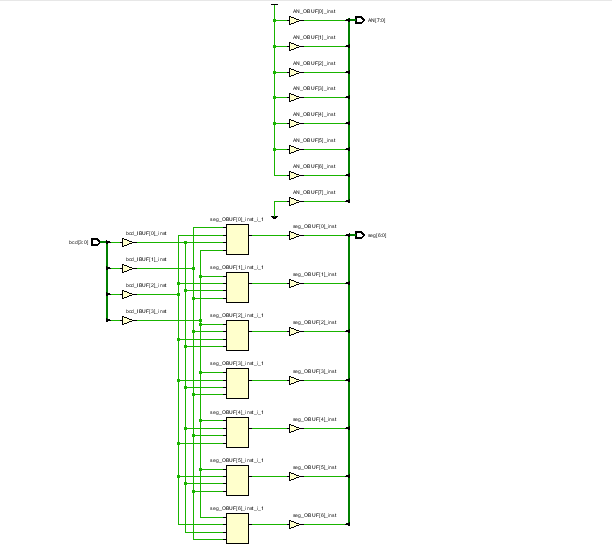
# In-Lab Tasks: (Write your lab task & screenshots here)

## Task 1:

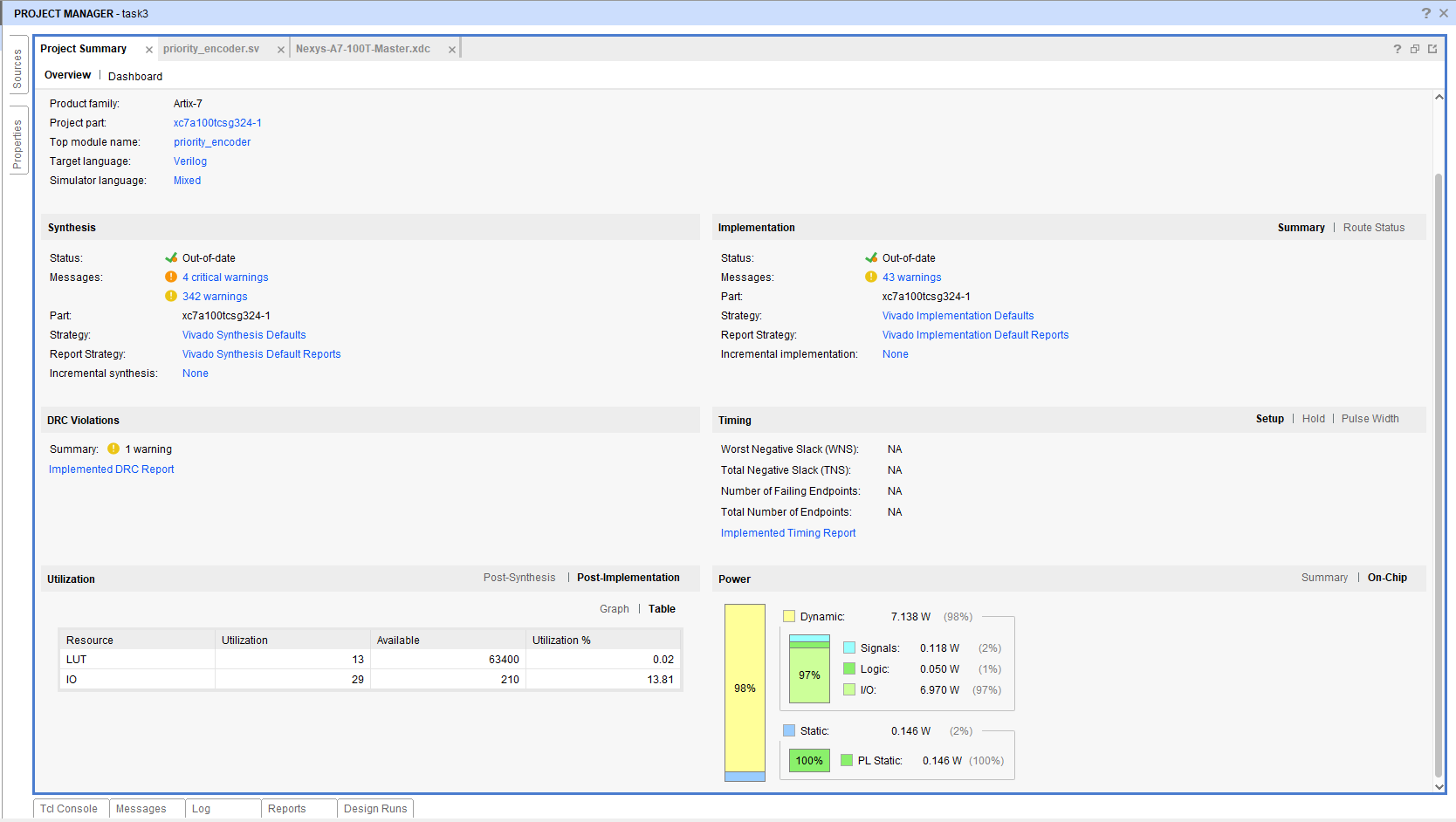
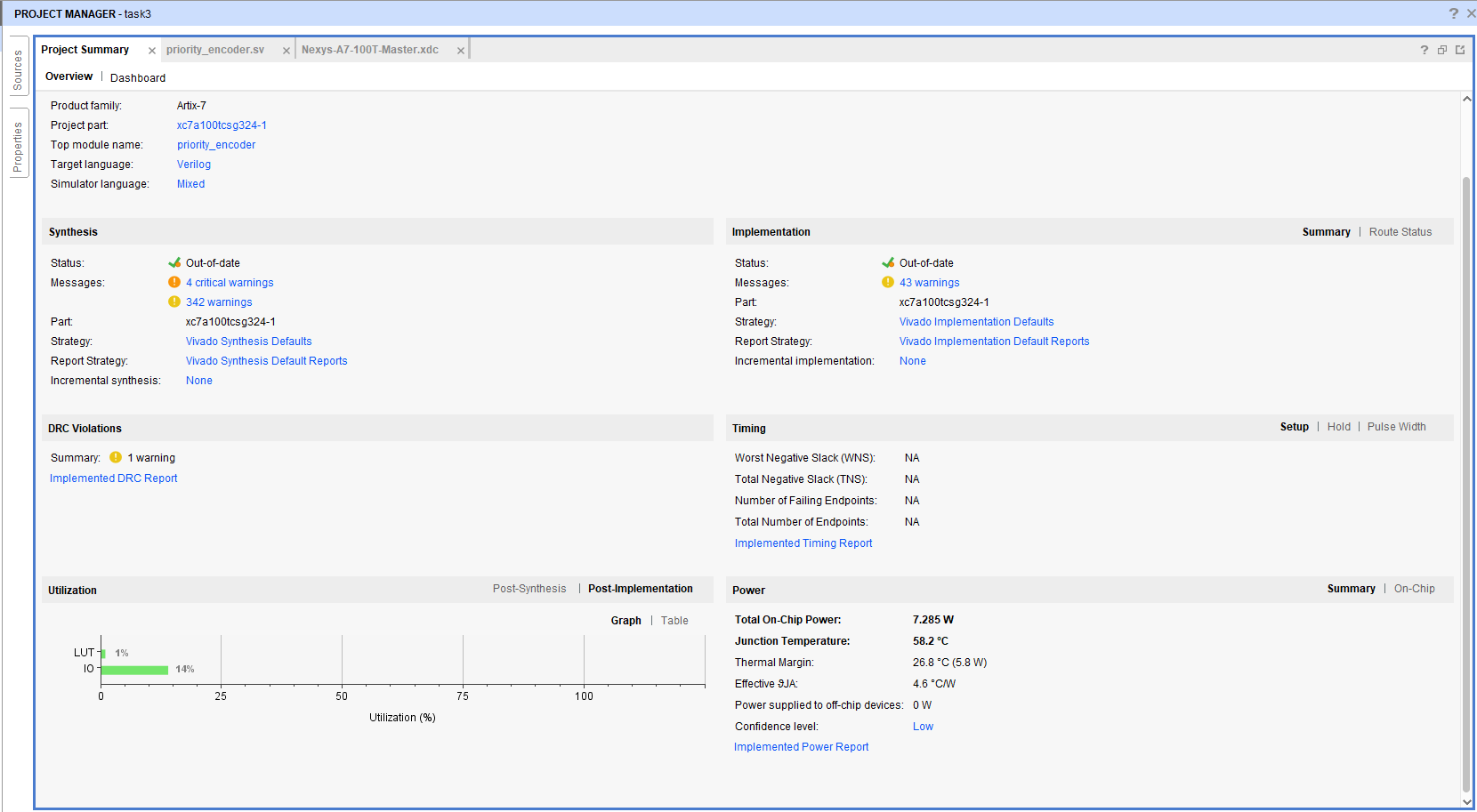


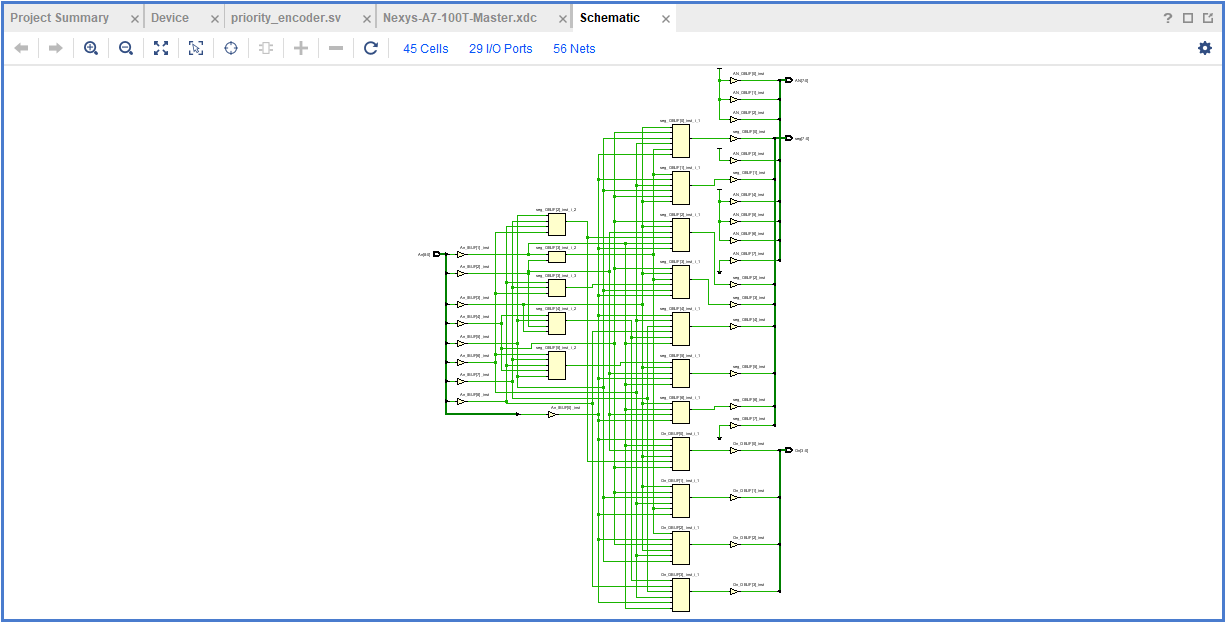
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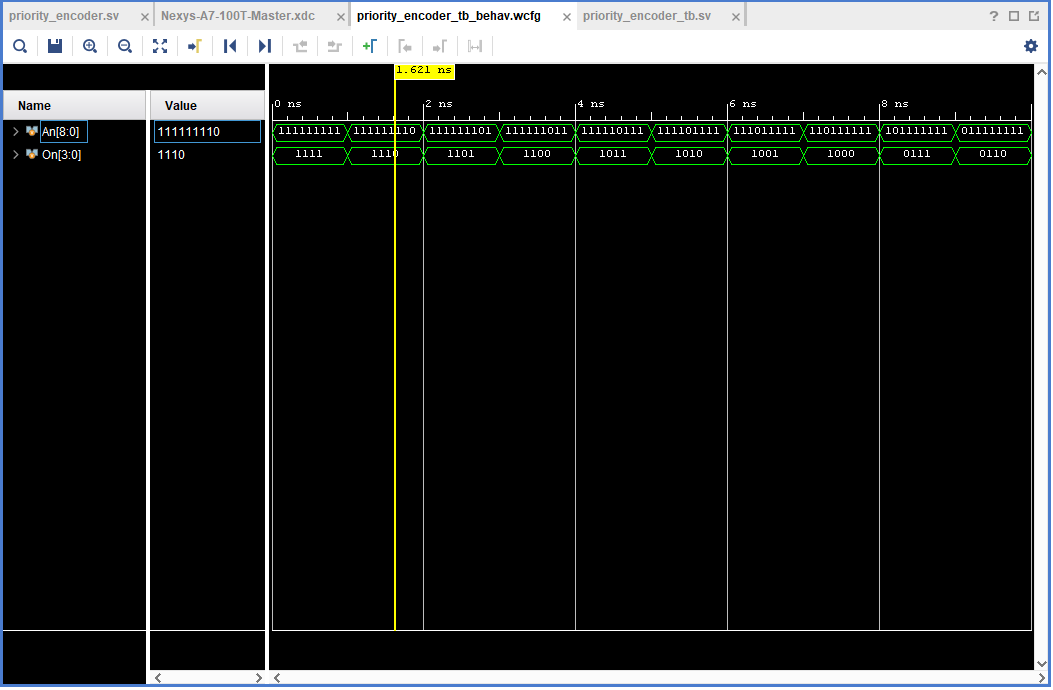
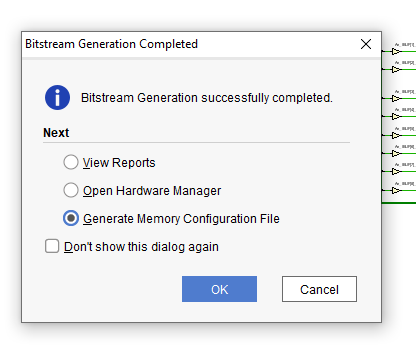




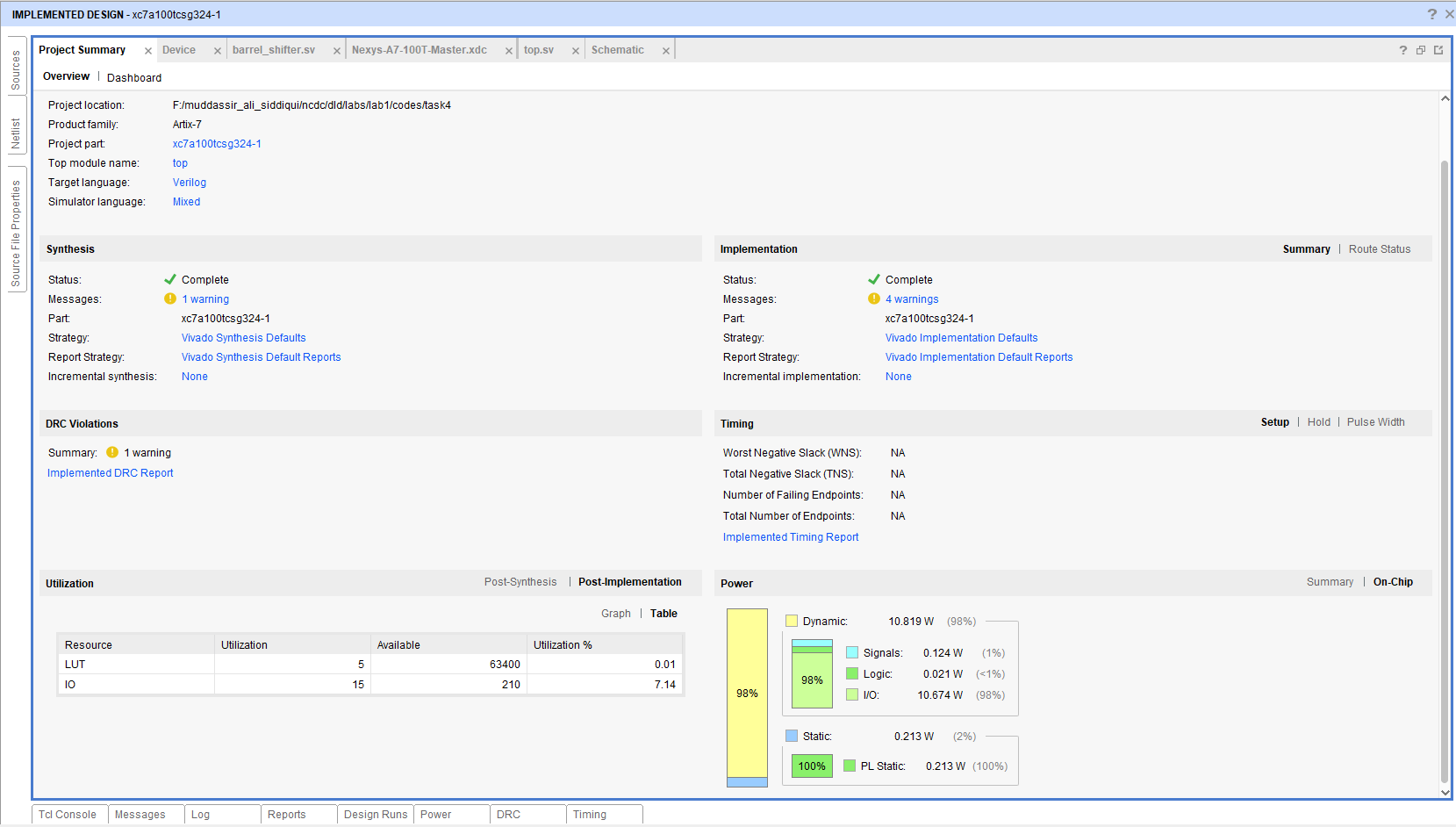
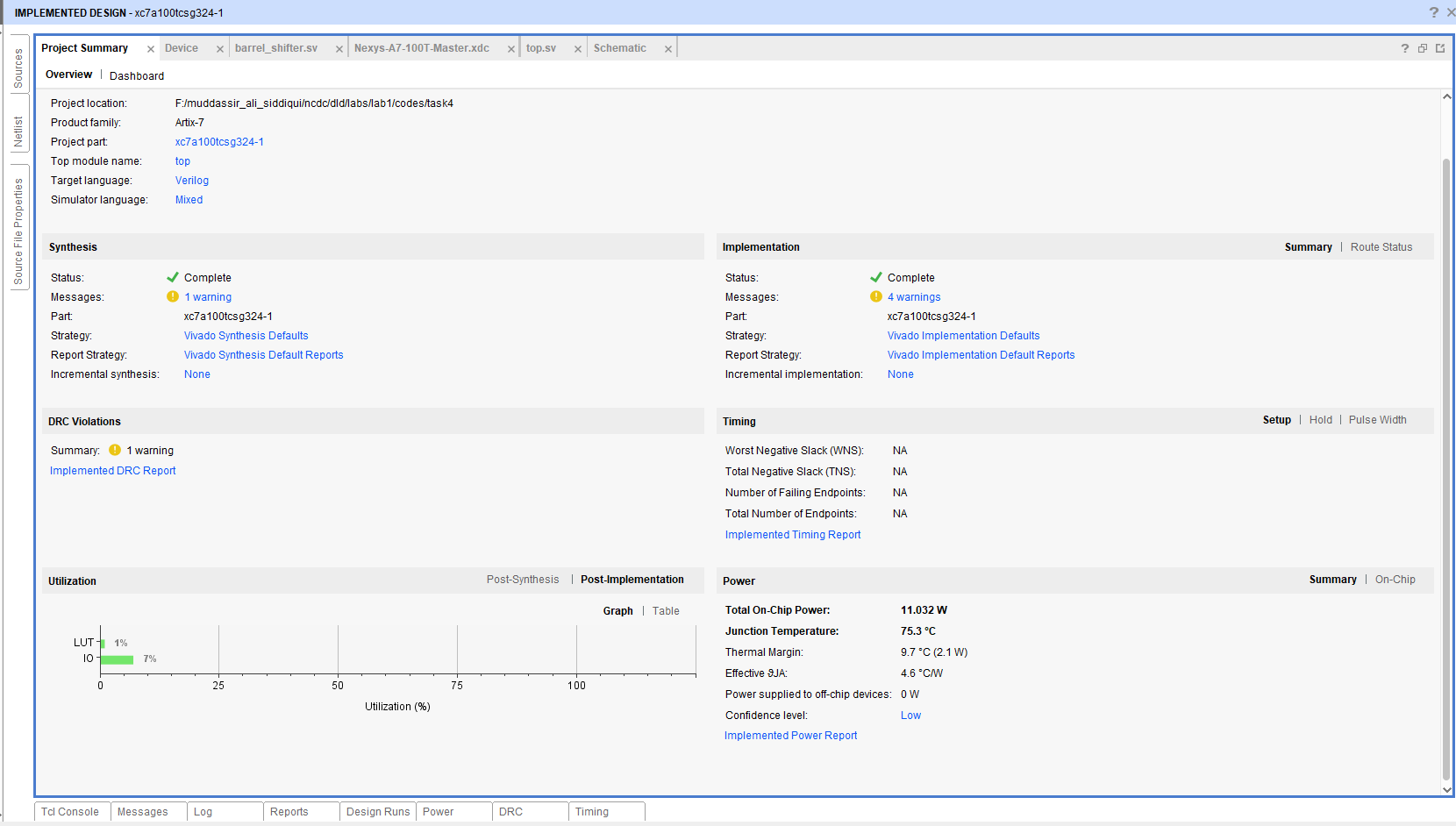
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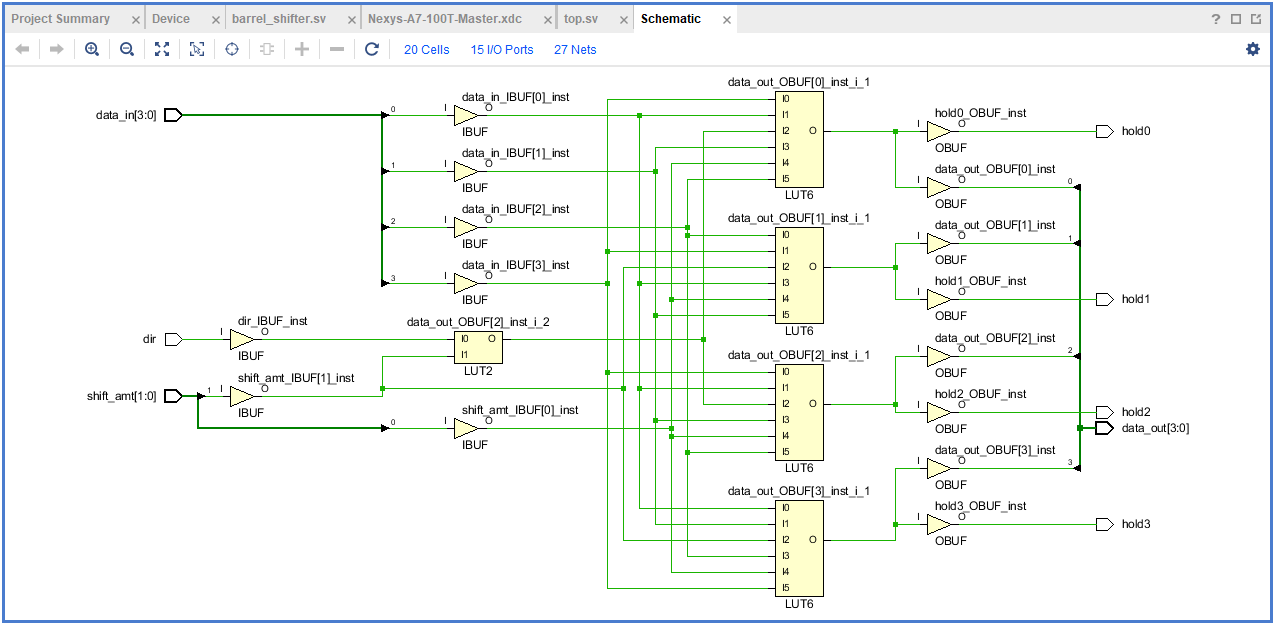




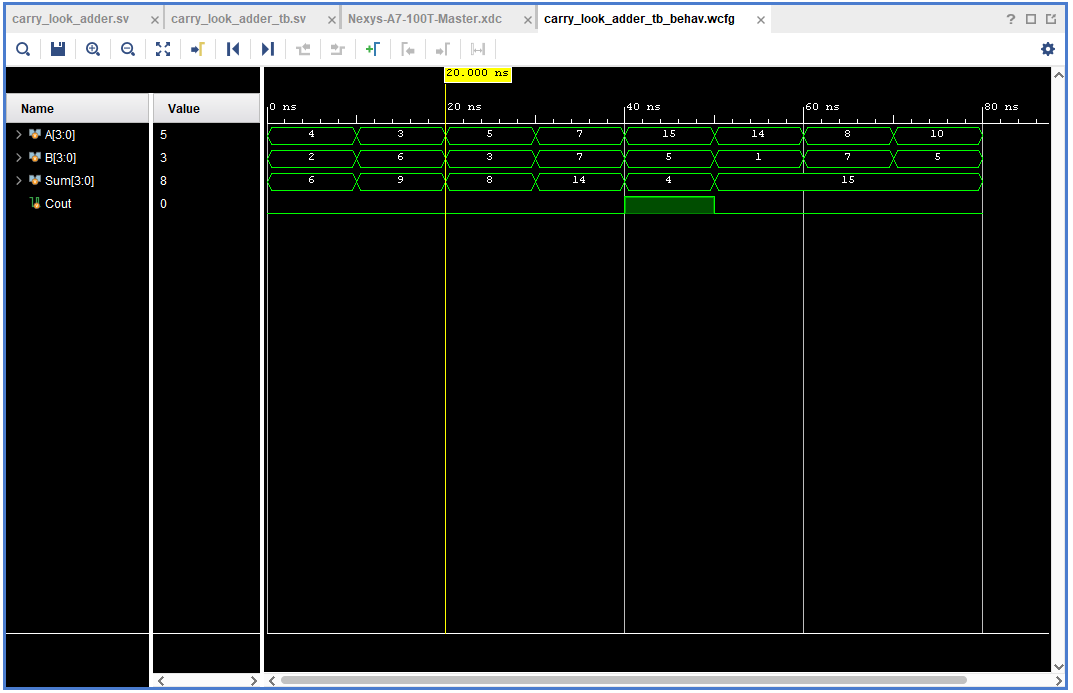
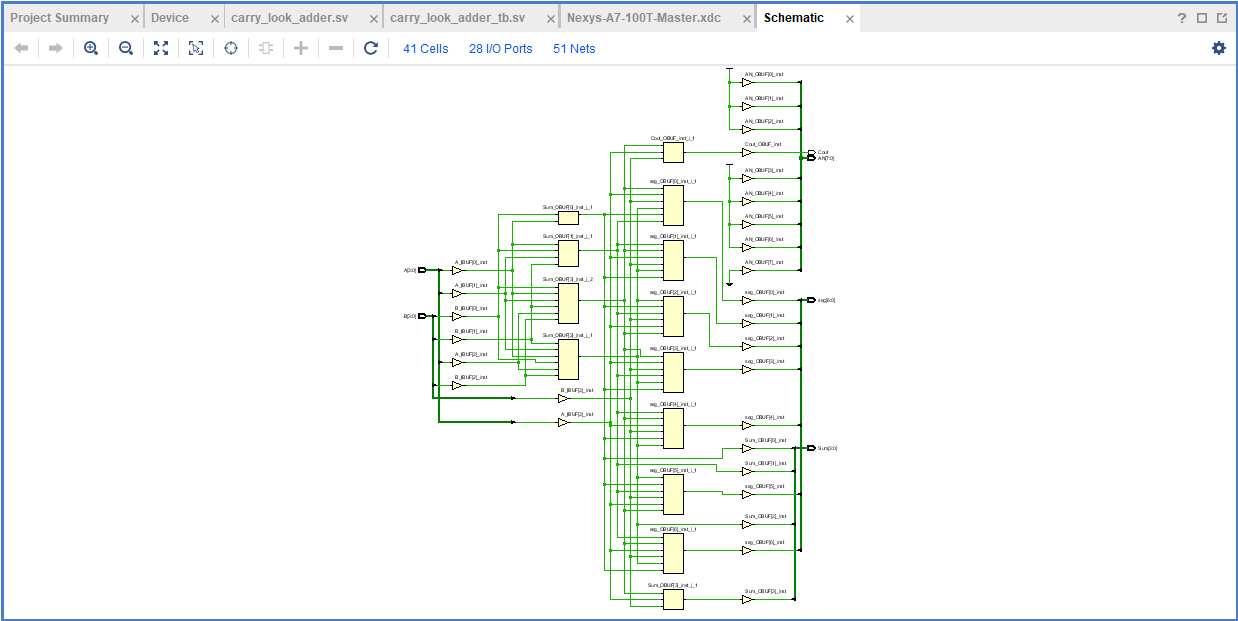
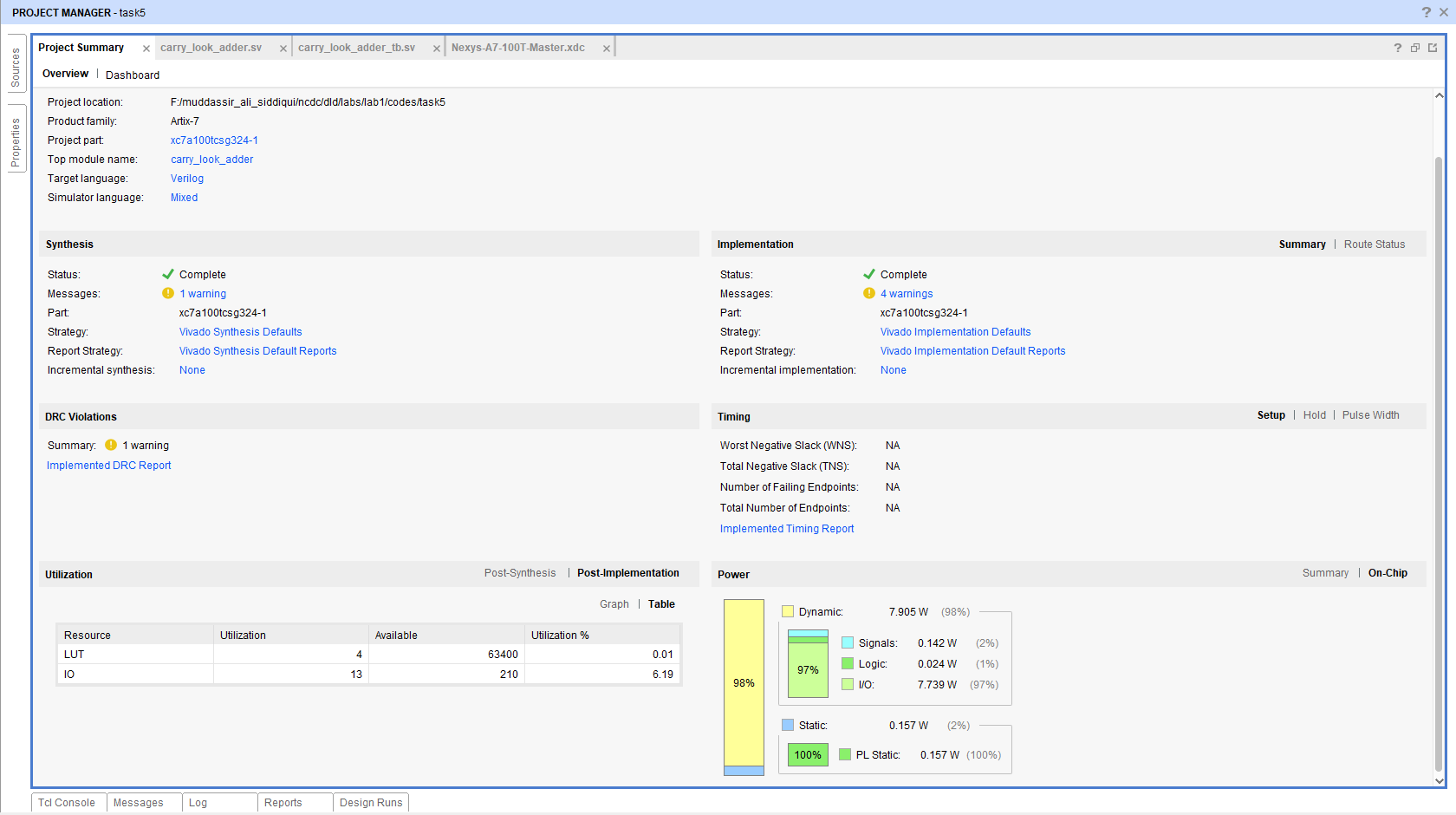
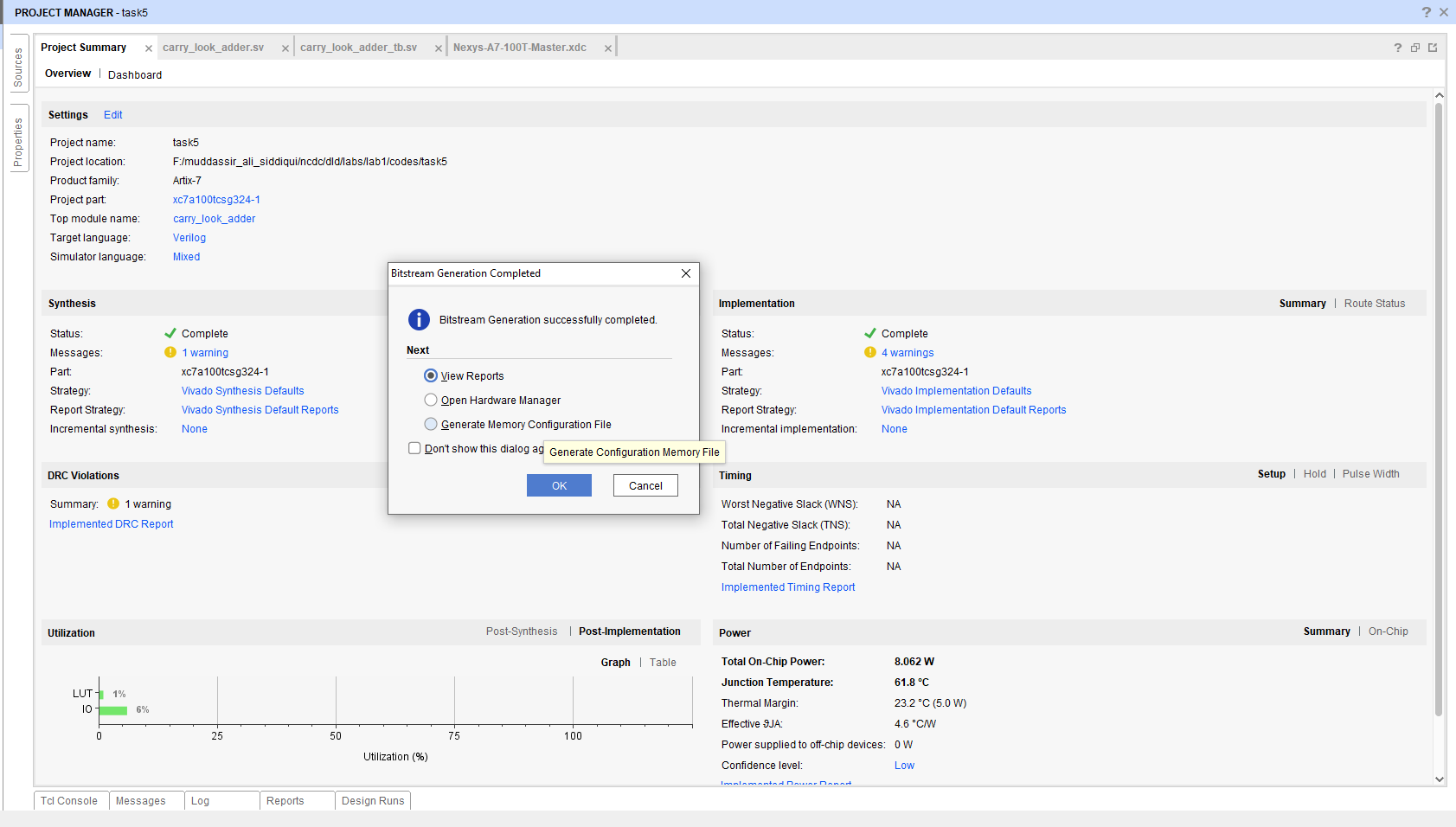


## Task 4:



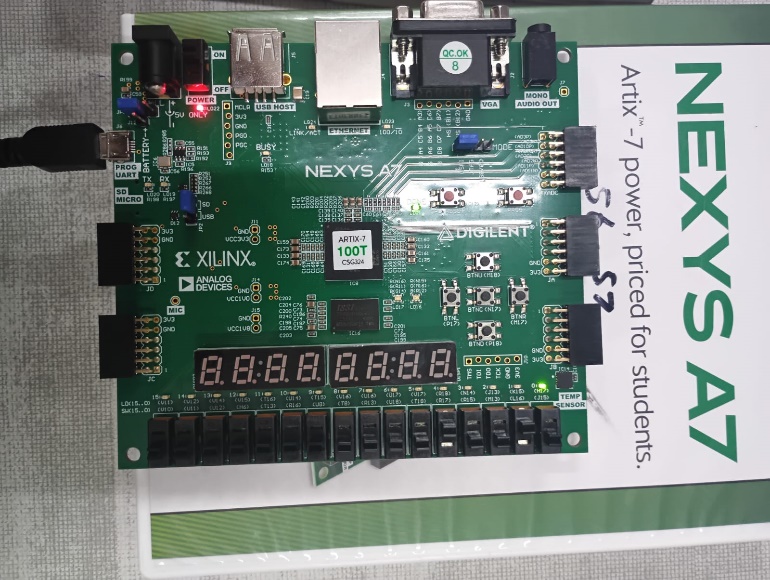
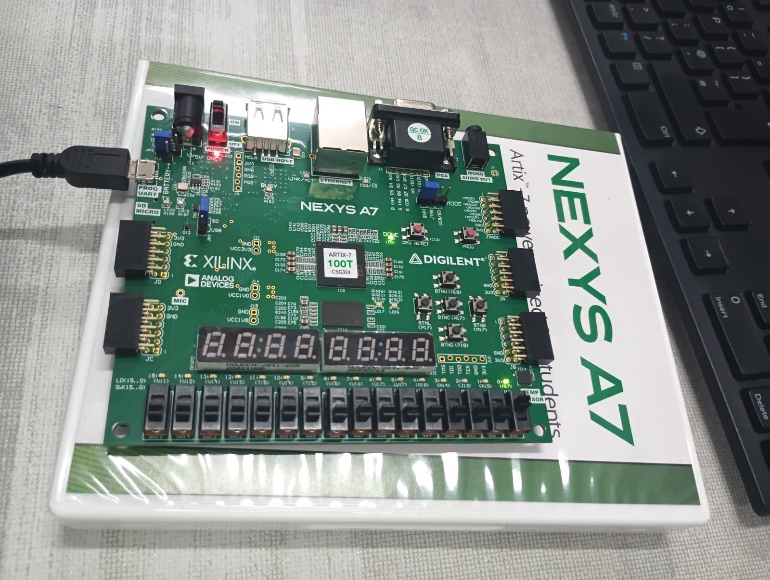


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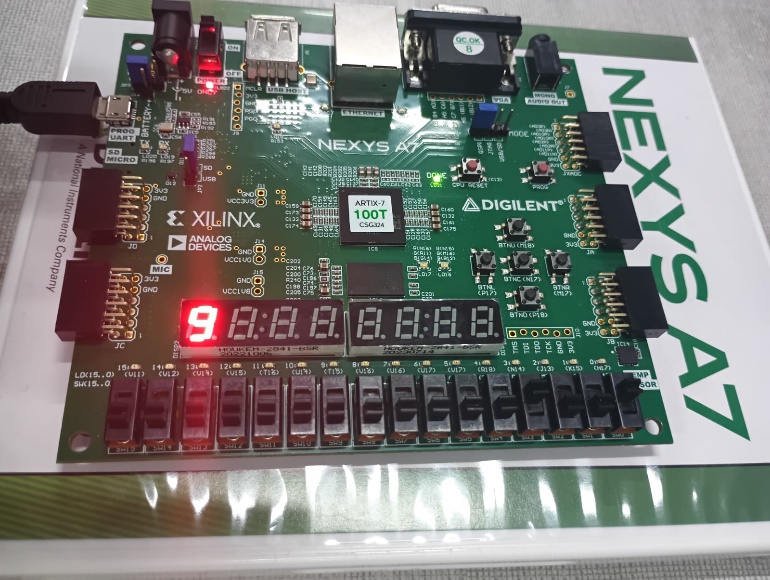


# FPGA Outputs:

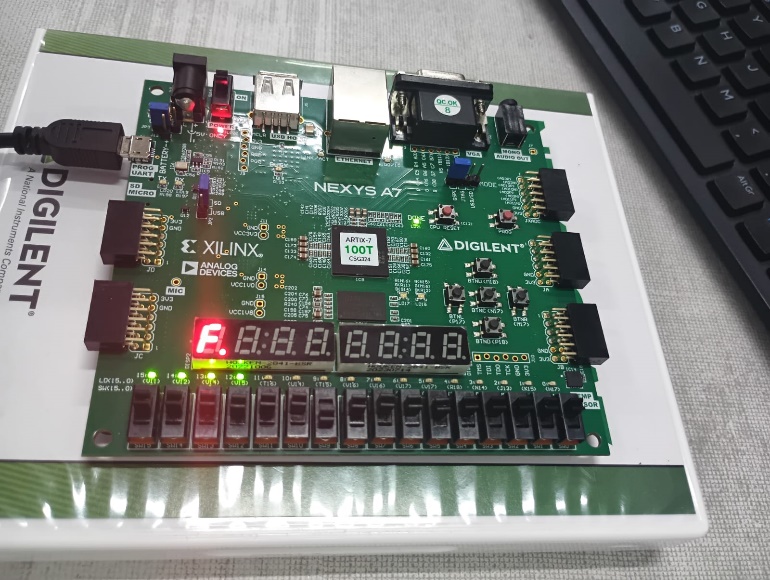
## Task 1:



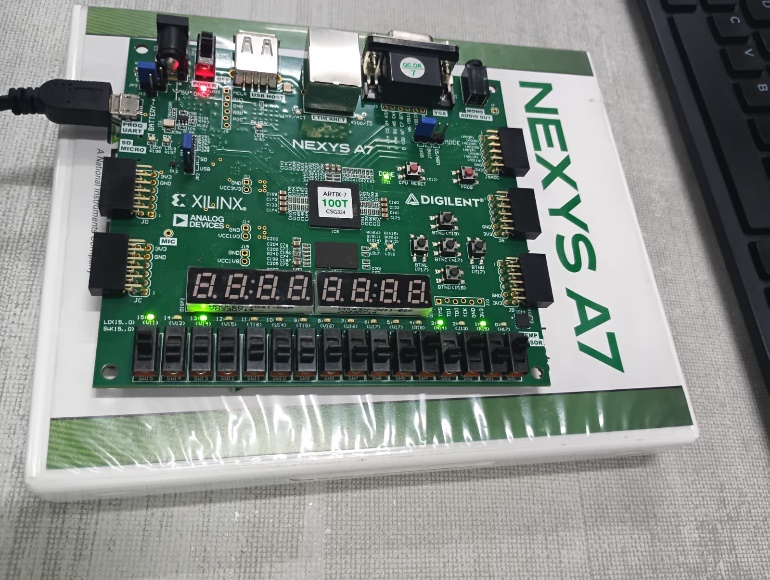
## Task 2:



## Task 3:



## Task 4:



# Critical Analysis: (Write you critical analysis / conclusion here)

In this lab we design in task 1 mux with 3 different approaches by gate level, case statement and behavioral. In task 2 we convert BCD to seven segment and show output on the FPGA’s 7-segment display. In task 3 we perform priority encoder by analyzing the truth table. In task 4 we do barrel shifter left and right by giving the direction to shift. In task 5 carry lookahead adder is performed by me.