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Design Verification Part

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Experiment NO.11:
SystemVerilog for Verification
Overview of 2-Port Memory Design for Project Implementation

10.1. Objectives

- Develop a test plan to verify the DUT's functionality.
- Create a verification environment to simulate the DUT.
- Identify and report any bugs or issues in the DUT.
- Ensure the DUT meets its specifications through testing.

10.2. Equipment Required

- Synopses Tool - VCS (Verilog Compiler Simulator)
- EDA Playground (alternative).

10.3. 2-Port Memory Design

Module Name: `dual_port_memory`

The `dual_port_memory` module implements a dual-port memory system that supports independent read and write operations on two separate ports (`port 0` and `port 1`). It uses a `mem_port` submodule to introduce latency for read and write acknowledgments. The design is parameterized and supports two response times (12 cycles for `port 0` and 34 cycles for `port 1`).

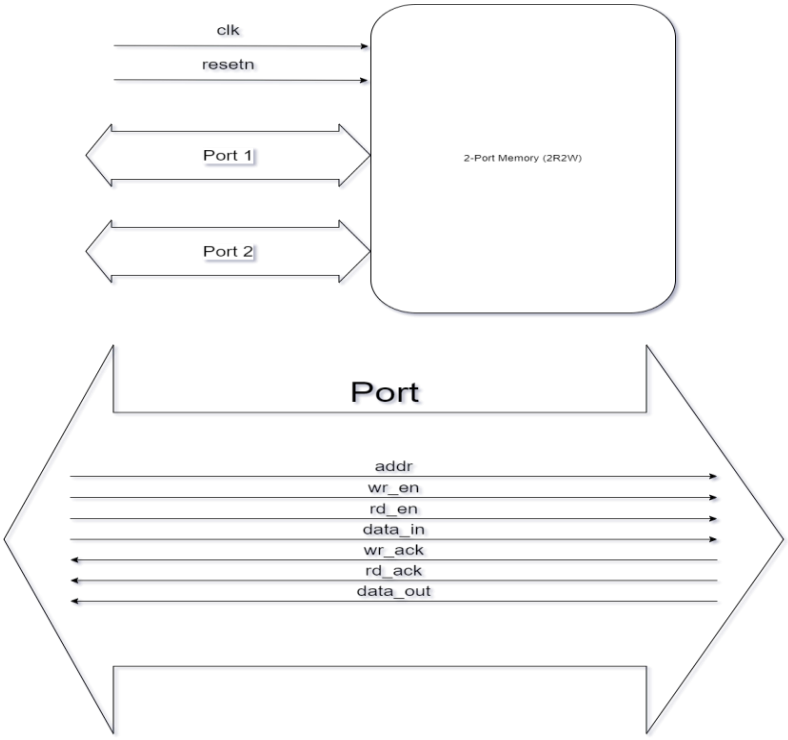

Figure 1: DUT

Inputs & Outputs:

Signal Name	**Direction**	**Width**	**Description**
clk	Input	1-bit	Clock signal for synchronization.
resetn	Input	1-bit	Active-low asynchronous reset.
wr_en0	Input	1-bit	Write enable for Port 0.
wr_en1	Input	1-bit	Write enable for Port 1.
rd_en0	Input	1-bit	Read enable for Port 0.
rd_en1	Input	1-bit	Read enable for Port 1.
wr_ack0	Output	1-bit	Write acknowledgment for Port 0.
wr_ack1	Output	1-bit	Write acknowledgment for Port 1.
rd_ack0	Output	1-bit	Read acknowledgment for Port 0.
rd_ack1	Output	1-bit	Read acknowledgment for Port 1.
addr0	Input	`addr_width` bits	Memory address for Port 0.
addr1	Input	`addr_width` bits	Memory address for Port 1.
data_in0	Input	`data_width` bits	Input data for write operation on Port 0.
data_in1	Input	`data_width` bits	Input data for write operation on Port 1.
data_out0	Output	`data_width` bits	Output data for read operation on Port 0.
data_out1	Output	`data_width` bits	Output data for read operation on Port 1.

Functional Description

1. Memory Model

- The memory model is a register array of size 2^6 (64 locations) with each location storing an 8-bit word.
- Two independent ports (`port 0` and `port 1`) allow simultaneous read and write operations to separate memory addresses.

2. Read and Write Control

- **Write Operation**:
  - Controlled by `wr_en0` and `wr_en1`.
  - Data is written to the memory at `addr0` and `addr1` for `port 0` and `port 1`, respectively.
  - Acknowledgment of the write (`wr_ack`) is delayed by the respective port's response time.
- **Read Operation**:
  - Controlled by `rd_en0` and `rd_en1`.
  - Data is read from memory at `addr0` and `addr1` for `port 0` and `port 1`, respectively.
  - Acknowledgment of the read (`rd_ack`) is delayed by the respective port's response time.

3. Latency Mechanism

- A `mem_port` submodule is instantiated for each port:
  - **Port 0**: Response time is parameterized to 12 cycles.
  - **Port 1**: Response time is parameterized to 34 cycles.
- The submodule manages state transitions, enabling precise acknowledgment of read/write operations after the defined latency.

4. Tasks

- **Write Task (`write_data`)**:
  - Writes `data_in0` to `addr0` or `data_in1` to `addr1` based on the port number.
- **Read Task (`read_data`)**:
  - Reads data from `addr0` or `addr1` into `data_out0` or `data_out1` based on the port number.

5. Reset Behavior

- On `resetn` assertion:
  - All signals and outputs are reset to their initial values.
  - Memory contents are cleared (all locations set to 0).

10.4. Verification Plan & Test Plan

A **Verification Plan (V-Plan)** is a detailed document used in the design verification process to ensure a digital design (DUT) function correctly according to its specifications. It outlines the overall strategy, including what needs to be tested, how it will be tested, and the tools or methodologies that will be used. The plan includes key elements like the design's features, a list of test scenarios (both functional and edge cases), the structure of the testbench (drivers, monitors, checkers), and specific goals such as achieving complete functional and code coverage. It also defines pass/fail criteria to measure success. The purpose of a V-Plan is to provide a clear roadmap for systematically verifying the DUT, ensuring all requirements are met before moving to production.

A **Test Plan** is a detailed document that outlines the specific test cases, scenarios, and conditions required to verify the Design Under Test (DUT). It serves as a guide for systematically testing the DUT to ensure it behaves as expected under various conditions. The Test Plan defines the objectives of the tests, lists the individual test cases, specifies the input stimuli and expected outputs, and identifies the pass/fail criteria for each test. By focusing on what needs to be tested and how it will be executed, a Test Plan ensures that all critical aspects of the DUT are thoroughly validated in an organized manner.

10.5. Procedure

Your role is to write a test plan to verify the system's functionality and build the verification environment to identify and report any bugs.