



Department of Electrical and Computer Engineering

Hardware Design Laboratory ENCS5131

Project 2

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Section No. 2

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Errors and Fixes

1. Incorrect counter initialization

- **Location:** `mem_port` module, `IDLE_STATE`
- **Original Code:** `counter <= response_time - 2;`
- **Fixed Code:** `counter <= response_time - 1;`
- **Description:** The counter should be initialized to `response_time - 1` to align with the logic in the rest of the module.

2. Wrong drive of write enable for port 1

- **Location:** `dual_port_memory` module, always block
- **Original Code:** `if(wr_en0 wr_ack0 wr_ack0) wr_en1 <= 1;`
- **Fixed Code:** `if (wr_en1 !wr_ack1) wr_en1 <= 1; else if (wr_ack1) wr_en1 <= 0;`
- **Description:** The write enable (`wr_en1`) should be driven based on the `wr_en1` signal, not `wr_en0`.

3. Wrong drive of read enable for port 1

- **Location:** `dual_port_memory` module, always block
- **Original Code:** `if(rd_en0 rd_ack0 rd_ack0) rd_en0 <= 1; else if(rd_ack0) rd_en1 <= 0;`
- **Fixed Code:** `if (rd_en1 !rd_ack1) rd_en1 <= 1; else if (rd_ack1) rd_en1 <= 0;`
- **Description:** The read enable (`rd_en1`) should be driven based on the `rd_en1` signal, not `rd_en0`.

4. Incorrect use of write enable for port 0

- **Location:** `dual_port_memory` module, always block
- **Original Code:** `if(wr_en0 wr_ack0 wr_ack0) wr_en1 <= 1;`
- **Fixed Code:** `if (wr_en0 !wr_ack0) wr_en0 <= 1; else if (wr_ack0) wr_en0 <= 0;`
- **Description:** The logic for driving `wr_en0` should be applied to port 0, not port 1.

5. Incorrect use of read enable for port 0

- **Location:** `dual_port_memory` module, always block
- **Original Code:** `if(rd_en0 rd_ack0 rd_ack0) rd_en0 <= 1; else if(rd_ack0) rd_en1 <= 0;`
- **Fixed Code:** `if (rd_en0 !rd_ack0) rd_en0 <= 1; else if (rd_ack0) rd_en0 <= 0;`
- **Description:** The logic for driving `rd_en0` should apply to port 0, not port 1.

6. Incorrect initialization of `wr_ack` and `rd_ack`

- **Location:** `dual_port_memory` module, always block
- **Original Code:**

```
– wr_ack0 <= 1;  
– wr_ack1 <= 1;  
– rd_ack0 <= 1;  
– rd_ack1 <= 1;
```
- **Fixed Code:**

```
– wr_ack0 <= 0;  
– wr_ack1 <= 0;  
– rd_ack0 <= 0;  
– rd_ack1 <= 0;
```
- **Description:** These should be initialized to 0 for proper operation, not 1.

7. Incorrect use of `write_data` for both ports

- **Location:** `dual_port_memory` module, always block
`write_data(1);`
- **Description:** The `write_data` task should be called for the correct port (0 for port 0, 1 for port 1).

8. Incorrect read logic for `data_out1`

- **Location:** `dual_port_memory` module, `read_data` task
- **Original Code:** `data_out1 <= mem[addr0];`
- **Fixed Code:** `data_out1 <= mem[addr1];`
- **Description:** The correct address should be used for port 1, not port 0.

1 Tests Results

You can access the code and simulation on EDA Playground using the following link: <https://edaplayground.com/x/k2Ct>

```
compiling more sources
All of 6 modules done
rm -f _quarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++ -O3 ../simv -dynamic -Wl,-rpath=$ORIGIN/`simv.daidir` -Wl,-rpath=../simv.daidir -Wl,-rpath=/apps/vcsmx/vcs/U-2023.03-SP2/linux64/lib -L/apps/vcsmx/vcs/U-
../simv up to date
CPU time: .689 seconds to compile + .694 seconds to elab + .358 seconds to link
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full164; Runtime version U-2023.03-SP2_Full164; Jan 10 14:19 2025
[Directed Test] Starting...
[Generator:] Port = 1, Addr = 14, Data = c8, Write = 1
[Generator:] Port = 0, Addr = a, Data = 64, Write = 1
[Generator:] Port = 0, Addr = a, Write = 0
[Generator:] Port = 1, Addr = 14, Write = 0
[Monitor] Port 0: Addr = a, Read Data = 64, Expected Data = 64
[Scoreboard] Match: Addr = a, Expected = 64, Got = 64
[Monitor] Port 1: Addr = 14, Read Data = c8, Expected Data = c8
[Scoreboard] Match: Addr = 14, Expected = c8, Got = c8
$finish called from file "testbench.sv", line 54.
$finish at simulation time 100000
V C S S i m u l a t i o n R e p o r t
Time: 100000 ns
CPU Time: 0.500 seconds; Data structure size: 0.0Mb
Fri Jan 10 14:19:59 2025
Done
```

Figure 1: test Writing and reading