
# Department of Electrical and Computer Engineering

## Hardware Design Laboratory ENCS5131

## Project 2

**Prepared by:**
- **Ali Al-Saed 1210198**
- **Osama Hamdan 1212107**

**Section No. 2**

**Instructor : Dr.Abdellatif Abu-Issa**
**TA : Rania Shahwan**

**Date January 10, 2025**

## Errors and Fixes

1. **Incorrect counter initialization**
   - **Location**: `mem_port` module, `IDLE_STATE`
   - **Original Code**: `counter <= response_time - 2;`
   - **Fixed Code**: `counter <= response_time - 1;`
   - **Description**: The counter should be initialized to `response_time - 1` to align with the logic in the rest of the module.

2. **Wrong drive of write enable for port 1**
   - **Location**: `dual_port_memory` module, always block
   - **Original Code**: `if(wr_en0  wr_ack_0  wr_ack0) wr_en_1 <= 1;`
   - **Fixed Code**: `if (wr_en1  !wr_ack_1) wr_en_1 <= 1; else if (wr_ack_1) wr_en_1 <= 0;`
   - **Description**: The write enable (`wr_en_1`) should be driven based on the `wr_en1` signal, not `wr_en0`.

3. **Wrong drive of read enable for port 1**
   - **Location**: `dual_port_memory` module, always block
   - **Original Code**: `if(rd_en0  rd_ack_0  rd_ack0) rd_en_0 <= 1; else if(rd_ack_0) rd_en_1 <= 0;`
   - **Fixed Code**: `if (rd_en1  !rd_ack_1) rd_en_1 <= 1; else if (rd_ack_1) rd_en_1 <= 0;`
   - **Description**: The read enable (`rd_en_1`) should be driven based on the `rd_en1` signal, not `rd_en0`.

4. **Incorrect use of write enable for port 0**
   - **Location**: `dual_port_memory` module, always block
   - **Original Code**: `if(wr_en0  wr_ack_0  wr_ack0) wr_en_1 <= 1;`
   - **Fixed Code**: `if (wr_en0  !wr_ack_0) wr_en_0 <= 1; else if (wr_ack_0) wr_en_0 <= 0;`
   - **Description**: The logic for driving `wr_en_0` should be applied to port 0, not port 1.

5. **Incorrect use of read enable for port 0**
   - **Location**: `dual_port_memory` module, always block
   - **Original Code**: `if(rd_en0  rd_ack_0  rd_ack0) rd_en_0 <= 1; else if(rd_ack_0) rd_en_1 <= 0;`
   - **Fixed Code**: `if (rd_en0  !rd_ack_0) rd_en_0 <= 1; else if (rd_ack_0) rd_en_0 <= 0;`
   - **Description**: The logic for driving `rd_en_0` should apply to port 0, not port 1.

6. **Incorrect initialization of `wr_ack` and `rd_ack`**
    - **Location**: `dual_port_memory` module, always block
    - **Original Code**:
        - `wr_ack0 <= 1;`
        - `wr_ack1 <= 1;`
        - `rd_ack0 <= 1;`
        - `rd_ack1 <= 1;`
    - **Fixed Code**:
        - `wr_ack0 <= 0;`
        - `wr_ack1 <= 0;`
        - `rd_ack0 <= 0;`
        - `rd_ack1 <= 0;`
    - **Description**: These should be initialized to `0` for proper operation, not `1`.
7. **Incorrect use of `write_data` for both ports**
    - **Location**: `dual_port_memory` module, always block
      `write_data(1);`
    - **Description**: The `write_data` task should be called for the correct port (`0` for port 0, `1` for port 1).
8. **Incorrect read logic for `data_out1`**
    - **Location**: `dual_port_memory` module, `read_data` task
    - **Original Code**: `data_out1 <= mem[addr0];`
    - **Fixed Code**: `data_out1 <= mem[addr1];`
    - **Description**: The correct address should be used for port 1, not port 0.

# 1 Tests Results

You can access the code and simulation on EDA Playground using the following link: `https://edaplayground.com/x/k2Ct`

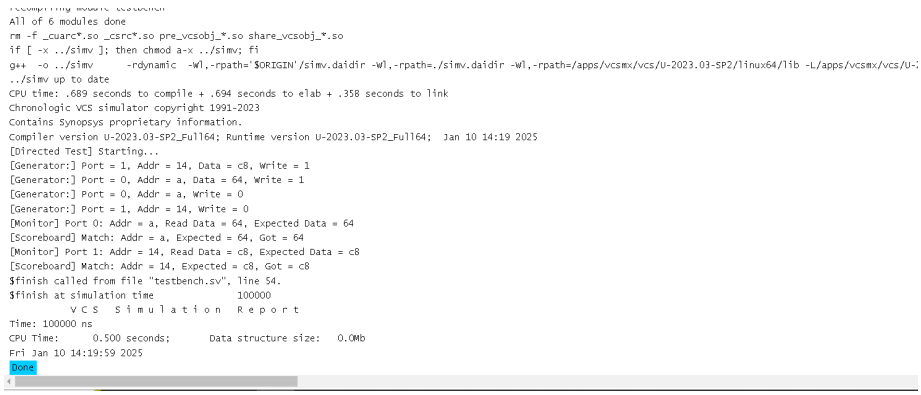


Figure 1: test Writing and reading