بسم الله

علی ایمانقلی 810197692

پروژه 1 طراحی سیستم های نهفته میتنی بر FPGA

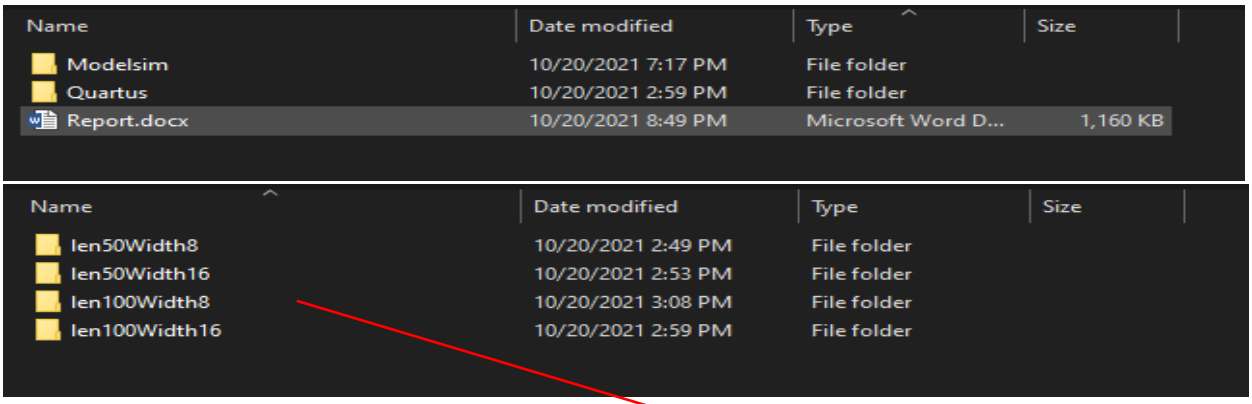
بخش اول: مقدمه و خلاصه

بخش دوم: تصویر مسیر داده و واحد کنترل و توضیحات پیرامون آن

بخش سوم: بررسی روند کلی کد های Verilog و تصاویر نتایج خروجی

بخش چهرم: بررسی روند کلی سنتز در ابزار Quartus و تصاویر خروجی ها و مقایسه بین خروجی های بدست امد.

ساختارفایل ها:



قسمت Quartus به تفکیک

بخش اول:

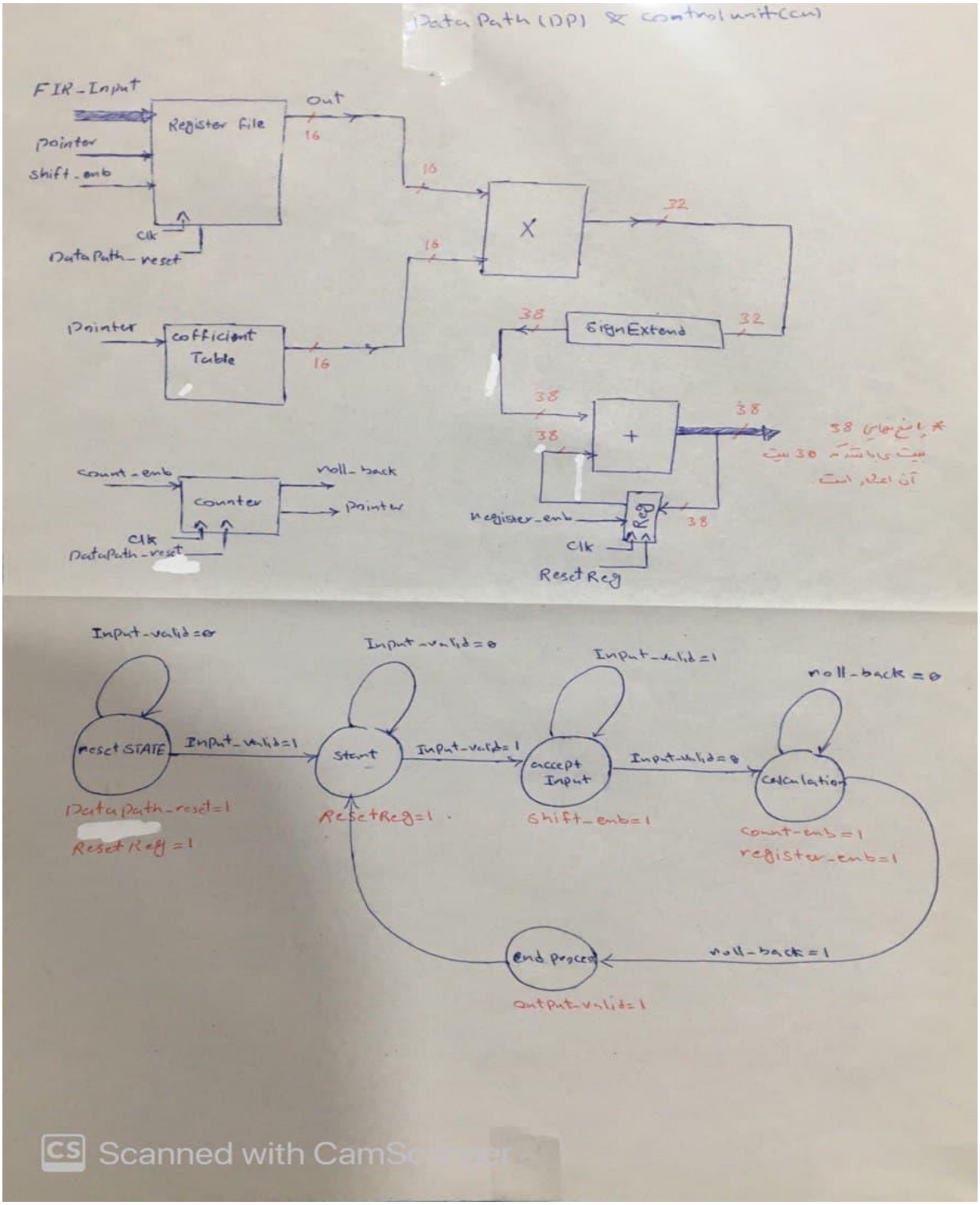
در این پروژه هدف انجام یک فیلتر خطی FIR بوده تا صوت بدست امده از نرم افزار متلب را فیلتر کند.

این پروژه با زبان توصیف سخت افزار Verilog نوشته شده است و به صورت پارامتری فیلتر خطی FIR را پیاده سازی میکند.

نکته ی حائز اهمیت ساختار serial فیلتر طراحی شده می باشد که در بخش دوم، مسیر داده و واحد کنترل آن را می توان مشاهده کرد.

*** کد به نحوی نوشته شده است که نام متغیر ها گویا ی کاربرد ان ها باشد و در برخی موارد کامنت گذاری نیز شده است. ***

بخش دوم:

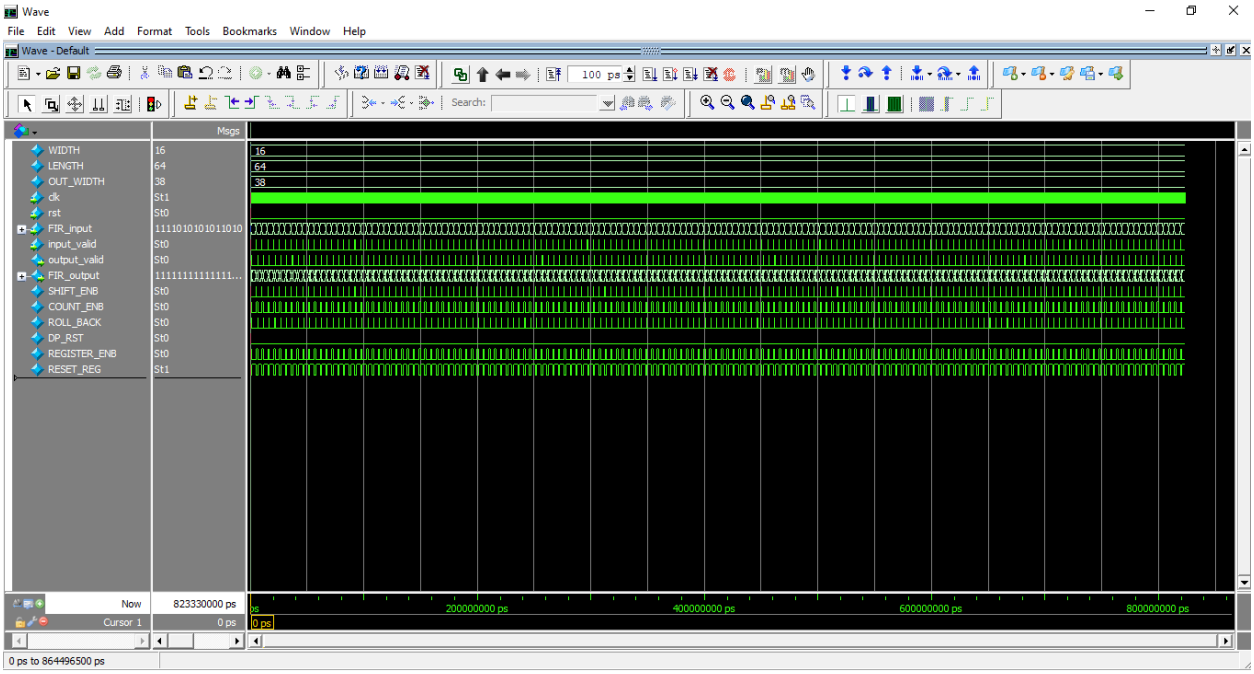


بخش سوم:

این بخش از دو قسمت مسیر داده و واحد کنترل تشکیل شده است.

در ابتدا سیستم با دریافت Input_Valid ورودی FIR_Input را دریافت کرده و پس از محاسبات خروجی را در FIR_Output قرار می دهد و سیگنال Output_Valid را فعال میکند.

نتایج Simulation :



در قسمت test bench کد نوشته شده است که خروجی ما را با خروجی معیار مقایسه می کند.

روند این کد به این صورت است که منتظر می ماند تا ما خروجی را در یک فایل به نام myOutputFile.txt بنویسیم (این مکانیزم توسط سیگنال startComapre_2_files مدیریت می شود.) و سپس شروع به مقایسه با فایل مرجع می کند.

*** فایل myOutputFile.txt خروجی برنامه می باشد که در پوشه ی Modelsim قرار دارد.

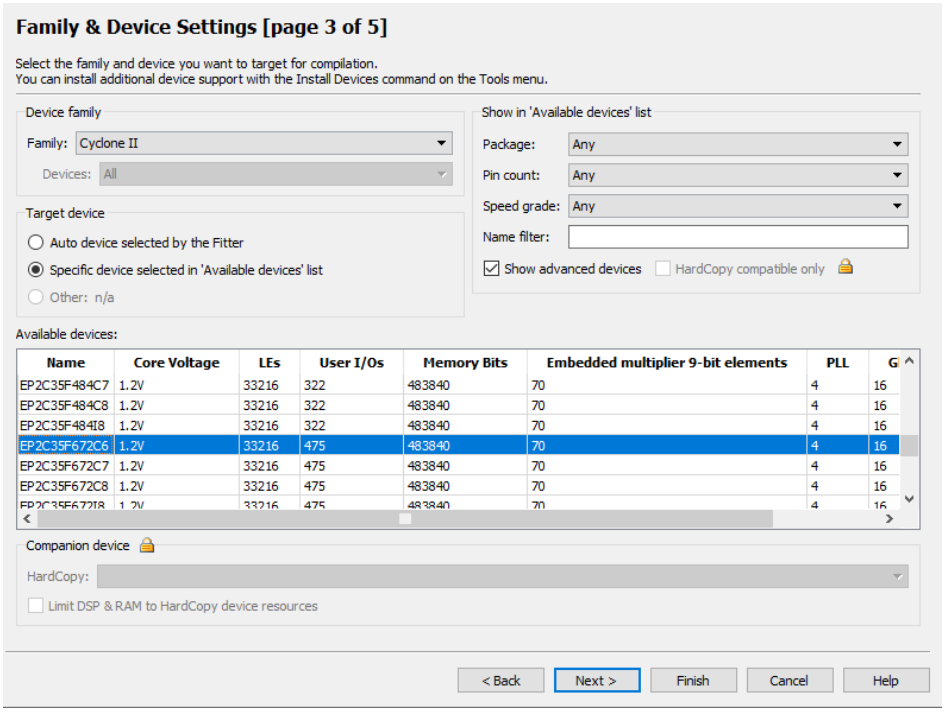
```
// compare the resault of my module with excepted outputs after that all outputs were written in the `myOutputFile.txt`.
always@(posedge startComapre_2_files)
begin
    $fclose(myOutputFile);
    #20
    $readmemb("myOutputFile.txt", myOutput);
    #20
    for(j=0; j < DATA_LEN; j=j+1)
    begin
        if(myOutput[j] != expected_data_from_text_file[j])
            $display("[-] Test failed for input:", j);
        else
            $display("[+] Test Passed for input:", j);
    end
    $display("***  test has finished.  ***");

$stop;

end

endmodule
```

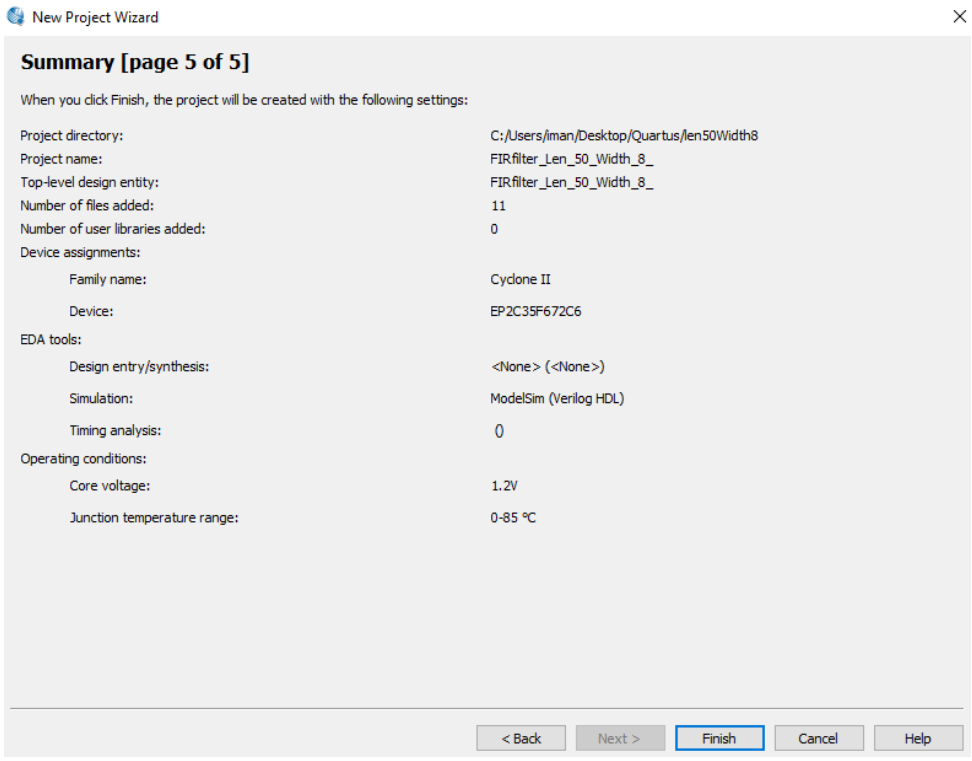
بخش چهارم:

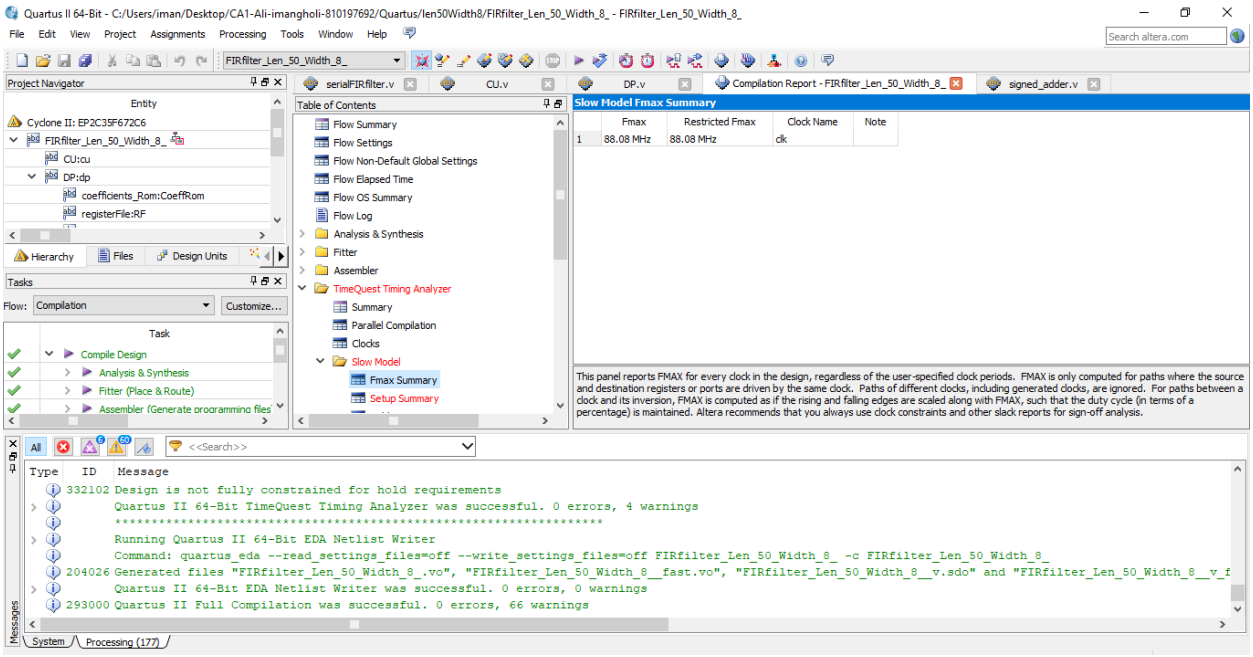
به تفکیک نتیاج برای 4 حالت خواسته شده در زیر آورده شده است:

*** برای تمامی حالت ها از خانواده ی cycloneII و مدلی که در ویدیو ی راهنمایی نشان داده شد استفاده شده است . ***

len50Width8:




New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Users/iman/Desktop/Quartus/len50Width8
Project name: FIRfilter_Len_50_Width_8_
Top-level design entity: FIRfilter_Len_50_Width_8_
Number of files added: 11
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C35F672C6
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: ModelSim (Verilog HDL)
Timing analysis: 0
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help


Quartus II 64-Bit - C:/Users/iman/Desktop/CA1-Ali-imangholi-810197692/Quartus/len50Width8/FIRfilter_Len_50_Width_8_ - FIRfilter_Len_50_Width_8_
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone II: EP2C35F672C6
FIRfilter_Len_50_Width_8_
CU:cu
DP:dp
coefficients_Rom:CoeffRom
registerFile:RF
Hierarchy Files Design Units
Tasks
Flow: Compilation Customize...
Task
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Fitter (Place & Route)
Assembler (Generate programming files
serialFIRfilter.v CU.v DP.v Compilation Report - FIRfilter_Len_50_Width_8_ signed_adder.v
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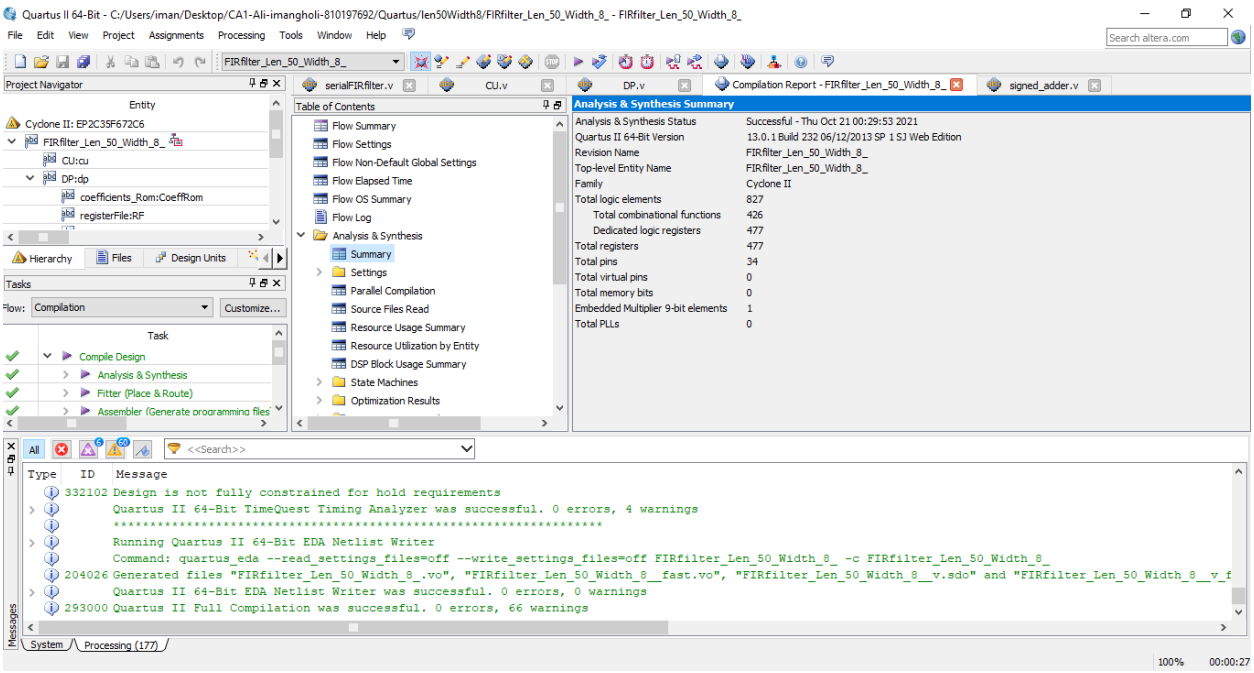
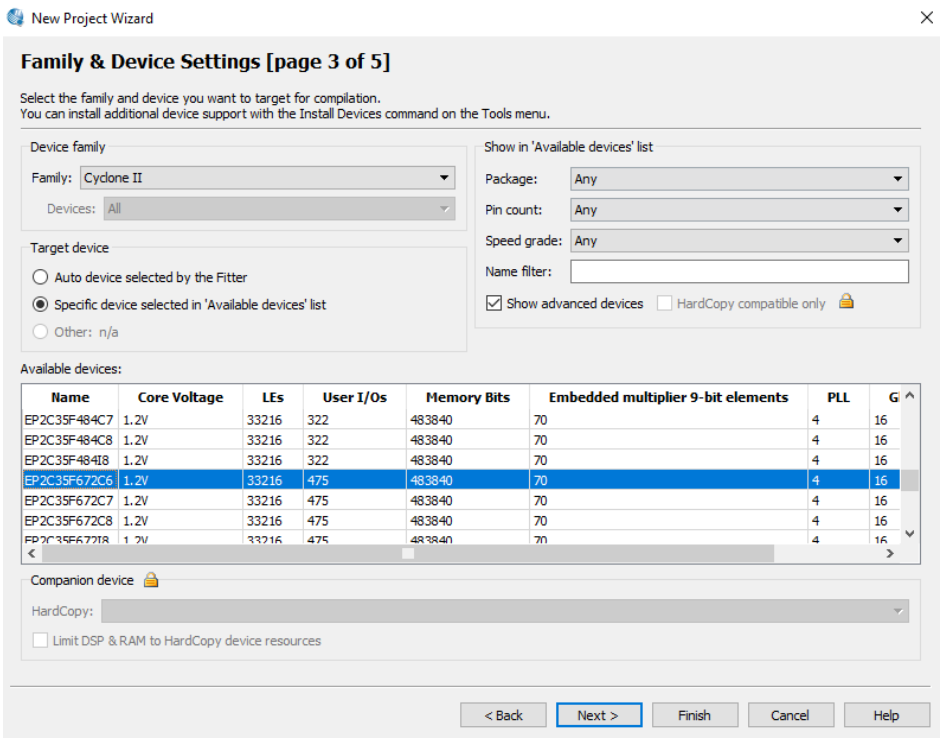
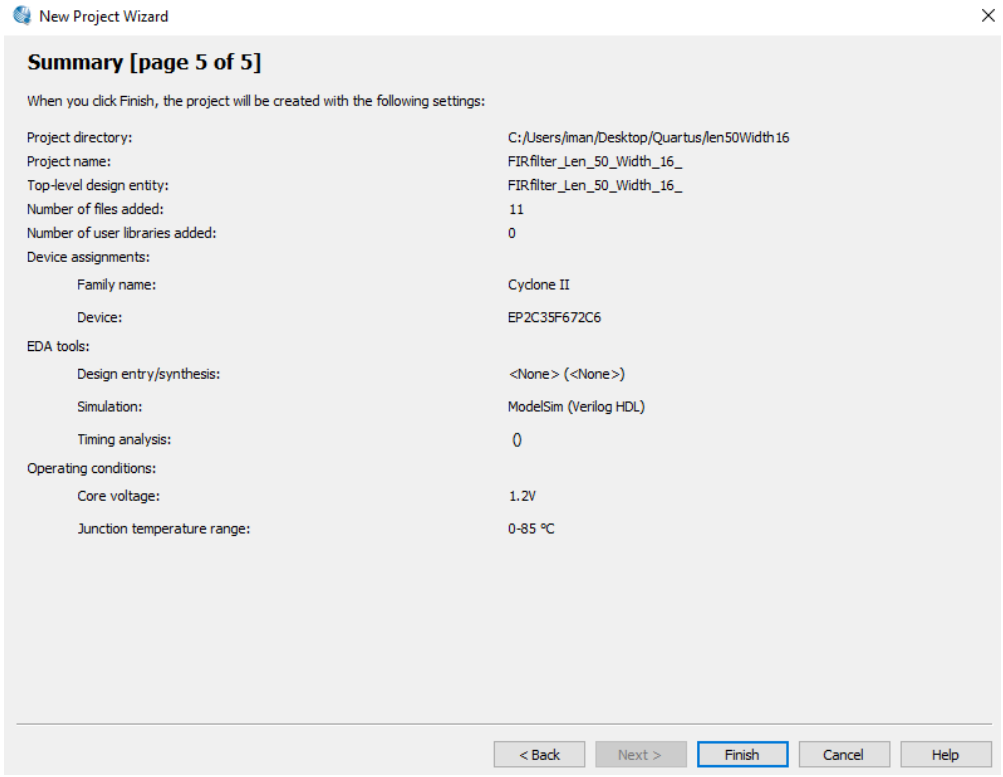
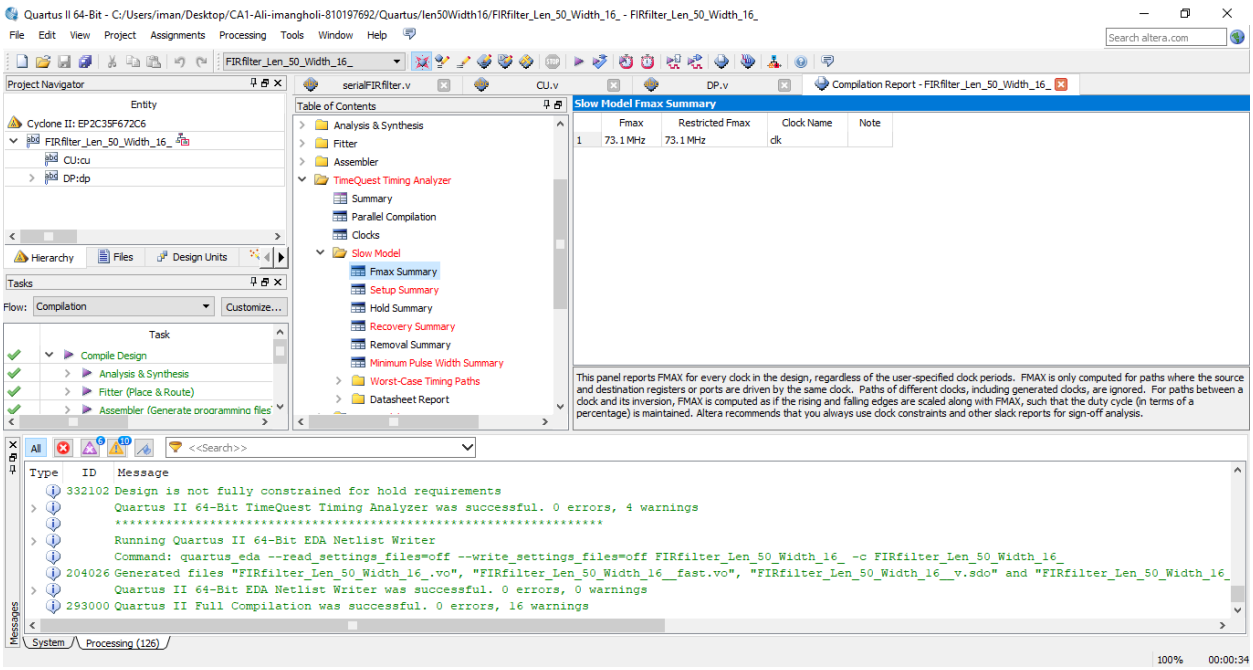
Slow Model
Fmax Summary
Setup Summary
Slow Model Fmax Summary
Fmax Restricted Fmax Clock Name Note
1 88.08 MHz 88.08 MHz clk
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.
Type ID Message
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Running Quartus II 64-Bit EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off FIRfilter_Len_50_Width_8_ -c FIRfilter_Len_50_Width_8_
204026 Generated files "FIRfilter_Len_50_Width_8_.vo", "FIRfilter_Len_50_Width_8__fast.vo", "FIRfilter_Len_50_Width_8__v.sdo" and "FIRfilter_Len_50_Width_8__v_f
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 66 warnings
System Processing (177)



len50Width16:




New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Users/iman/Desktop/Quartus/len50Width16
Project name: FIRfilter_Len_50_Width_16_
Top-level design entity: FIRfilter_Len_50_Width_16_
Number of files added: 11
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C35F672C6
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: ModelSim (Verilog HDL)
Timing analysis: 0
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help


Quartus II 64-Bit - C:/Users/iman/Desktop/CA1-Ali-imangholi-810197692/Quartus/len50Width16/FIRfilter_Len_50_Width_16_ - FIRfilter_Len_50_Width_16_
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone II: EP2C35F672C6
FIRfilter_Len_50_Width_16_
CU:cu
DP:dp
Hierarchy Files Design Units
Tasks
Flow: Compilation Customize...
Task
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Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files
serialFIRfilter.v CU.v DP.v Compilation Report - FIRfilter_Len_50_Width_16_
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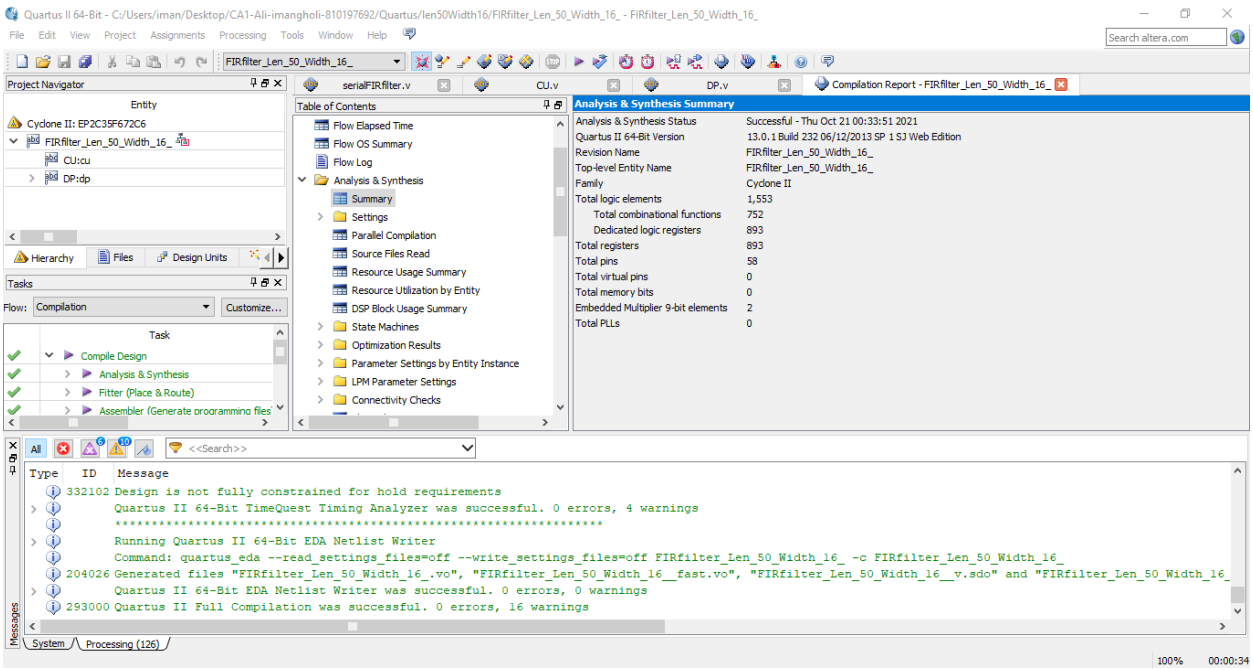
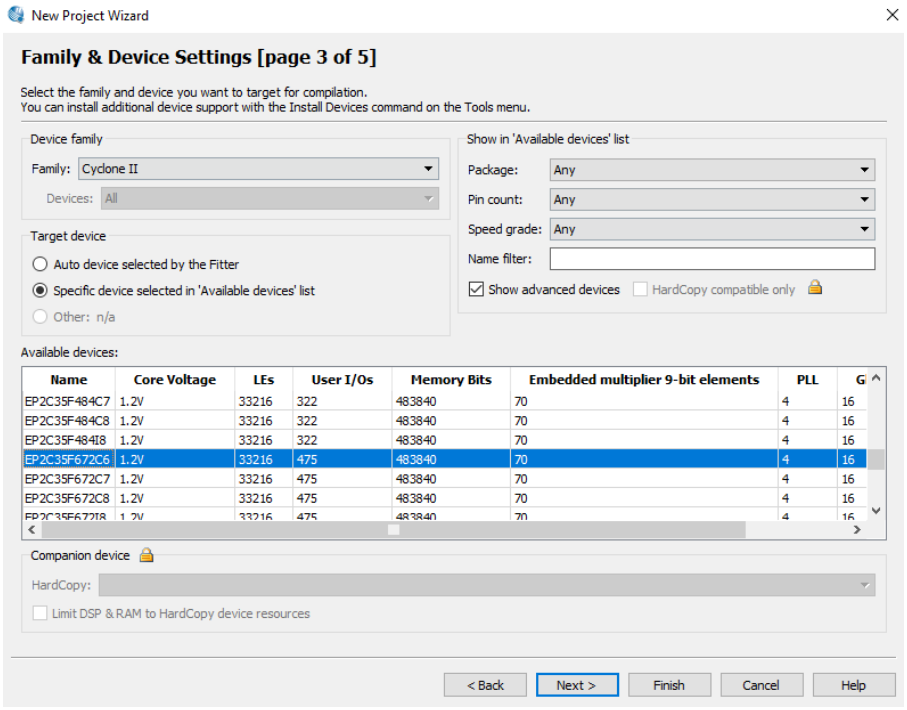
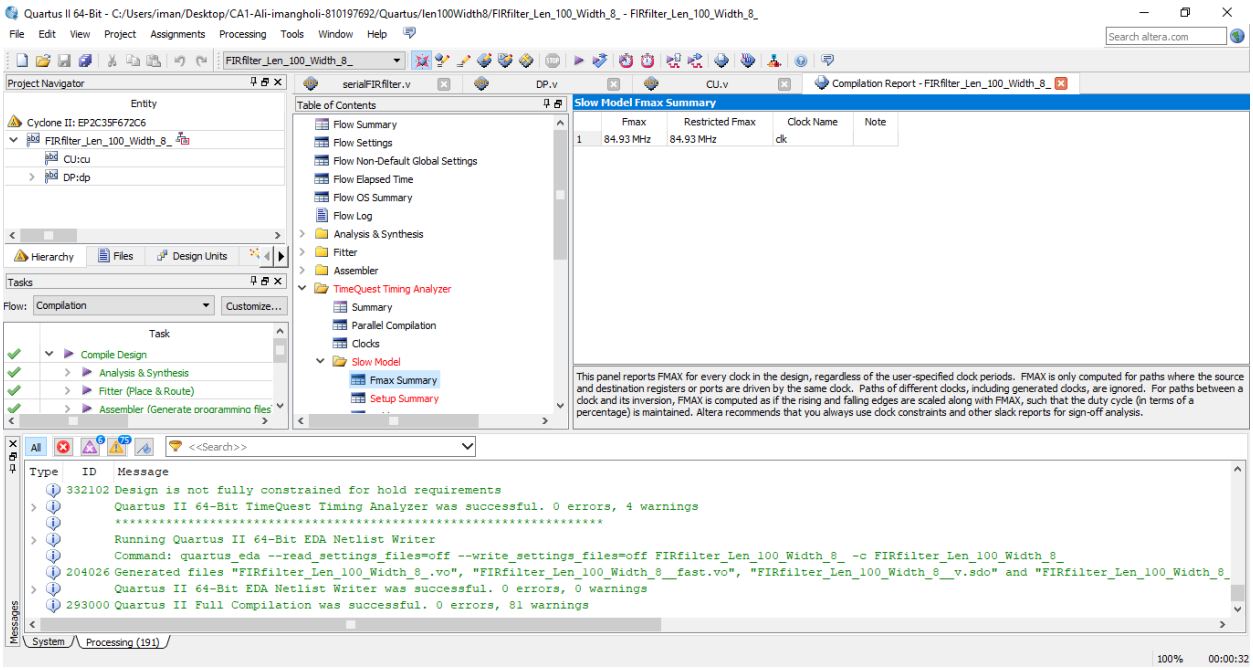
Hold Summary
Recovery Summary
Removal Summary
Minimum Pulse Width Summary
Worst-Case Timing Paths
Datasheet Report
Slow Model Fmax Summary
Fmax Restricted Fmax Clock Name Note
1 73.1 MHz 73.1 MHz clk
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.
Type ID Message
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Running Quartus II 64-Bit EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off FIRfilter_Len_50_Width_16_ -c FIRfilter_Len_50_Width_16_
204026 Generated files "FIRfilter_Len_50_Width_16_.vo", "FIRfilter_Len_50_Width_16__fast.vo", "FIRfilter_Len_50_Width_16__v.sdo" and "FIRfilter_Len_50_Width_16_
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 16 warnings
System Processing (126)
100% 00:00:34



len100Width8:




New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Users/iman/Desktop/Quartus/len100Width8
Project name: FIRfilter_Len_100_Width_8_
Top-level design entity: FIRfilter_Len_100_Width_8_
Number of files added: 10
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C35F672C6
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: ModelSim (Verilog HDL)
Timing analysis: 0
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C


Quartus II 64-Bit - C:/Users/iman/Desktop/CA1-Ali-imangholi-810197692/Quartus/len100Width8/FIRfilter_Len_100_Width_8_ - FIRfilter_Len_100_Width_8_
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone II: EP2C35F672C6
FIRfilter_Len_100_Width_8_
CU:cu
DP:dp
Hierarchy Files Design Units
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Flow: Compilation Customize...
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DP.v
CU.v
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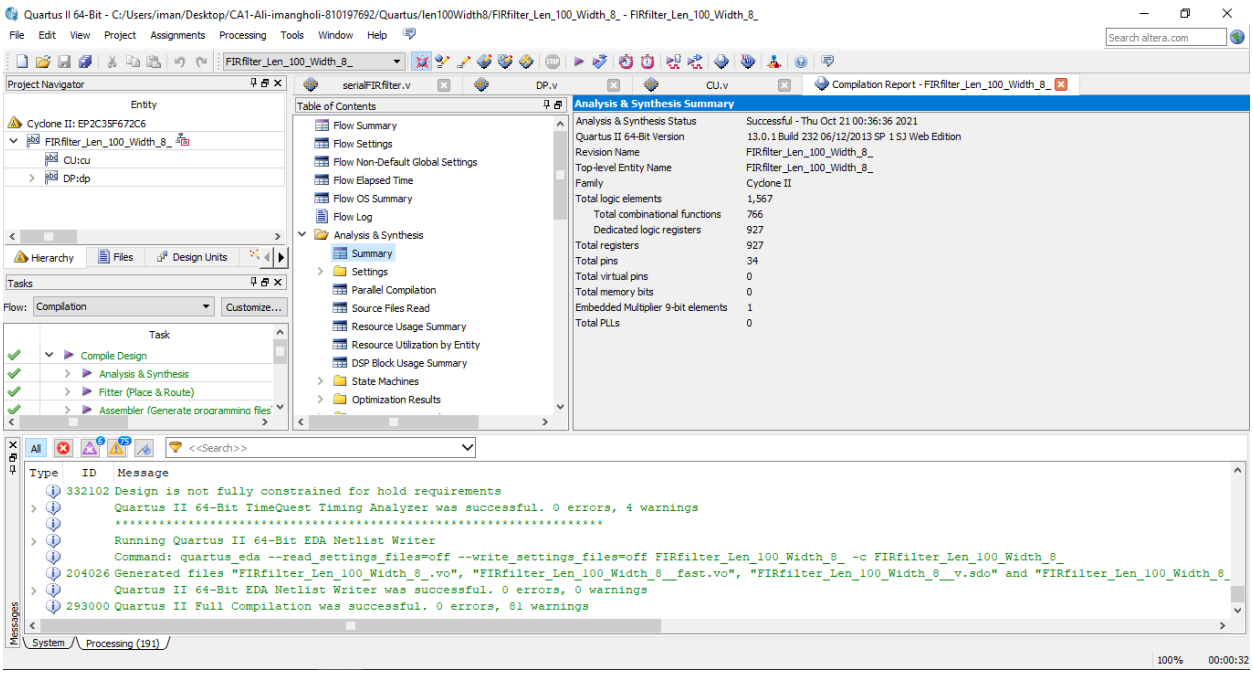
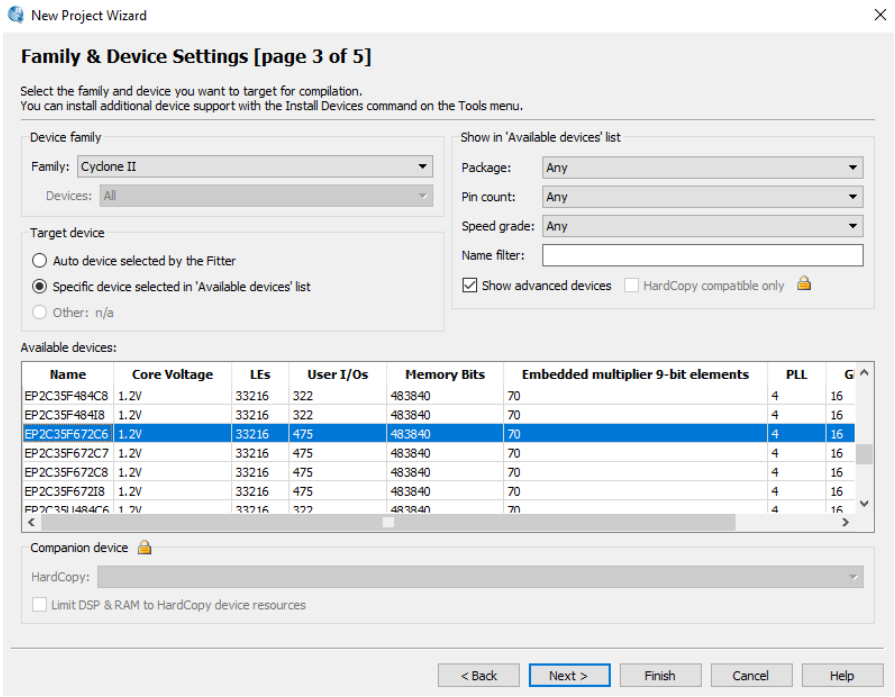
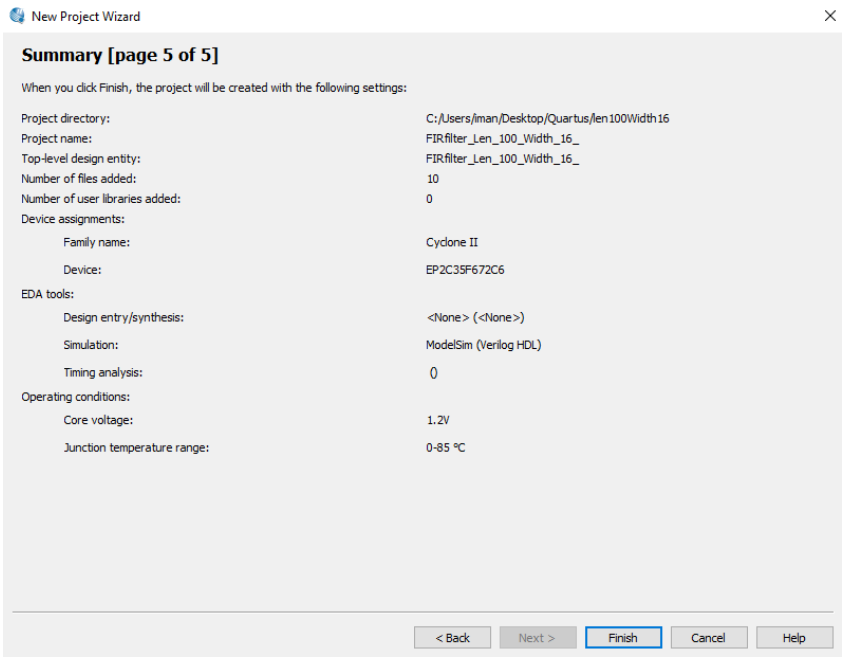
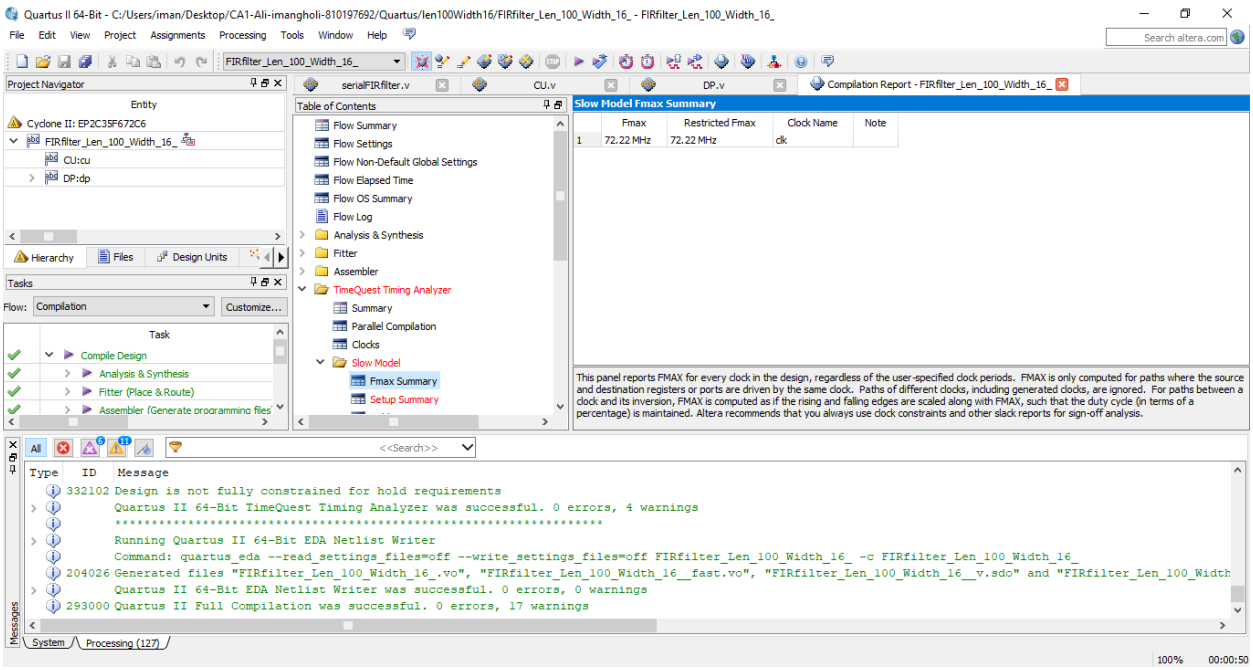
Slow Model
Fmax Summary
Setup Summary
Slow Model Fmax Summary
Fmax Restricted Fmax Clock Name Note
1 84.93 MHz 84.93 MHz clk
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.
Type ID Message
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Running Quartus II 64-Bit EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off FIRfilter_Len_100_Width_8_ -c FIRfilter_Len_100_Width_8_
204026 Generated files "FIRfilter_Len_100_Width_8_.vo", "FIRfilter_Len_100_Width_8__fast.vo", "FIRfilter_Len_100_Width_8__v.sdo" and "FIRfilter_Len_100_Width_8_
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 81 warnings
System Processing (191)
100% 00:00:32



len100Width16:




New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Users/iman/Desktop/Quartus/len100Width16
Project name: FIRfilter_Len_100_Width_16_
Top-level design entity: FIRfilter_Len_100_Width_16_
Number of files added: 10
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C35F672C6
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: ModelSim (Verilog HDL)
Timing analysis: 0
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help


Quartus II 64-Bit - C:/Users/iman/Desktop/CA1-Ali-imangholi-810197692/Quartus/len100Width16/FIRfilter_Len_100_Width_16_ - FIRfilter_Len_100_Width_16_
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone II: EP2C35F672C6
FIRfilter_Len_100_Width_16_
CU:cu
DP:dp
Hierarchy Files Design Units
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Flow: Compilation Customize...
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Compilation Report - FIRfilter_Len_100_Width_16_
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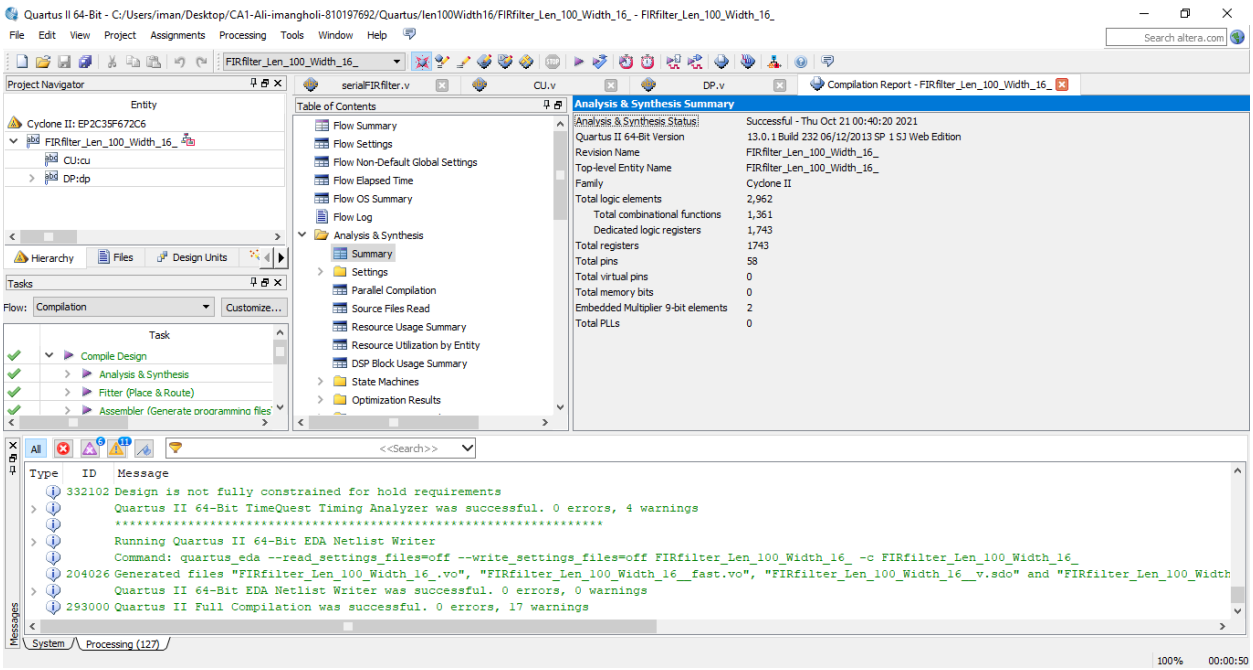
Slow Model Fmax Summary
Fmax Restricted Fmax Clock Name Note
1 72.22 MHz 72.22 MHz clk
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.
Type ID Message
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Running Quartus II 64-Bit EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off FIRfilter_Len_100_Width_16_ -c FIRfilter_Len_100_Width_16_
204026 Generated files "FIRfilter_Len_100_Width_16_.vo", "FIRfilter_Len_100_Width_16__fast.vo", "FIRfilter_Len_100_Width_16__v.sdo" and "FIRfilter_Len_100_Width
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 17 warnings
System Processing (127)
100% 00:00:50



مقایسه ی بین 4 حالت بالا:

	Total logic elements	Total registers
len50Width8	827	477
len50Width16	1553	893
len100Width8	1567	927
len100Width16	2962	1743

مقایسه بین حالت های بالا:

Total logic elements:

len50Width8 < len50Width16 < len100Width8 < len100Width16

همانطور که از جدول بالا مشخص است، با افزایش width و length تعداد قابل توجه ای المان منطقی به مدار اضافه می شود.

Total registers:

len50Width8 < len50Width16 < len100Width8 < len100Width16

همانطور که از جدول بالا مشخص است، با افزایش width و length تعداد قابل توجه ای رجیستر(فیلپ فلاپ) به مدار اضافه می شود.

*** با توجه به جدول بالا به صورت تقریبی، رجیستر ها (فیلپ فلاپ ها) نصف المان های منطقی هر سطر را تشکیل می دهند.