Digital
ELECTRONICS

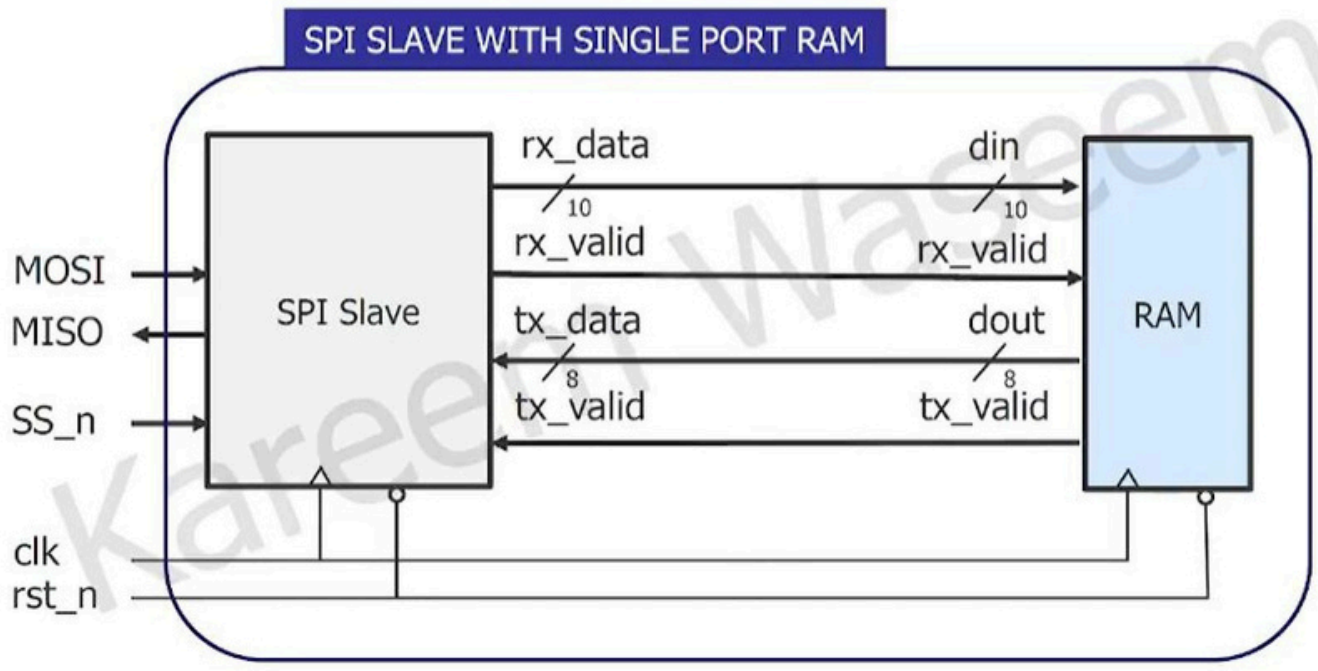
SPI INTERFACE WITH RAM

Detailed report

SURF THE PROJECT FILES:

GitHub link: https://github.com/Ali-Mohamed-cairo/Digital_E_SPI_RAM.git

Target block diagram



Contents:

RTL Code

A)RAM:

RAM.v

```
1   module RAM(din, rx_valid, clk, rst_n, tx_valid, dout);
2   //Define the module parameters
3   parameter  ADDR_SIZE = 8,
4              MEM_DEPTH = 2**ADDR_SIZE;
5   //Specify the inputs of module
6   input [ADDR_SIZE+1 : 0] din;
7   input rx_valid, clk, rst_n;
8   //Specify the outputs of module
9   output reg tx_valid;
10  output reg [ADDR_SIZE-1 : 0] dout;
11
12  //The memory unit declaration
13  reg [ADDR_SIZE-1 : 0] mem[MEM_DEPTH-1 : 0], Address_Saver;
14
15  //Block function
16
17  always @(posedge clk) begin
18      if(~rst_n) begin //Synchroneous active low reset
19          dout     <= 0;
20          tx_valid <= 0;
21          Address_Saver <= 0;
22      end
```

A)RAM(Cont.):


```
    else
        case(din[ADDR_SIZE+1])
        1'b0://Write commands
        begin
            if(rx_valid) begin
                dout     <= 0;
                tx_valid <= 0;
                case(din[ADDR_SIZE])
                //Write address command
                1'b0: Address_Saver      <= din[ADDR_SIZE-1 : 0];
                //Write data command
                1'b1: mem[Address_Saver] <= din[ADDR_SIZE-1 : 0];
                endcase
            end
        end
        1'b1://Read commands
        begin
            case(din[ADDR_SIZE])
            //Read address command
            1'b0:
            begin
                dout     <= 0;
                tx_valid <= 0;
                Address_Saver <= din[ADDR_SIZE-1 : 0];
            end
            //Read data command
            1'b1:
            begin
                dout     <= mem[Address_Saver];
                tx_valid <= 1;
            end
            endcase
        end
        endcase
end
endmodule
```

B)GPR(General purpose register):[5]

GPR.v

```v
module GPR(Parallel_In_SR, Serial_In_SR, Load, clk_SR, rst_n_SR, Parallel_Out_SR);
parameter WIDTH_SR = 8;

//Specify the module inputs
input  [WIDTH_SR-3 : 0] Parallel_In_SR;
input  Serial_In_SR, Load, clk_SR, rst_n_SR;

//Specify the module outputs
output reg [WIDTH_SR-1 : 0] Parallel_Out_SR;

//Module funcitonality
always @(posedge clk_SR) begin
    if(~rst_n_SR)
        Parallel_Out_SR <= 0;
    else
        if(Load)
            Parallel_Out_SR <= {Parallel_In_SR, 2'b00};
        else
            Parallel_Out_SR <=(Parallel_Out_SR << 1) | Serial_In_SR;

end
endmodule
```

C)Counter:

Counter.v

```v
module Counter(start, clk_c, rstn_c, count_c);
//parameter
parameter WIDTH = 4;

//Input signal declaration
input clk_c, rstn_c, start;

//Output signal declaration
output reg [WIDTH-1 : 0] count_c;

//Module functionality
always @(posedge clk_c) begin
    if(~rstn_c)
        count_c <= 0;
    else
        if(start)
            count_c <= count_c + 1;
end

endmodule
```

D)SPI Slave:

SPI_Slave.v

```v
//Some definitions can be used when instantiating the module(Depend on the user)
`define READ_ADD_CASE       0
`define READ_DATA_CASE      1
`define ACTIVE_LOW          0
`define ACTIVE_HIGH         1
`define CLEAR               0
`define SET                 1
module SPI_Slave(MOSI, MISO, SS_n, rx_data, rx_valid, tx_data, tx_valid, clk, rst_n);
//Parameters declaration
parameter ADDR_SIZE  = 8;
localparam COUNTER_WIDTH = 5,
           IDLE      = 0,  //We have five main states in which the module will be operating in one of them:
           CHK_CMD   = 1,  //1- IDLE state    -> Accessed when reset and at the end of any command.
           WRITE     = 2,  //2- CHK_CMD state -> Accessed when break the IDLE state.
           READ_ADD  = 3,  //3- WRITE         -> It's the state in which the module is when execute any write command (address or data).
           READ_DATA = 4;  //4- READ_ADD      -> It's the state when there is an address is sent to RAM to be used when read data.
                           //5- READ_DATA     -> It's the state when you want to read data from the RAM block.
//Declare module inputs
input  MOSI, SS_n, tx_valid, clk, rst_n;
input  [ADDR_SIZE-1 : 0] tx_data;

//Declare module outputs
output reg MISO;   //Serial output terminal.
output reg rx_valid;
output reg [ADDR_SIZE+1 : 0] rx_data;

wire [COUNTER_WIDTH-1 : 0] counter_out;
wire [ADDR_SIZE+1 : 0] GPR_Out;
reg Counter_rst, Load_GPR, Read_case;

//An attribute to choose the required binary coding which will be used during synthesising.
(* fsm_encoding = "gray" *)
//Choose gray, one_hot or sequential
reg [2:0] cs, ns; // cs: Current State ,   ns : Next State

//Counter instantiation
Counter #(.WIDTH(5)) SPI_Counter(.start((~SS_n)), .clk_c(clk), .rstn_c(Counter_rst), .count_c(counter_out));
```

D)SPI Slave(Cont.):

```
38
39  //GPR instantiation
40  GPR #(.WIDTH_SR(ADDR_SIZE+2)) GPReg(
41      .Parallel_In_SR(tx_data), .Serial_In_SR(MOSI), .Load(Load_GPR), .clk_SR(clk),
42      .rst_n_SR(rst_n), .Parallel_Out_SR(GPR_Out)
43  );
44
45  /*This module will be treated as FSM(Finite State Machine), so that it has three main blocks:
46  *1- Next state block
47  *2- Memory stage logic
48  *3- Output logic
49  */
50  //Memory stage logic + Output logic
51  always @(posedge clk) begin
52      //Synchroueous active low reset signal to be used when need and when power on.
53      if(~rst_n) begin
54          cs <= IDLE;
55          rx_data  <= `CLEAR;
56          rx_valid <= `CLEAR;
57          Read_case <= `READ_ADD_CASE;
58          MISO <= `CLEAR;
59          Load_GPR <= `CLEAR;
60      end
61      else begin
62          cs <= ns;
63          //Handling output at the IDLE state.
64          if(cs == IDLE) begin
65              rx_data  <= 0;
66              rx_valid <= 0;
67          end
68          //Handling the output at the WRITE or READ_ADD state.
69          if(cs == WRITE || cs == READ_ADD) begin
70              if(counter_out == ADDR_SIZE+3) begin//Preparation of data to be sent to the RAM is ended.
71                  rx_data  <= GPR_Out;
72                  rx_valid <= 1;
73                  if(cs == READ_ADD) //Switching to the need read state(READ_DATA).
74                      Read_case <= ~Read_case;
75              end
76          end
```

D)SPI Slave(Cont.):

```
77          //Handling the output at  the READ_DATA state.
78          else if(cs == READ_DATA) begin
79              //Data is still not ready to be read
80              if(~tx_valid) begin
81                  if(counter_out == ADDR_SIZE+3) begin //Preparation of the command to be sent to the RAM is ended.
82                      rx_data  <= GPR_Out;
83                      rx_valid <= 1;
84                  end
85              end
86              //Data is ready to be read
87              else if(tx_valid) begin
88                  if(counter_out == ADDR_SIZE+5)//Load data to the GPR
89                      Load_GPR <= `SET;
90                  else if(counter_out == 15)//Turn off the LOAD signal after data is being loaded
91                      Load_GPR <= `CLEAR;
92                  else begin                //Send data via the MISO terminal
93                      MISO <= GPR_Out[ADDR_SIZE+1];
94                      if(counter_out == ADDR_SIZE+19) begin
95                          Read_case <= ~Read_case; //Switching to the need read state(READ_ADD).
96                      end
97                  end
98              end
99          end
100     end
101 end
```

D)SPI Slave(Cont.):

```
102
103   //Next state logic
104   //Handle the next state at which the FSM must transfer to depending on the current inputs and the current state.
105   always @(*) begin
106       case(cs)
107       IDLE:
108       begin
109           Counter_rst = 0;
110           if(~SS_n)
111               ns = CHK_CMD;
112       end
113       CHK_CMD:
114       begin
115           if(SS_n)
116               ns = IDLE;
117           else begin
118               if(~MOSI)
119                   ns = WRITE;
120               else begin
121                   if(~Read_case)
122                       ns = READ_ADD;
123                   else
124                       ns = READ_DATA;
125               end
126               Counter_rst = 1;
127           end
128       end
129       WRITE:
130           if(SS_n) begin
131               Counter_rst = 0;
132               ns = IDLE;
133           end
134       READ_ADD:
135           if(SS_n) begin
136               Counter_rst = 0;
137               ns = IDLE;
138           end
```

D)SPI Slave(Cont.):

```
139         READ_DATA:
140             if(SS_n) begin
141                 Counter_rst = 0;
142                 ns = IDLE;
143             end
144         default: ns = IDLE;
145         endcase
146     end
147
148
149     endmodule
```

E)SPI Wrapper:

SPI_Wrapper.v

```v
module SPI_Wrapper(MOSI_W, SS_n_W, clk_W, rst_n_W, MISO_W);
//Parameters declaration
parameter WIDTH = 8;

//Inputs declarations
input MOSI_W, SS_n_W, clk_W, rst_n_W;

//Output declaration
output MISO_W;

//Internal signals declarations
wire [WIDTH+1 : 0] rx_data_W;
wire rx_valid_W, tx_valid_W;
wire [WIDTH-1 : 0] tx_data_W;


//Modules instantiations
//Instantiate the SPI Slave module
SPI_Slave #(.ADDR_SIZE(WIDTH)) Slave(
    .MOSI(MOSI_W), .MISO(MISO_W), .SS_n(SS_n_W), .rx_data(rx_data_W), .rx_valid(rx_valid_W),
    .tx_data(tx_data_W), .tx_valid(tx_valid_W), .clk(clk_W), .rst_n(rst_n_W)
);

//Instantiate the RAM block
RAM #(.ADDR_SIZE(WIDTH)) RAM_Unit(
    .din(rx_data_W), .rx_valid(rx_valid_W), .clk(clk_W), .rst_n(rst_n_W), .tx_valid(tx_valid_W), .dout(tx_data_W)
);

endmodule
```

Testbenches

A)RAM testbench:

RAM_tb.v

```
module RAM_test;
parameter MEM_DEPTH_tb = 15,
          ADDR_SIZE_tb = 8;
//Signals declarations
reg [ADDR_SIZE_tb+1 : 0] din_tb;
reg rx_valid_tb, clk_tb, rst_n_tb;
wire tx_valid_tb;
wire [ADDR_SIZE_tb-1 : 0] dout_tb;

//Module instantiation
RAM #(.MEM_DEPTH(MEM_DEPTH_tb), .ADDR_SIZE(ADDR_SIZE_tb)) R(
    .din(din_tb), .rx_valid(rx_valid_tb), .clk(clk_tb), .rst_n(rst_n_tb), .tx_valid(tx_valid_tb), .dout(dout_tb)
);

//Generate the module clock signal
initial begin
    clk_tb = 1;
    forever #1 clk_tb =~clk_tb;
end

initial begin
    //Test the Synchroneous active low reset signal
    rst_n_tb = 0;
    din_tb = 14; rx_valid_tb = 1;
    @(negedge clk_tb);
    rst_n_tb = 1;
    @(negedge clk_tb);
    //Randomized testing
    repeat(10) begin
        din_tb = $random; rx_valid_tb = $random;
        @(negedge clk_tb);
    end
    $stop;
end

endmodule
```

B)SPI Wrapper testbench:

SPI_Wrapper_tb.v

```v
module SPI_tb;
//Signals declaration
parameter WIDTH_tb = 8;
reg MOSI_W_tb, SS_n_W_tb, clk_W_tb, rst_n_W_tb;
wire MISO_W_tb;

//Module instantiation
SPI_Wrapper #(.WIDTH(WIDTH_tb)) SPI_W_tb(
    .MOSI_W(MOSI_W_tb), .SS_n_W(SS_n_W_tb), .clk_W(clk_W_tb), .rst_n_W(rst_n_W_tb), .MISO_W(MISO_W_tb)
);

reg [7:0] i;

initial begin
    clk_W_tb = 1;
    forever #1  clk_W_tb = ~clk_W_tb;
end

//Directed testing
initial begin
    //Test the reset signal.
    rst_n_W_tb = 0;
    SS_n_W_tb = 0;  MOSI_W_tb = 0;
    @(negedge clk_W_tb);
    rst_n_W_tb = 1;
```

B)SPI Wrapper testbench(Cont.):

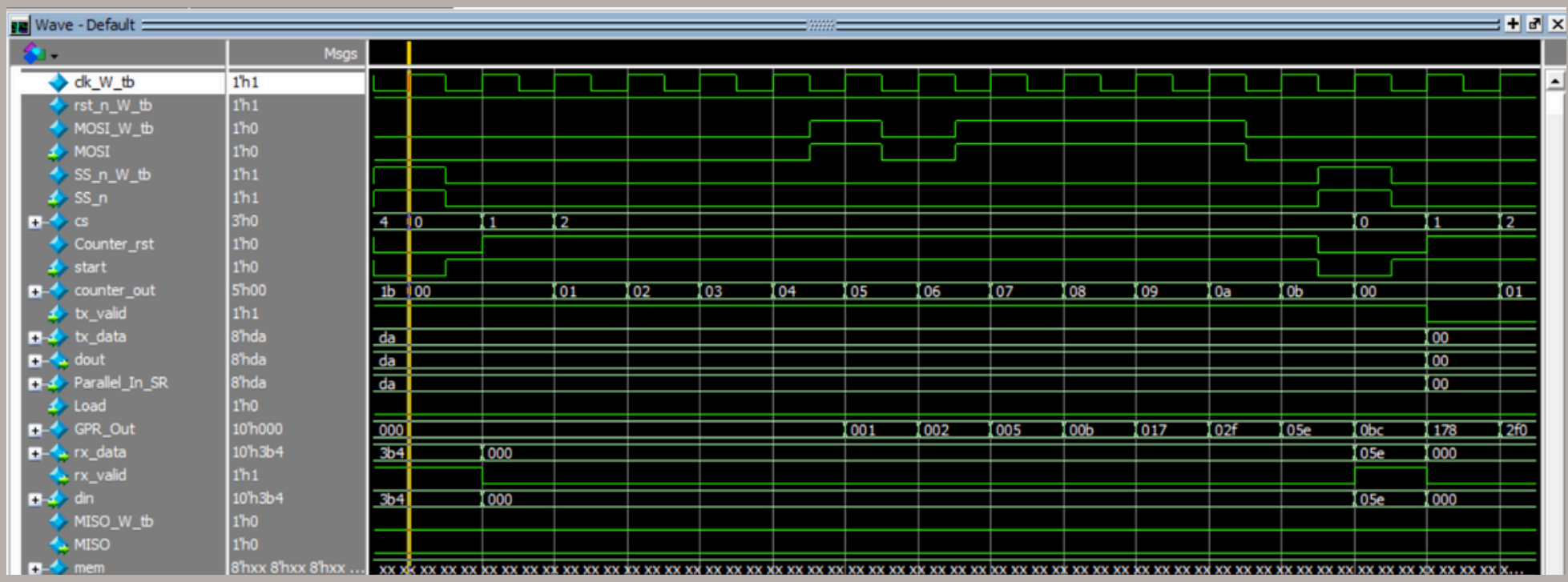
```
26      /**********************Write address and data then read address and data four successive times.**********************************/
27      repeat(4) begin
28          i = 0; //This bus is required for the reading and writing from the same memory address purpose even using randomized testing.
29          //The write address command code
30          SS_n_W_tb = 0;  MOSI_W_tb = 0;
31          @(negedge clk_W_tb);
32          @(negedge clk_W_tb);
33          MOSI_W_tb = 0;
34          @(negedge clk_W_tb);
35          MOSI_W_tb = 0;
36          @(negedge clk_W_tb);
37          //Test writing address (Randomized)
38          repeat(WIDTH_tb) begin
39              MOSI_W_tb = $random;
40              i = (i << 1) | MOSI_W_tb;
41              @(negedge clk_W_tb);
42          end
43          SS_n_W_tb = 1; // End of master sending sequence.
44          @(negedge clk_W_tb);
45          //The write data command code
46          SS_n_W_tb = 0; MOSI_W_tb = 0;
47          @(negedge clk_W_tb);
48          @(negedge clk_W_tb);
49          MOSI_W_tb = 0;
50          @(negedge clk_W_tb);
51          MOSI_W_tb = 1;
52          @(negedge clk_W_tb);
53          //Test writing data (Randomized)
54          repeat(WIDTH_tb) begin
55              MOSI_W_tb = $random;
56              @(negedge clk_W_tb);
57          end
58          SS_n_W_tb = 1; // End of master sending sequence.
```

B)SPI Wrapper testbench(Cont.):

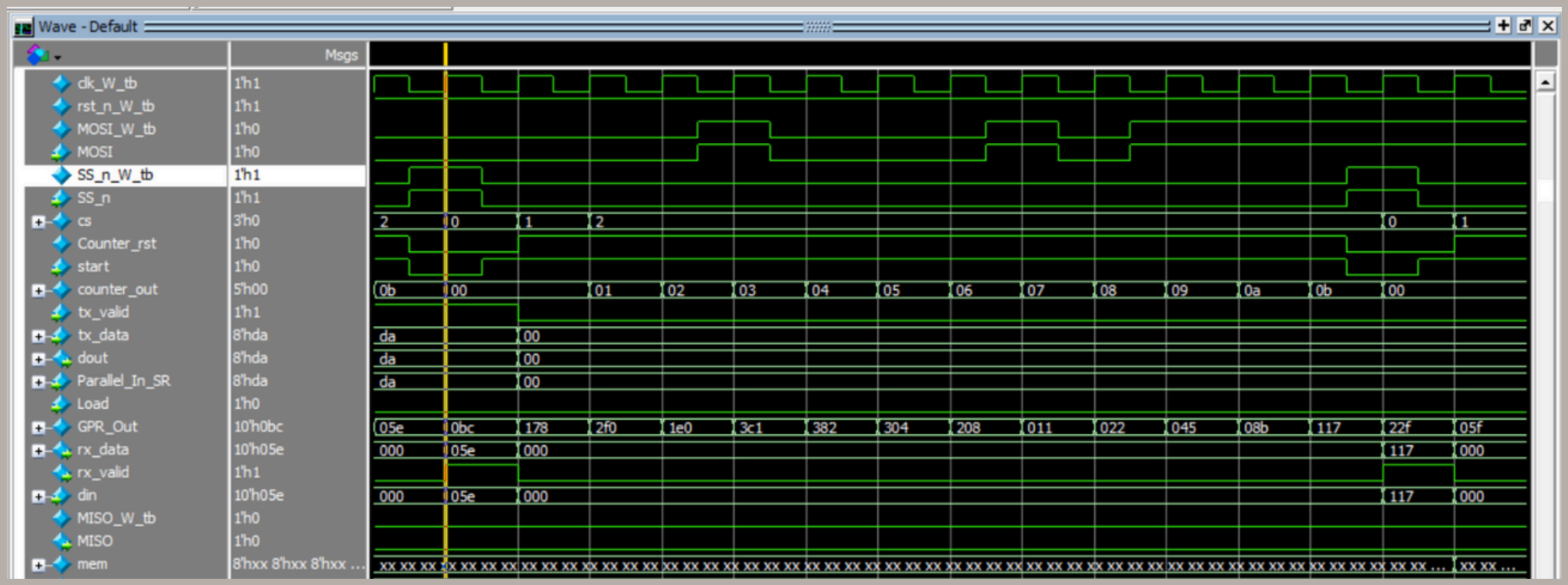
```
        //The read address command code
        SS_n_W_tb = 0; MOSI_W_tb = 1;
        @(negedge clk_W_tb);
        @(negedge clk_W_tb);
        MOSI_W_tb = 1;
        @(negedge clk_W_tb);
        MOSI_W_tb = 0;
        @(negedge clk_W_tb);
        //Test read address  (Based on the previously entered one)
        repeat(WIDTH_tb) begin
            MOSI_W_tb = i[7];
            i = i << 1;
            @(negedge clk_W_tb);
        end
        SS_n_W_tb = 1; // End of master sending sequence.
        @(negedge clk_W_tb);
        //The read data command code
        SS_n_W_tb = 0; MOSI_W_tb = 1;
        @(negedge clk_W_tb);
        @(negedge clk_W_tb);
        MOSI_W_tb = 1;
        @(negedge clk_W_tb);
        MOSI_W_tb = 1;
        @(negedge clk_W_tb);
        //Test read data
        repeat(WIDTH_tb) begin
            MOSI_W_tb = $random;
            @(negedge clk_W_tb);
        end
        repeat(2*WIDTH_tb) begin
            @(negedge clk_W_tb);
        end
        SS_n_W_tb = 1;
        @(negedge clk_W_tb);
    end
    $stop;
end
endmodule
```

QUESTASIM SIMULATION RESULTS(WAVEFORMS)

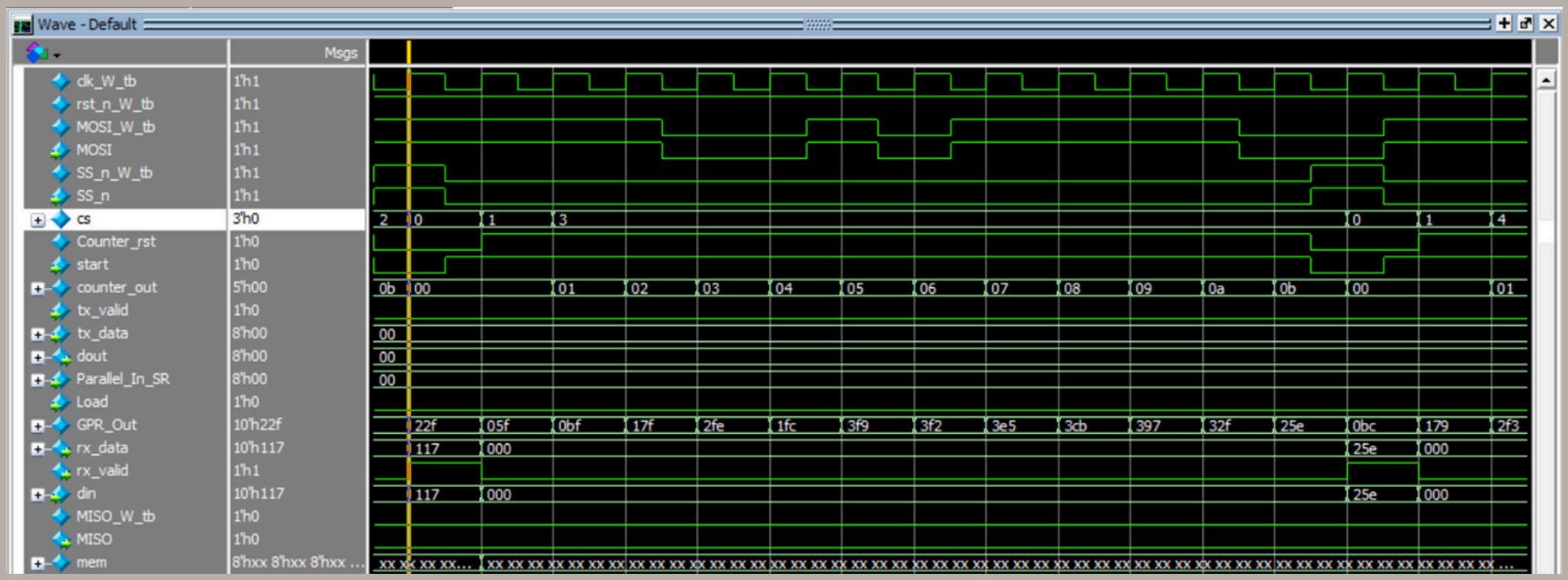
A)Write Address command:



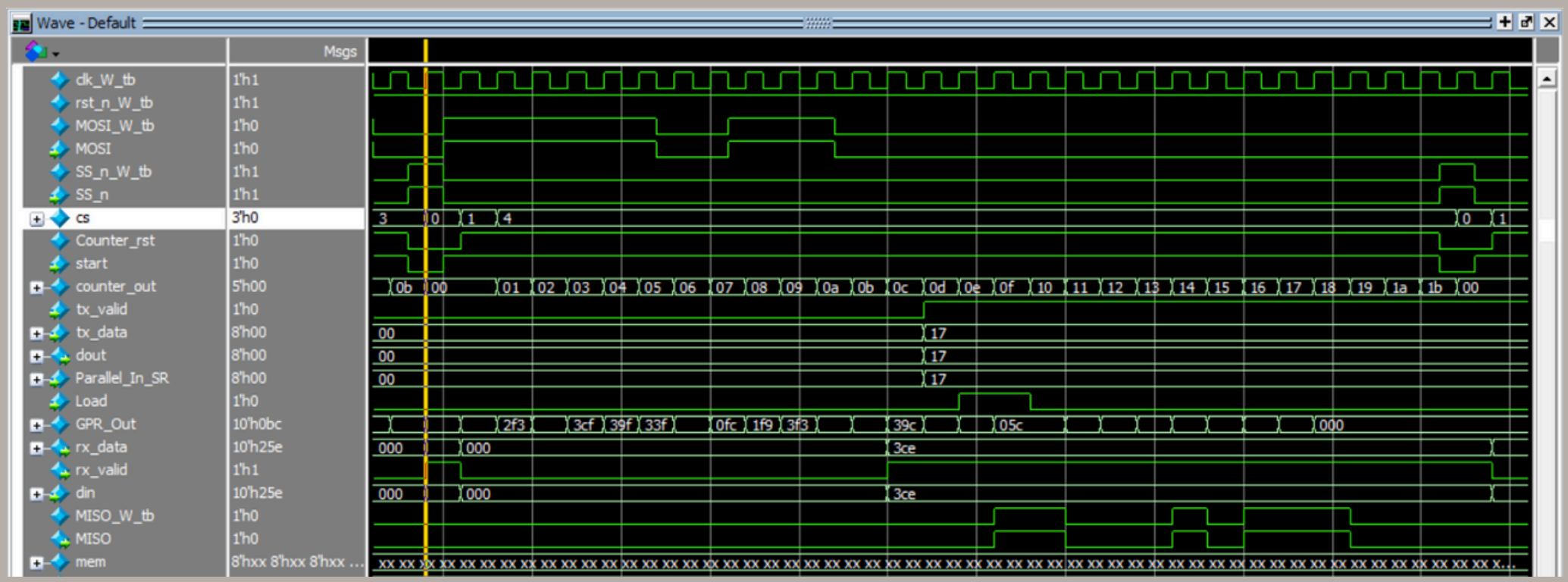
B)Write Data command:



C)Read address command:



D)Read Data command:

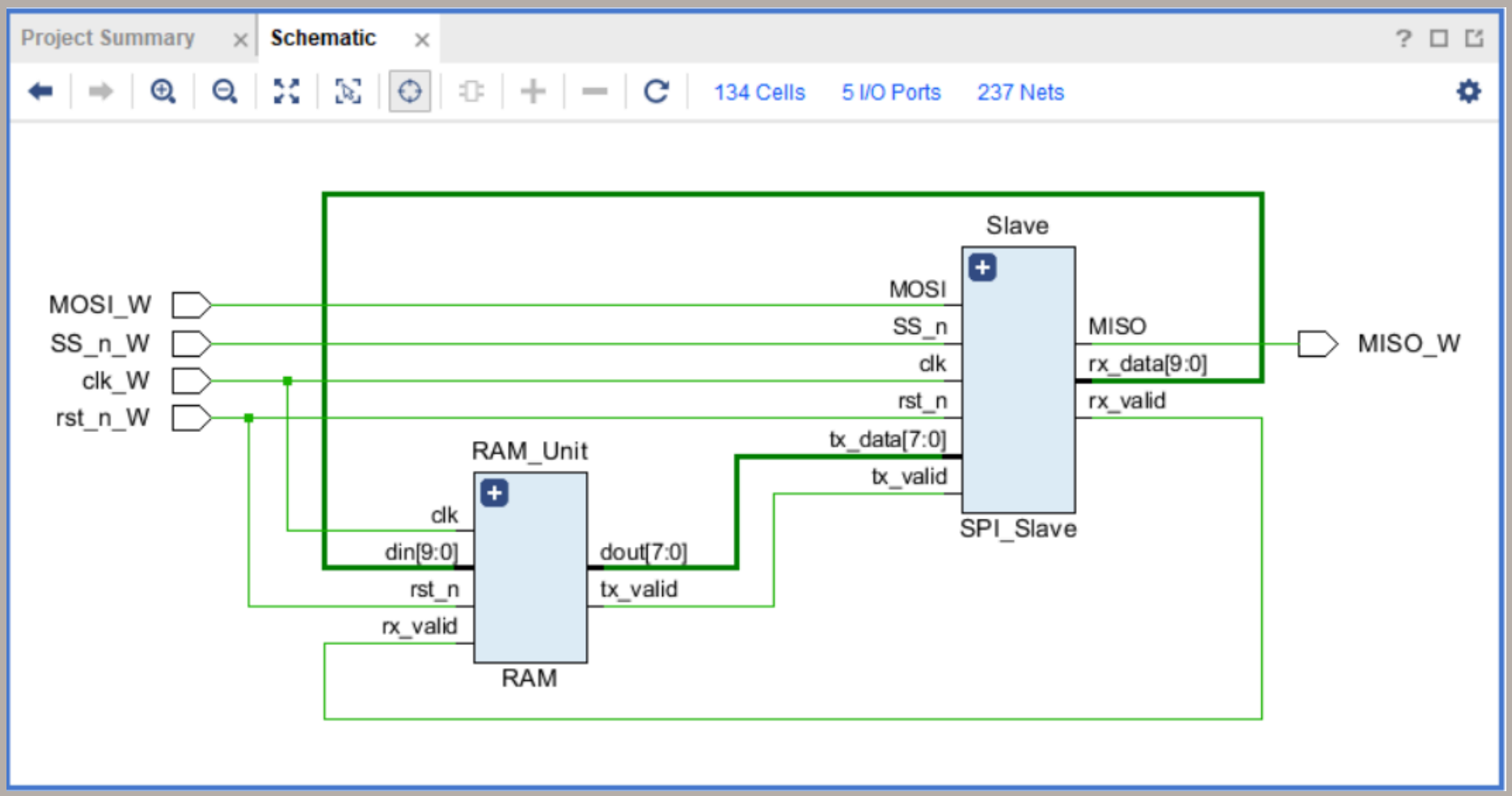


Do file


```
vlib work

vlog SPI_Wrapper.v SPI_Slave.v RAM.v GPR.v Counter.v SPI_Wrapper_tb.v

vsim -voptargs=+acc work.SPI_tb

add wave -position insertpoint  \
sim:/SPI_tb/clk_W_tb

add wave -position insertpoint  \
sim:/SPI_tb/rst_n_W_tb

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/SS_n

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/MOSI

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/cs

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/Counter_rst

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/SPI_Counter/start

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/counter_out

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/tx_valid

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/tx_data

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/RAM_Unit/dout

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/GPReg/Parallel_In_SR

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/GPReg/Load

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/GPR_Out

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/rx_data

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/rx_valid

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/RAM_Unit/din

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/Slave/MISO

add wave -position insertpoint  \
sim:/SPI_tb/SPI_W_tb/RAM_Unit/mem

run -all
```

Elaboration using vivado

A)Schematic:



B)Message box:

Tcl Console | Messages | Log | Reports | Design Runs

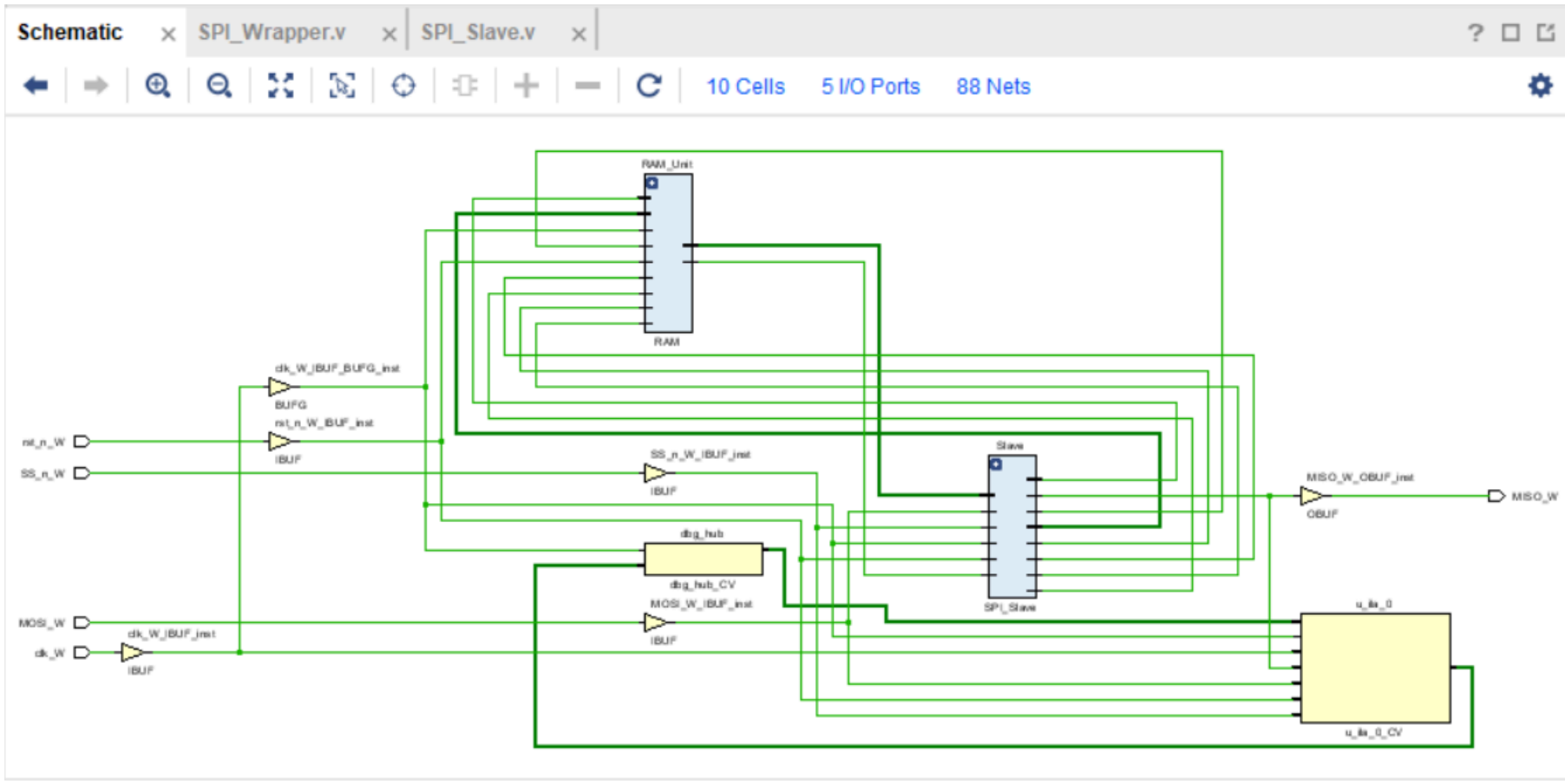
Warning (3) | Info (53) | Status (54) | Show All

- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'P:/Programs_installed/Xilinx/Vivado/2018.2/data/ip'.
- Elaborated Design (14 infos)
  - General Messages (14 infos)
    - [Synth 8-6157] synthesizing module 'SPI_Wrapper' [SPI_Wrapper.v:1] (4 more like this)
    - [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI_Slave.v:27]
    - [Synth 8-6155] done synthesizing module 'Counter' (1#1) [Counter.v:1] (4 more like this)
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
- Synthesis (3 warnings, 36 infos)
  - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  - [Synth 8-6157] synthesizing module 'SPI_Wrapper' [SPI_Wrapper.v:1] (4 more like this)
  - [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI_Slave.v:27]
  - [Synth 8-6155] done synthesizing module 'Counter' (1#1) [Counter.v:1] (4 more like this)
  - [Device 21-403] Loading part xc7a35ticpg236-1L
  - [Project 1-236] Implementation specific constraints were found while reading constraint file [O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/SPI_Wrapper_propImpl.xdc].
    Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  - [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
  - [Synth 8-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse (2 more like this)
  - [Synth 8-5544] ROM "rx_data" won't be mapped to Block RAM because address size (3) smaller than threshold (5) (2 more like this)
  - [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'
  - [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [SPI_Slave.v:92] (1 more like this)
  - [Synth 8-4480] The timing for the instance i_0/RAM_Unit/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)

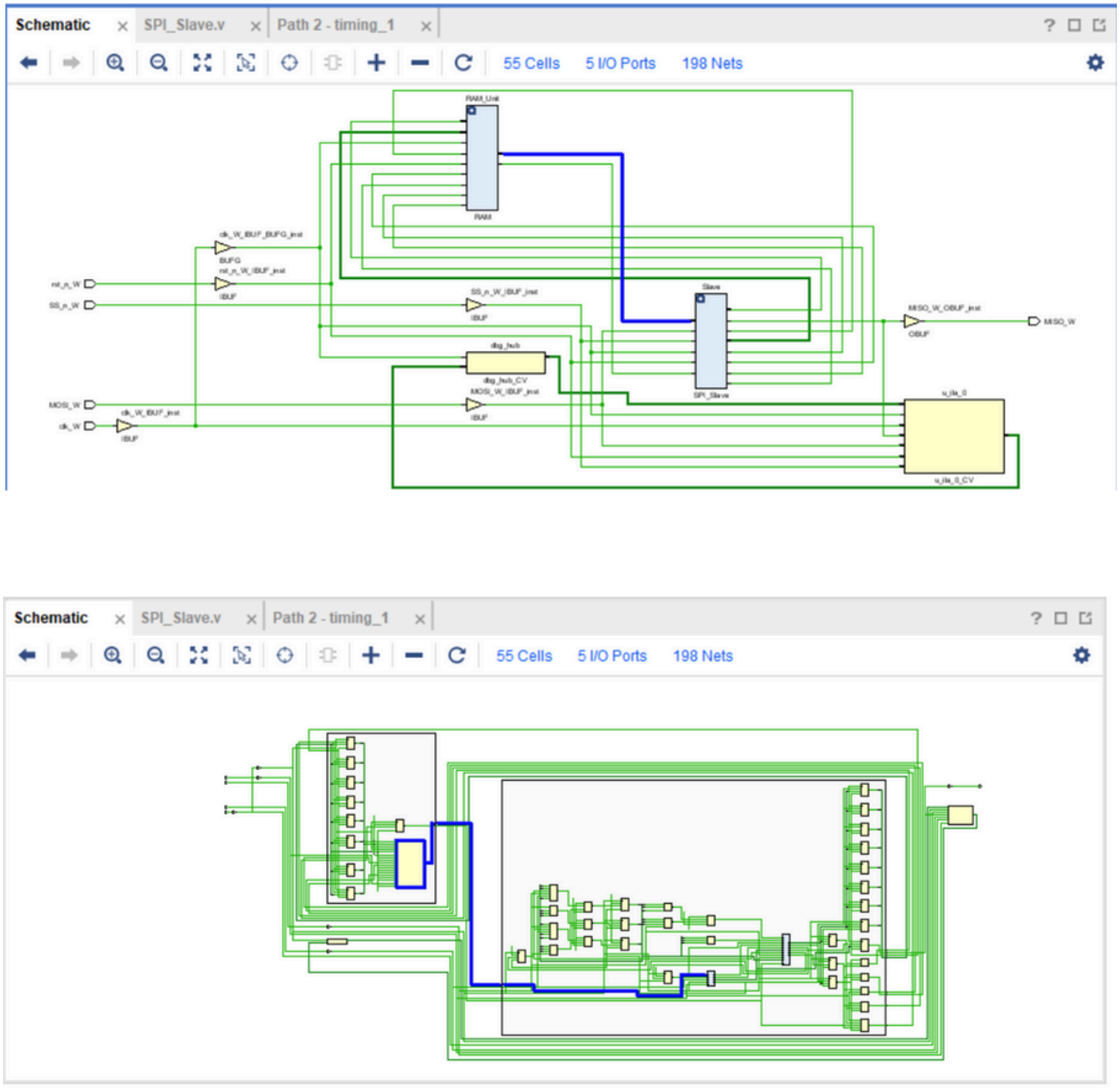
SYNTHESIS USING VIVADO

A)Gray Code:

->>Schematic:



->>Critical path:



->>Messages:

Tcl Console | Messages | Log | Reports | Design Runs | Debug

Warning (3) | Info (54) | Status (73) | Show All

- [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
- [Synth 8-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse (2 more like this)
- [Synth 8-5544] ROM "rx_data" won't be mapped to Block RAM because address size (3) smaller than threshold (5) (2 more like this)
- [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'
- [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [SPI_Slave.v:111] (1 more like this)
- [Synth 8-4480] The timing for the instance i_0/RAM_Unit/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 9 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/SPI_Wrapper.runs/synth_1/SPI_Wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Mon Aug 5 17:30:42 2024...

Synthesized Design (6 infos)

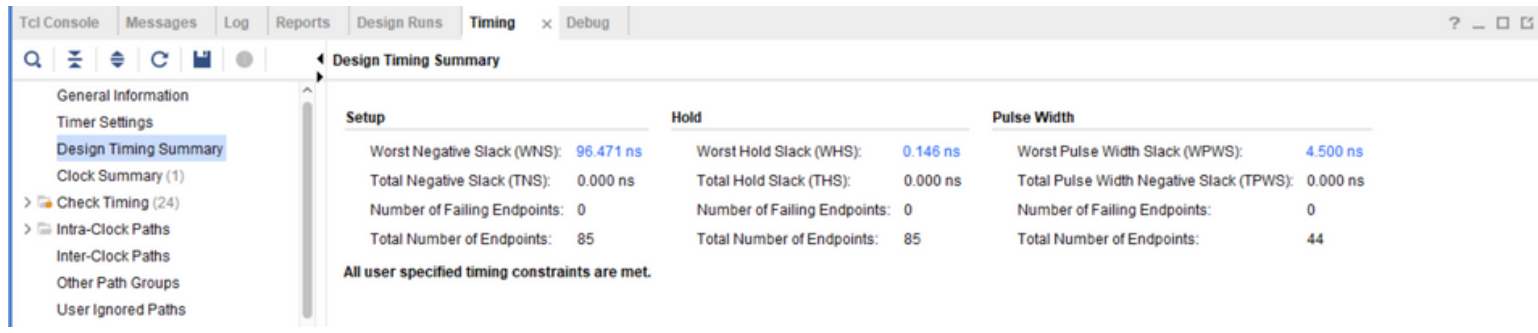
General Messages (6 infos)

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed.

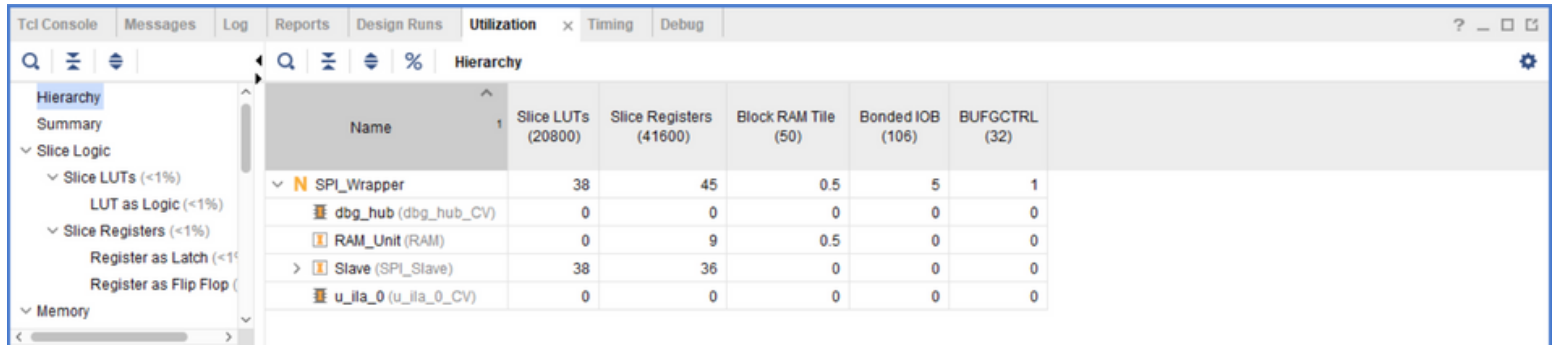
->>Report:

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

->>Timing:

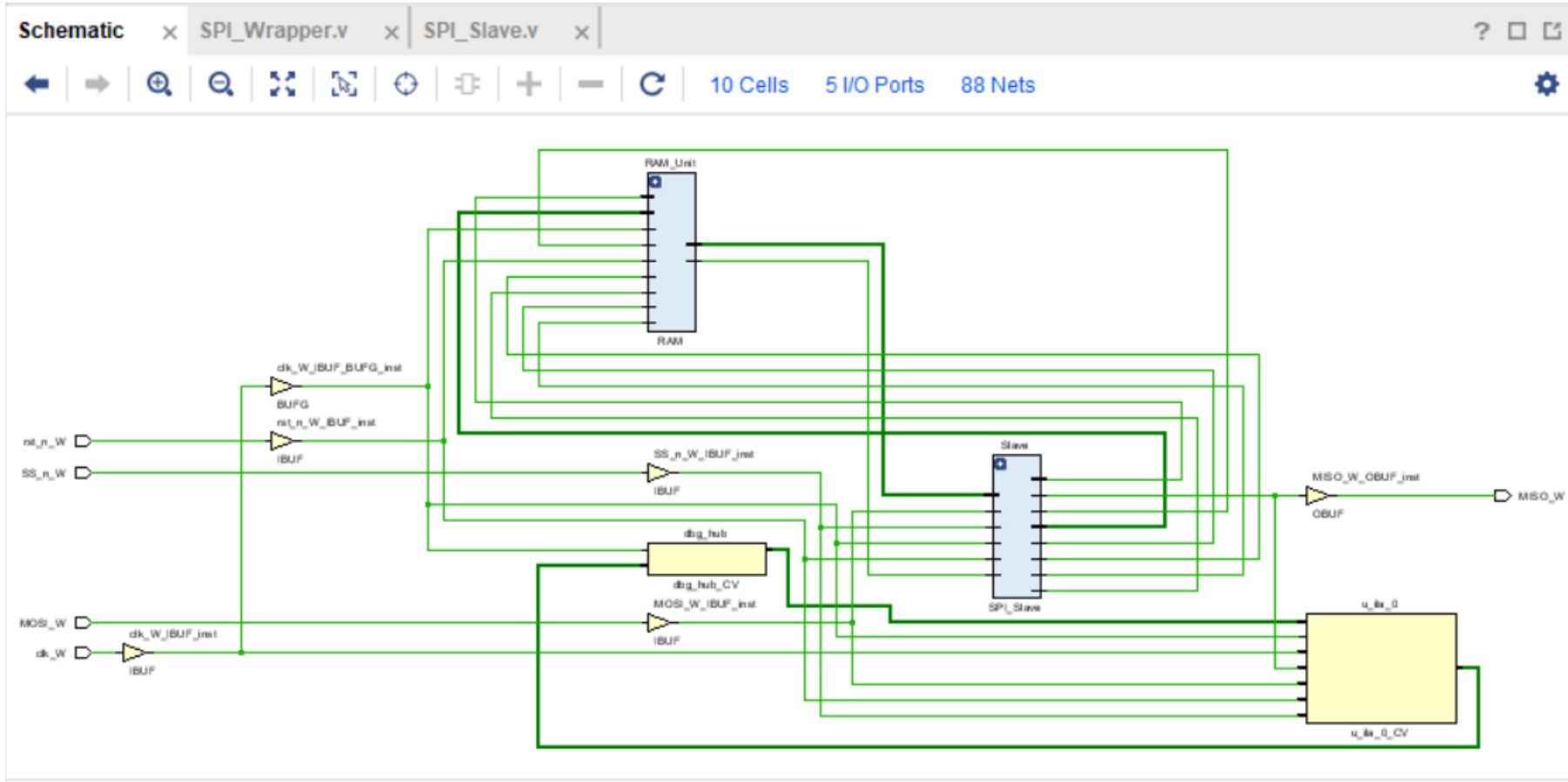


->>Utilization:

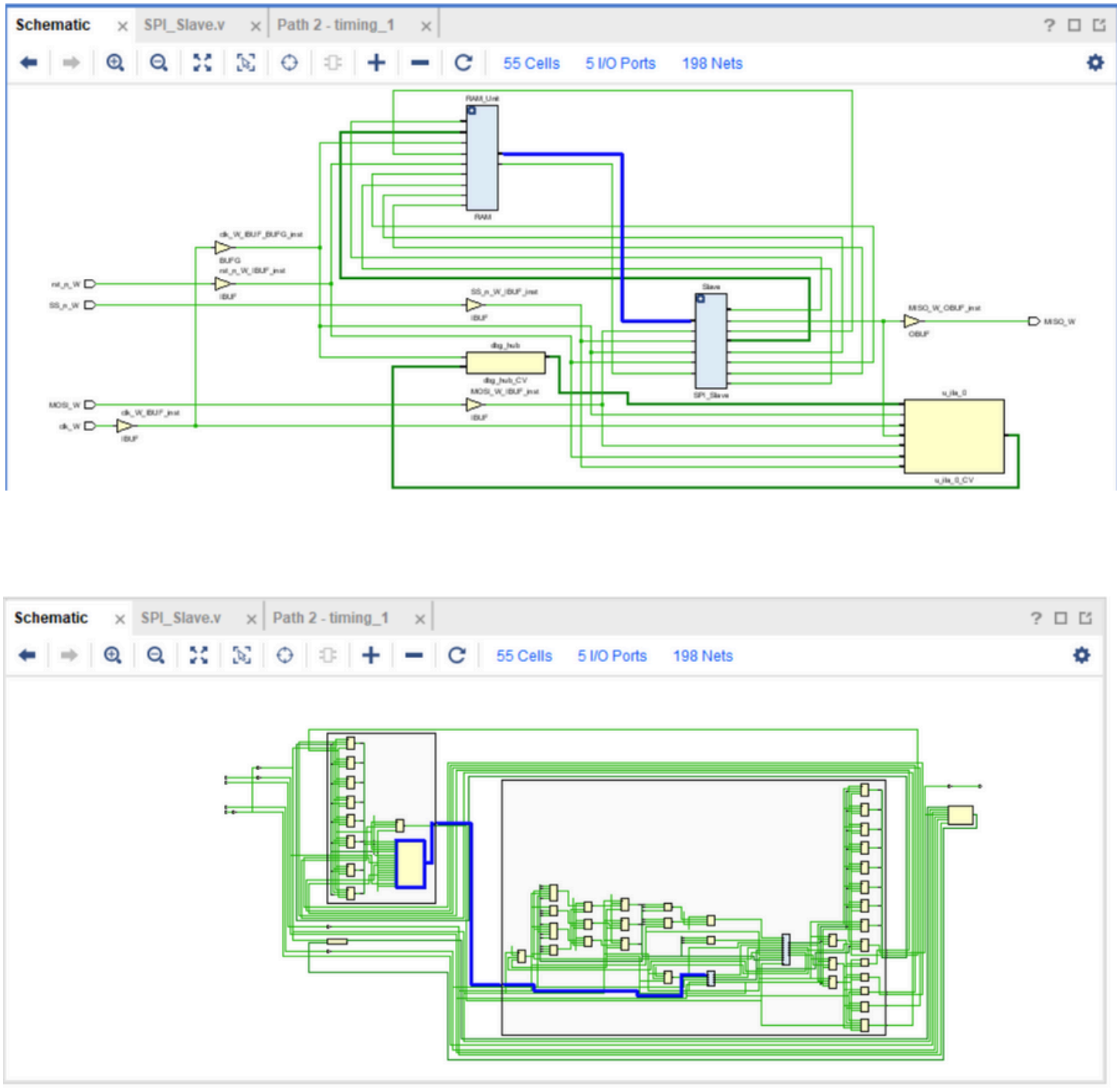


B)One-Hot:

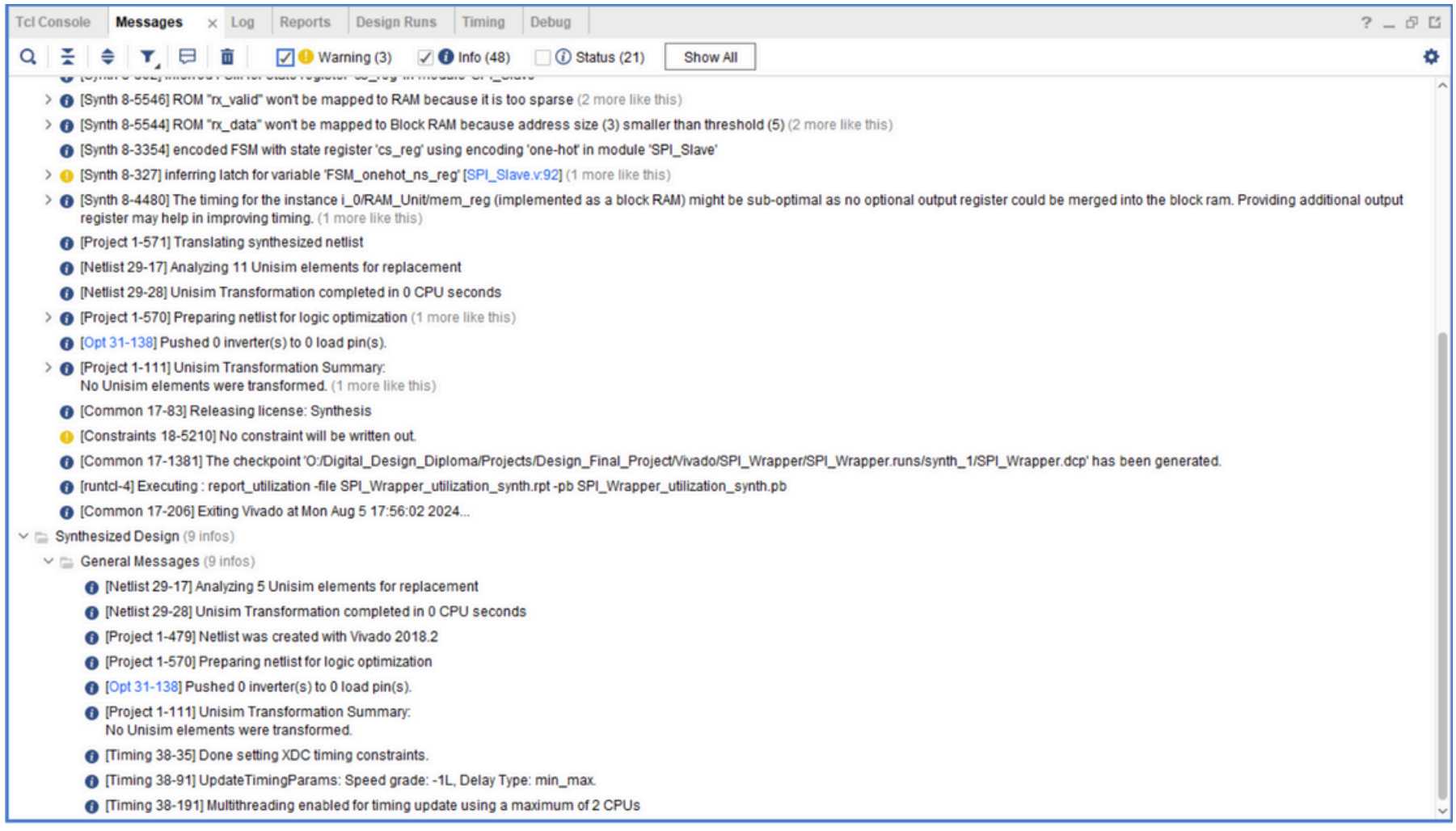
->>Schematic:



->>Critical path:



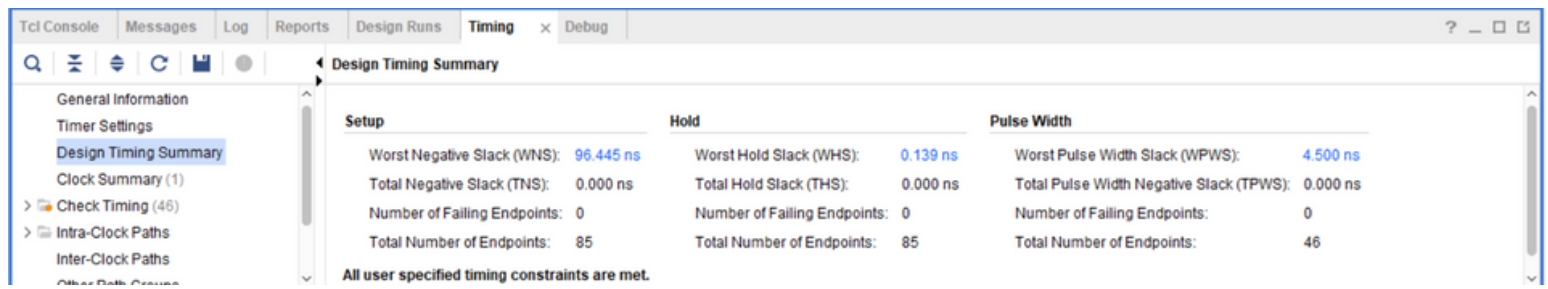
->>Messages:


Tcl Console
Messages
Log
Reports
Design Runs
Timing
Debug
Warning (3)
Info (48)
Status (21)
Show All
[Synth 8-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse (2 more like this)
[Synth 8-5544] ROM "rx_data" won't be mapped to Block RAM because address size (3) smaller than threshold (5) (2 more like this)
[Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
[Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [SPI_Slave.v:92] (1 more like this)
[Synth 8-4480] The timing for the instance i_0/RAM_Unit/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
[Project 1-571] Translating synthesized netlist
[Netlist 29-17] Analyzing 11 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-570] Preparing netlist for logic optimization (1 more like this)
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
[Common 17-83] Releasing license: Synthesis
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/SPI_Wrapper.runs/synth_1/SPI_Wrapper.dcp' has been generated.
[runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
[Common 17-206] Exiting Vivado at Mon Aug 5 17:56:02 2024...
Synthesized Design (9 infos)
General Messages (9 infos)
[Netlist 29-17] Analyzing 5 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
[Timing 38-35] Done setting XDC timing constraints.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

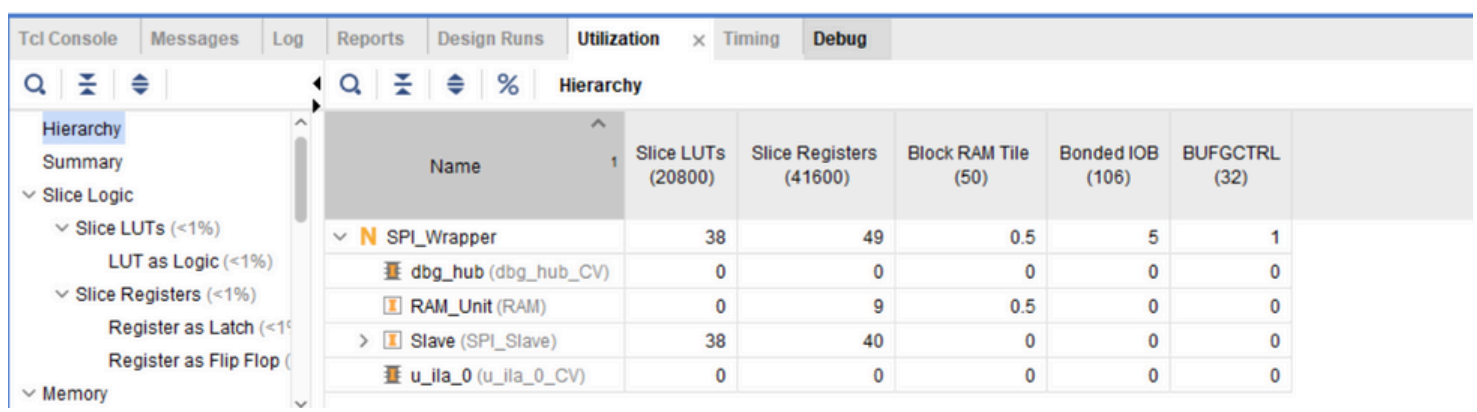
->>Report:

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

->>Timing:

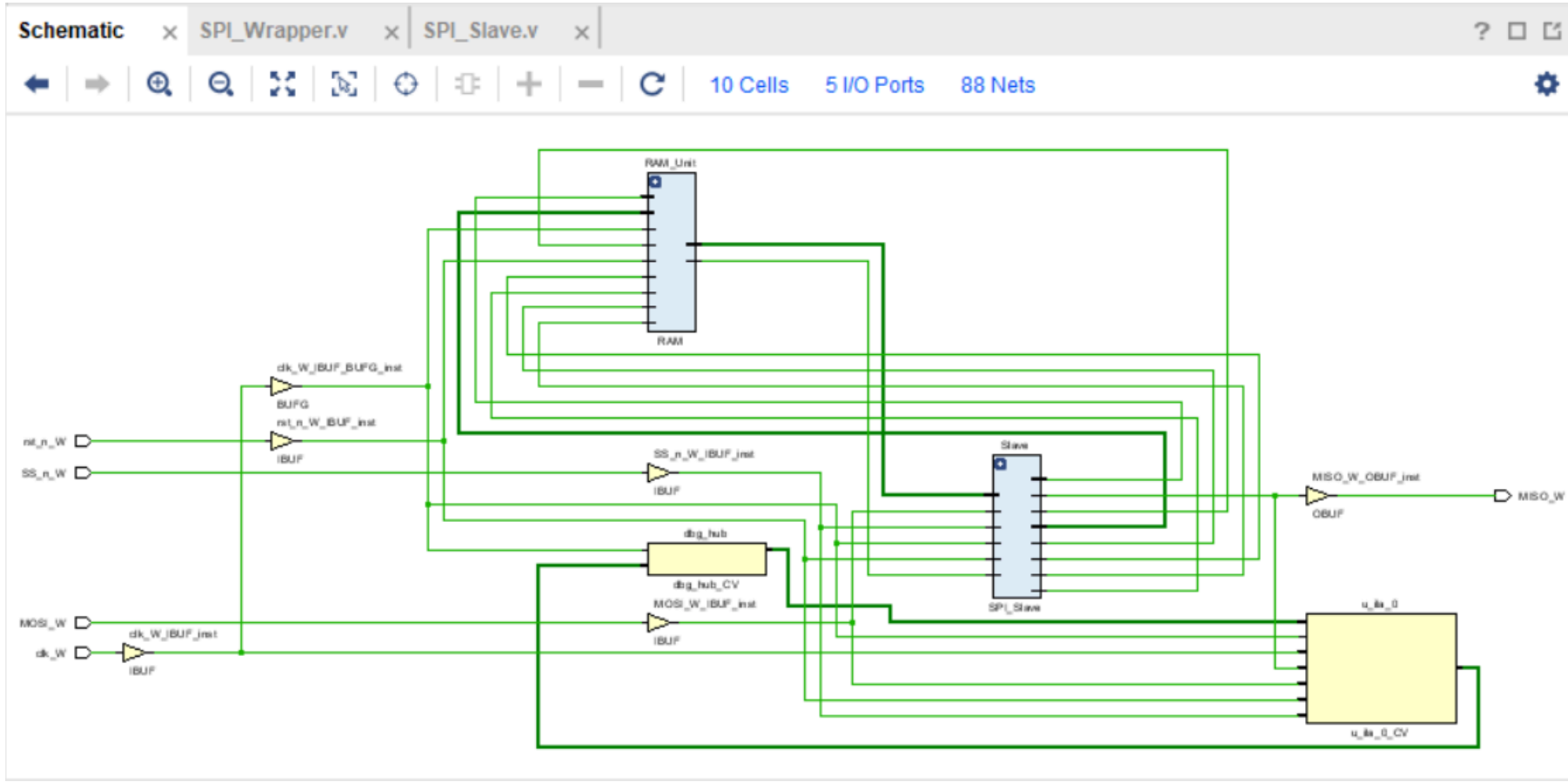


->>Utilization:

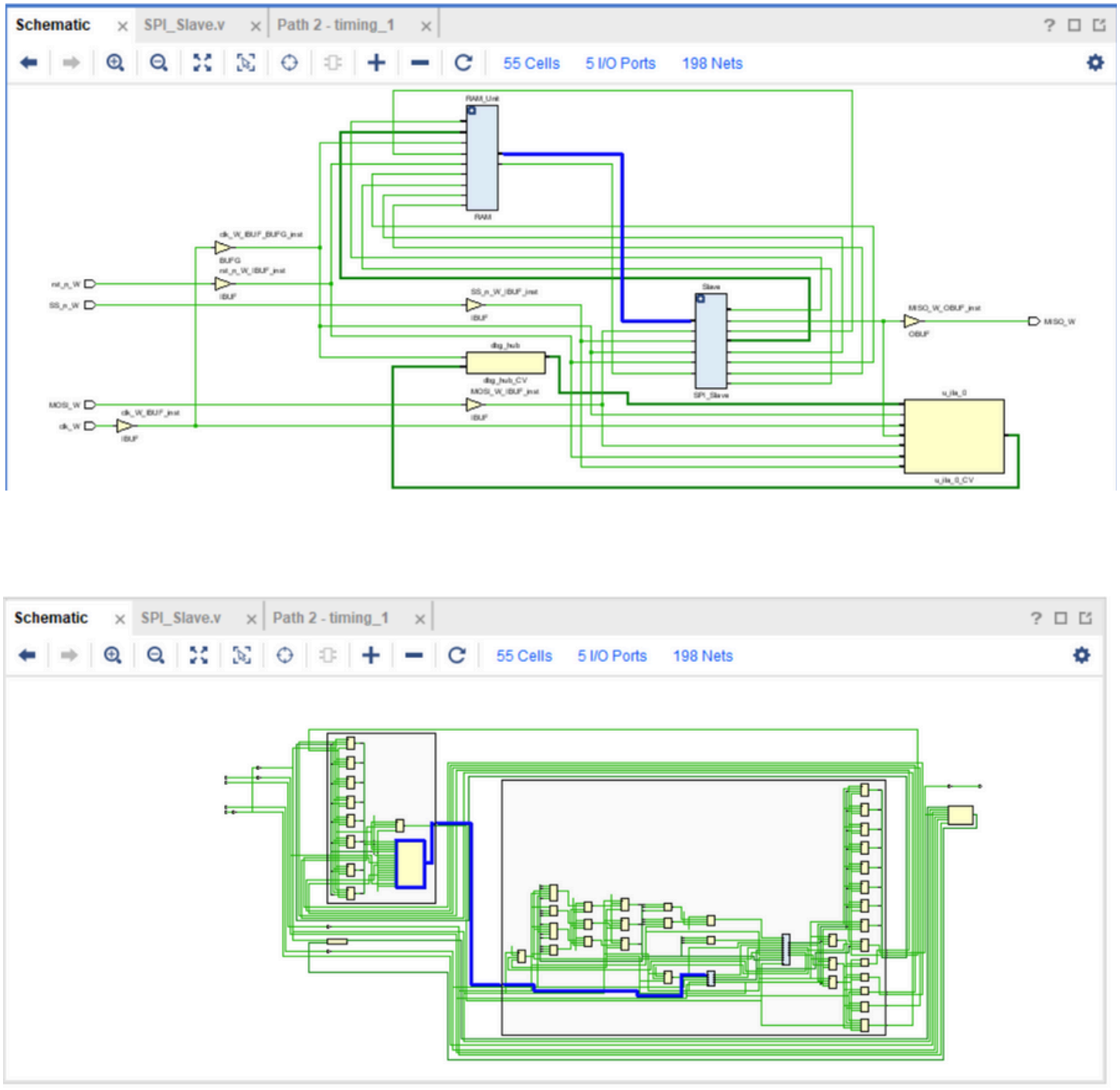


C)Sequential:

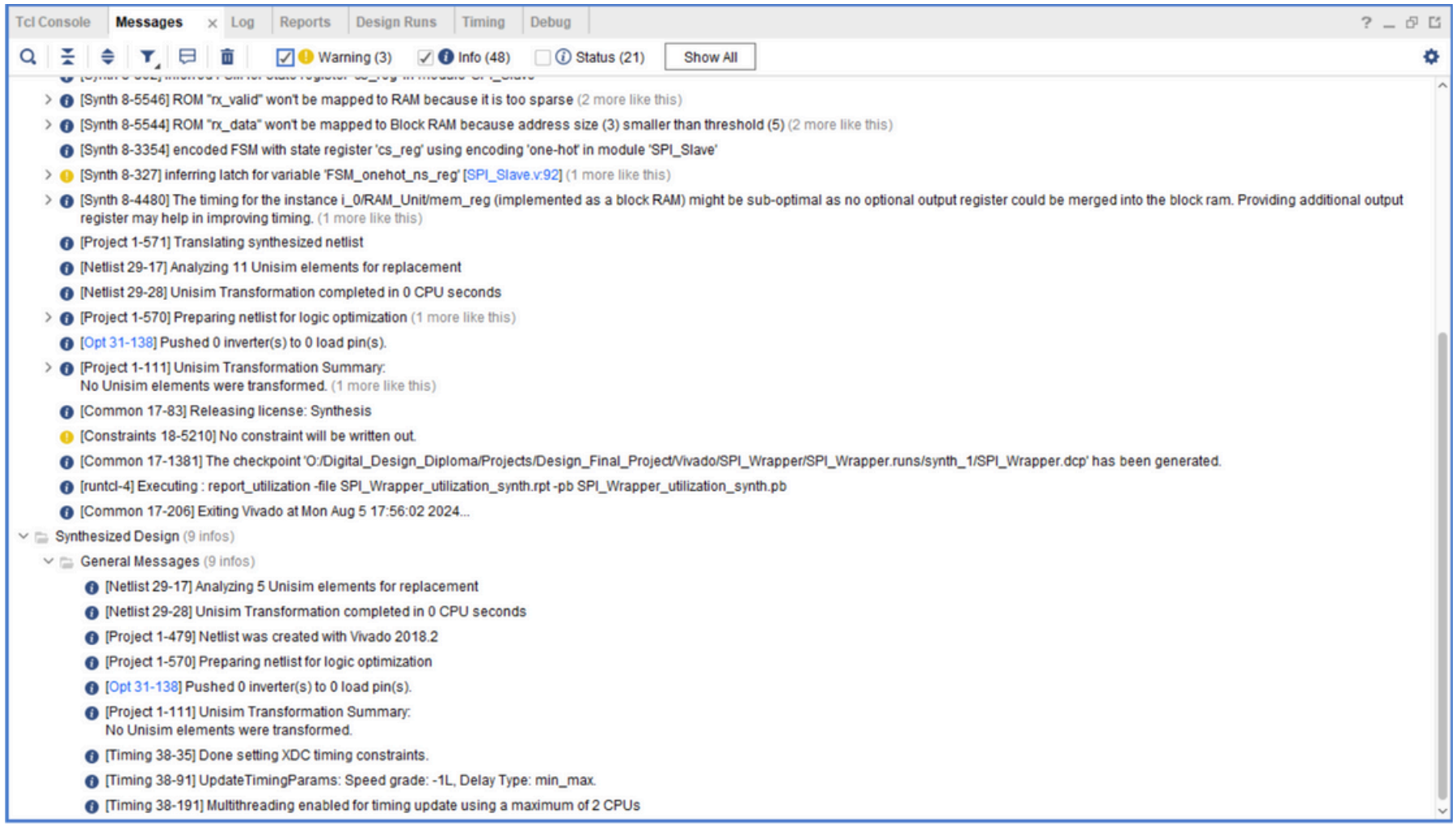
->>Schematic:



->>Critical path:



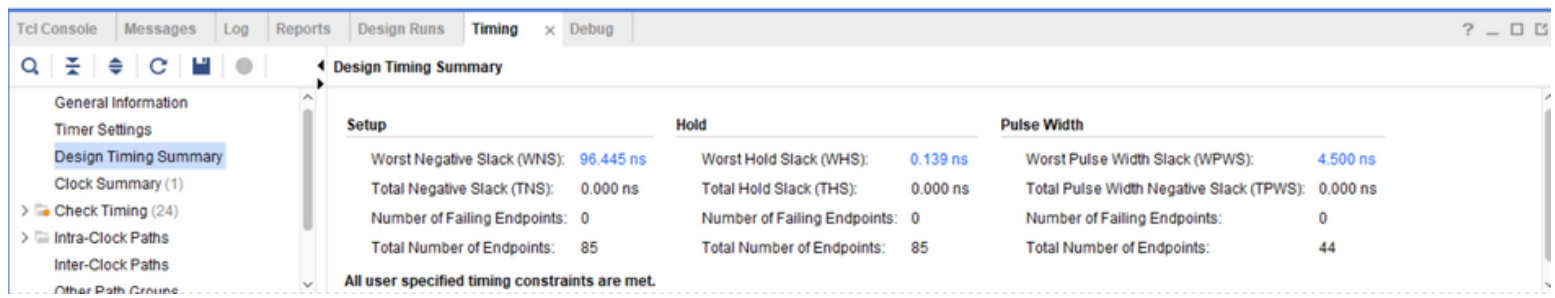
->>Messages:


Tcl Console
Messages
Log
Reports
Design Runs
Timing
Debug
Warning (3)
Info (48)
Status (21)
Show All
[Synth 8-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse (2 more like this)
[Synth 8-5544] ROM "rx_data" won't be mapped to Block RAM because address size (3) smaller than threshold (5) (2 more like this)
[Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
[Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [SPI_Slave.v:92] (1 more like this)
[Synth 8-4480] The timing for the instance i_0/RAM_Unit/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
[Project 1-571] Translating synthesized netlist
[Netlist 29-17] Analyzing 11 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-570] Preparing netlist for logic optimization (1 more like this)
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
[Common 17-83] Releasing license: Synthesis
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/SPI_Wrapper.runs/synth_1/SPI_Wrapper.dcp' has been generated.
[runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
[Common 17-206] Exiting Vivado at Mon Aug 5 17:56:02 2024...
Synthesized Design (9 infos)
General Messages (9 infos)
[Netlist 29-17] Analyzing 5 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
[Timing 38-35] Done setting XDC timing constraints.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

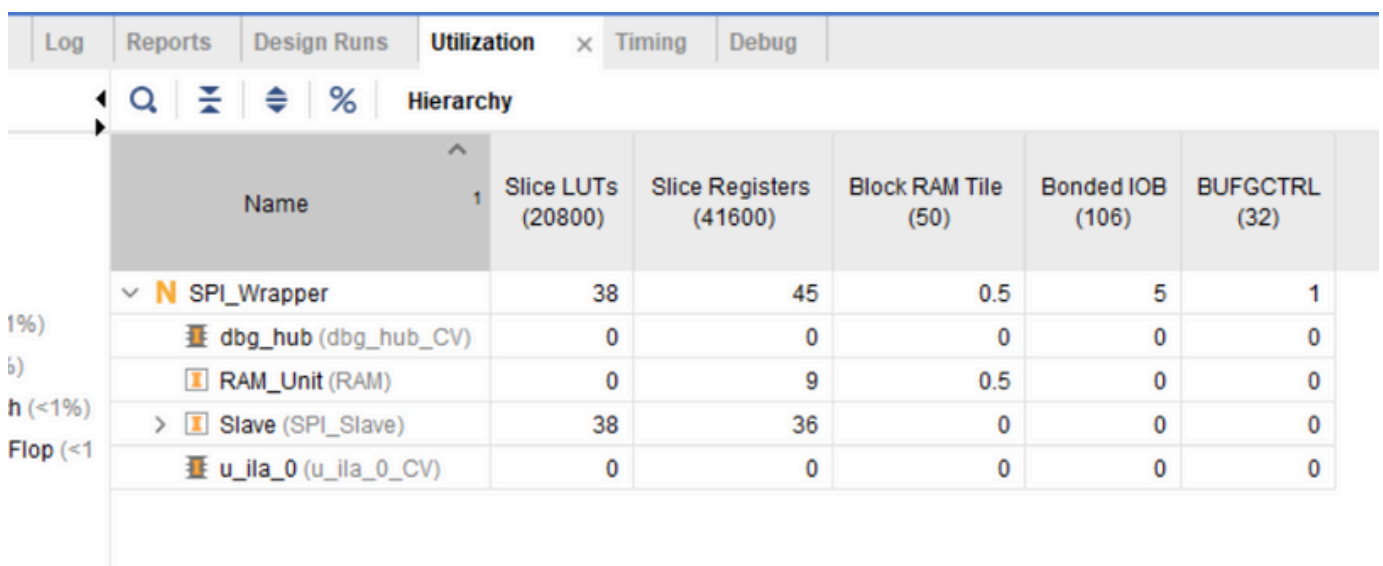
->>Report:

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

->>Timing:



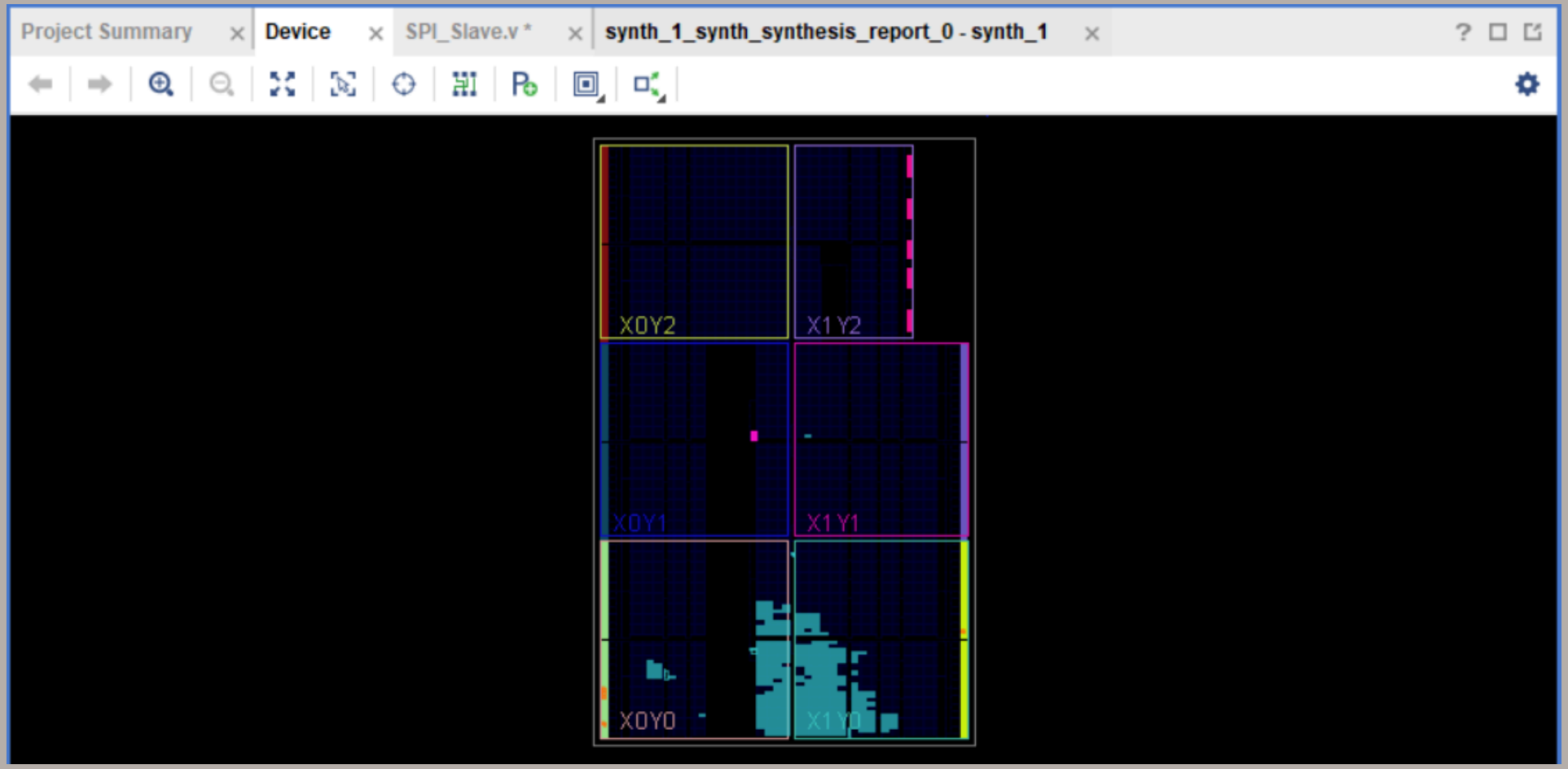
->>Utilization:



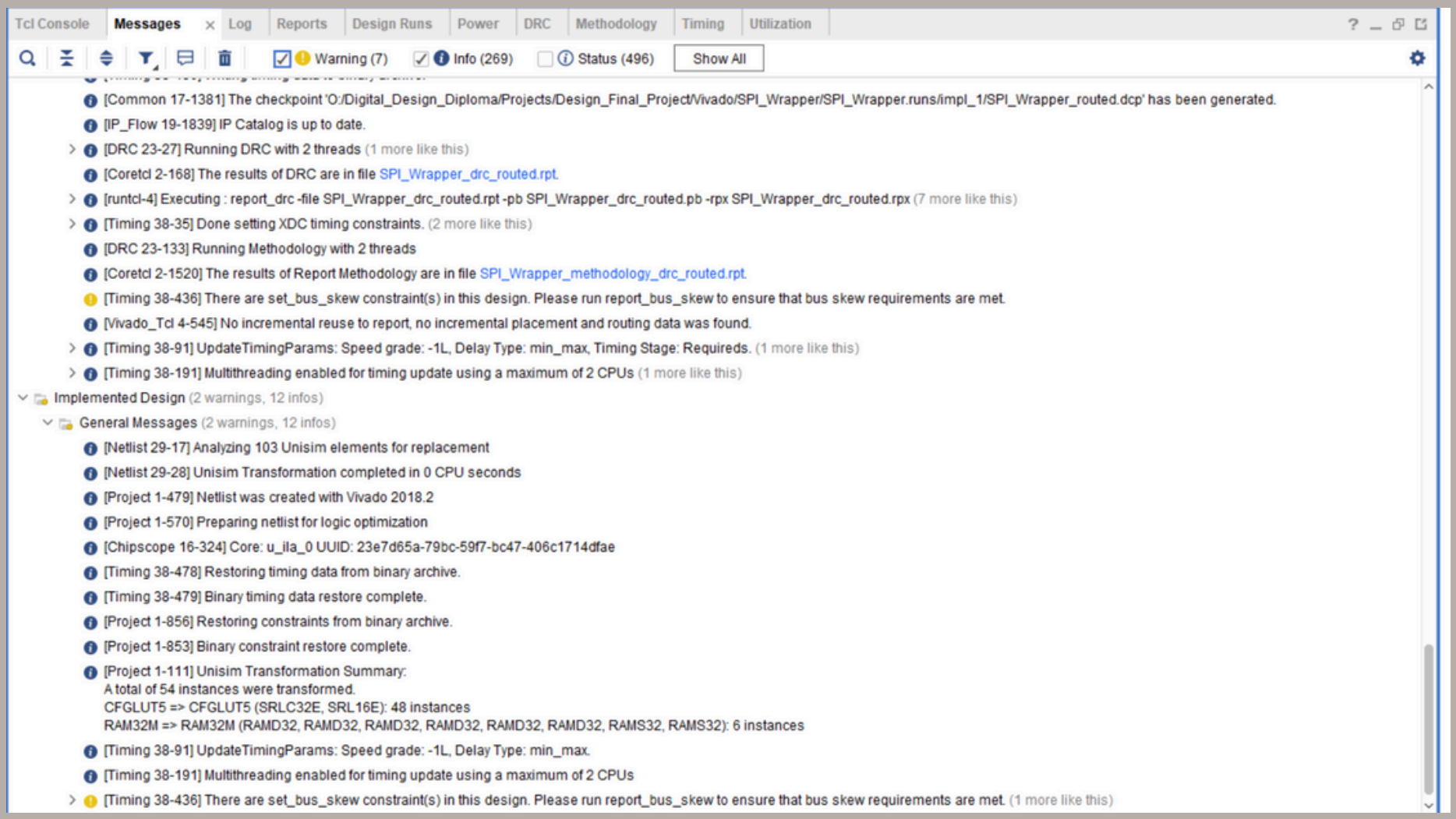
Implementation using vivado

A)Gray Code:

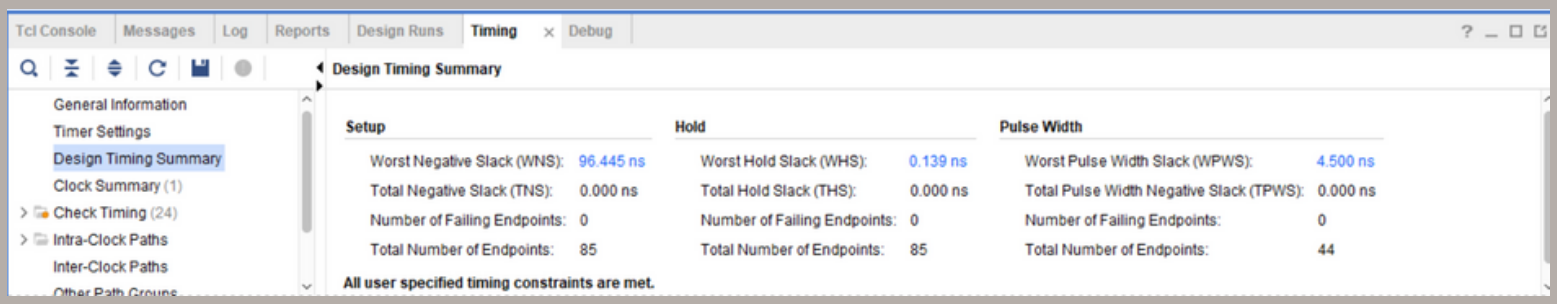
->>Device:



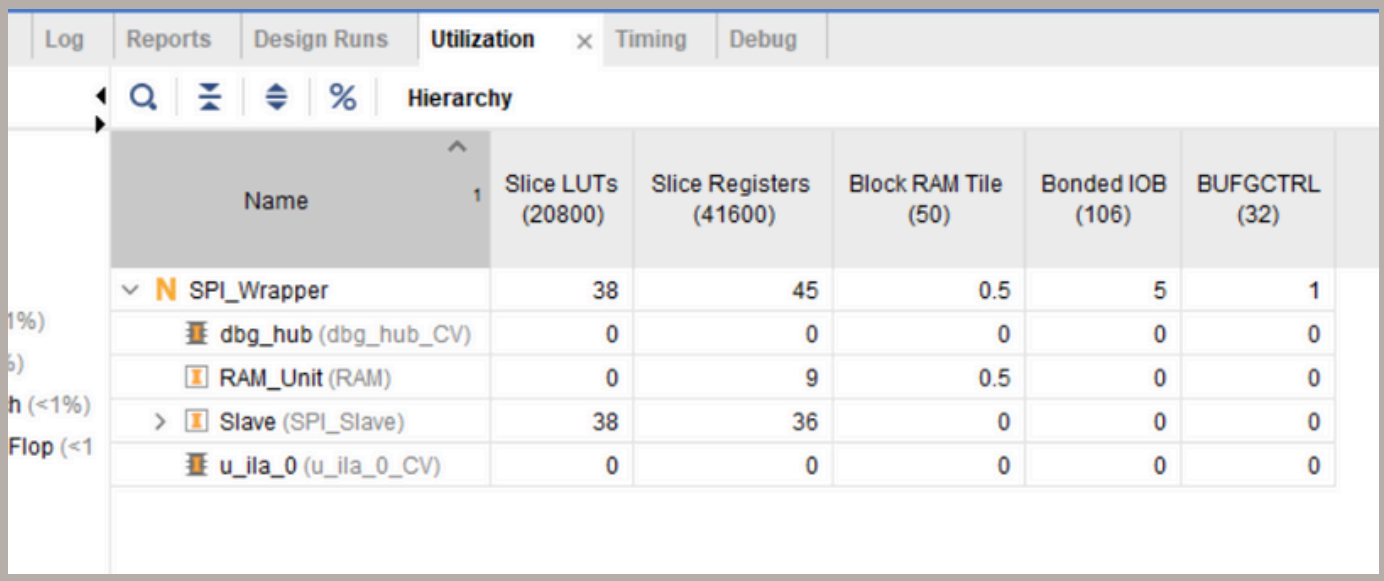
->>Messages:


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Warning (7)
Info (269)
Status (496)
Show All
[Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/SPI_Wrapper.runs/impl_1/SPI_Wrapper_routed.dcp' has been generated.
[IP_Flow 19-1839] IP Catalog is up to date.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file SPI_Wrapper_drc_routed.rpt.
[runtcl-4] Executing : report_drc -file SPI_Wrapper_drc_routed.rpt -pb SPI_Wrapper_drc_routed.pb -rpx SPI_Wrapper_drc_routed.rpx (7 more like this)
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[DRC 23-133] Running Methodology with 2 threads
[Coretcl 2-1520] The results of Report Methodology are in file SPI_Wrapper_methodology_drc_routed.rpt.
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
Implemented Design (2 warnings, 12 infos)
General Messages (2 warnings, 12 infos)
[Netlist 29-17] Analyzing 103 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae
[Timing 38-478] Restoring timing data from binary archive.
[Timing 38-479] Binary timing data restore complete.
[Project 1-856] Restoring constraints from binary archive.
[Project 1-853] Binary constraint restore complete.
[Project 1-111] Unisim Transformation Summary:
A total of 54 instances were transformed.
CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 48 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met. (1 more like this)

->>Timing:

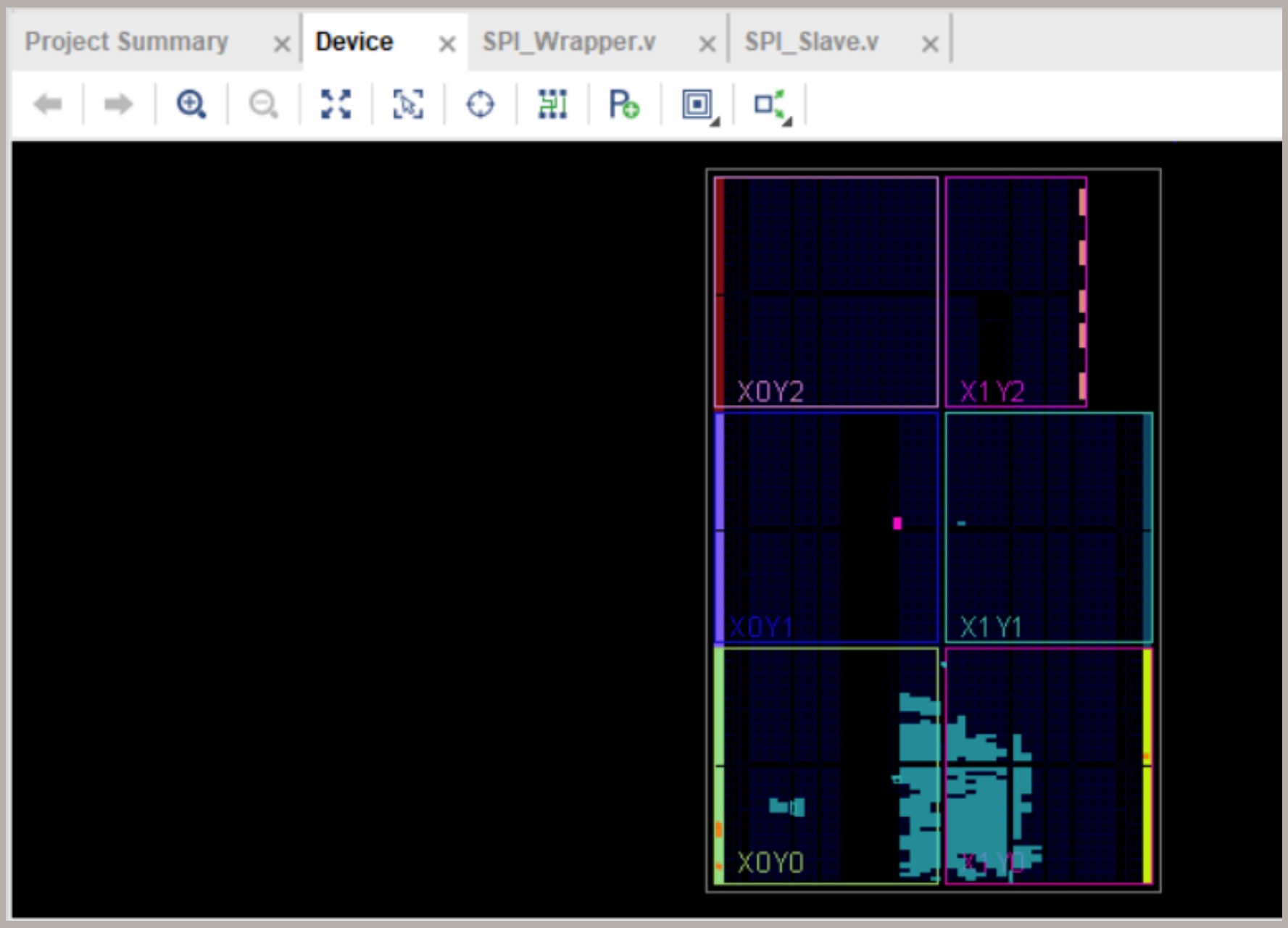


->>Utilization:

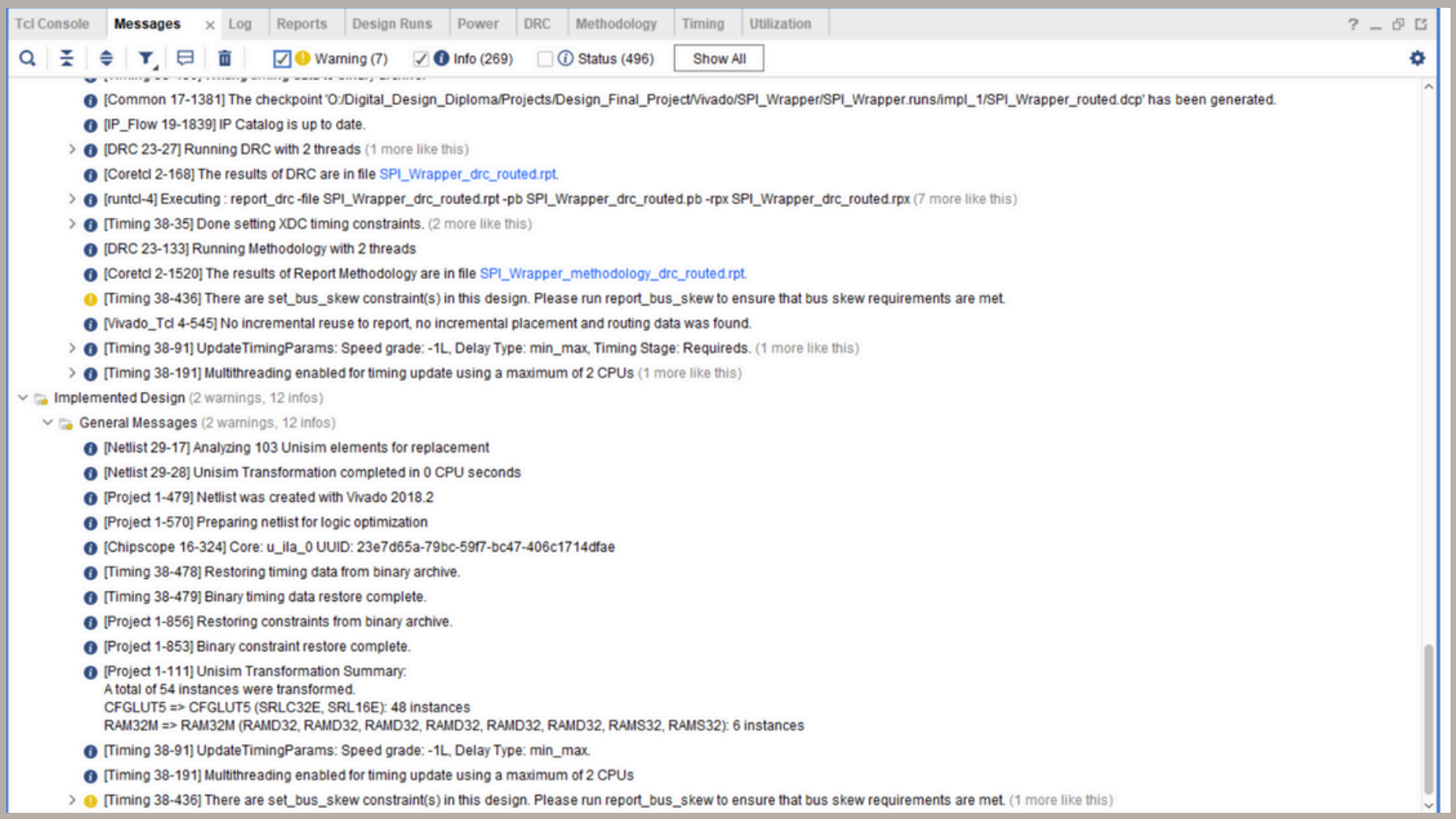


B)One-Hot:

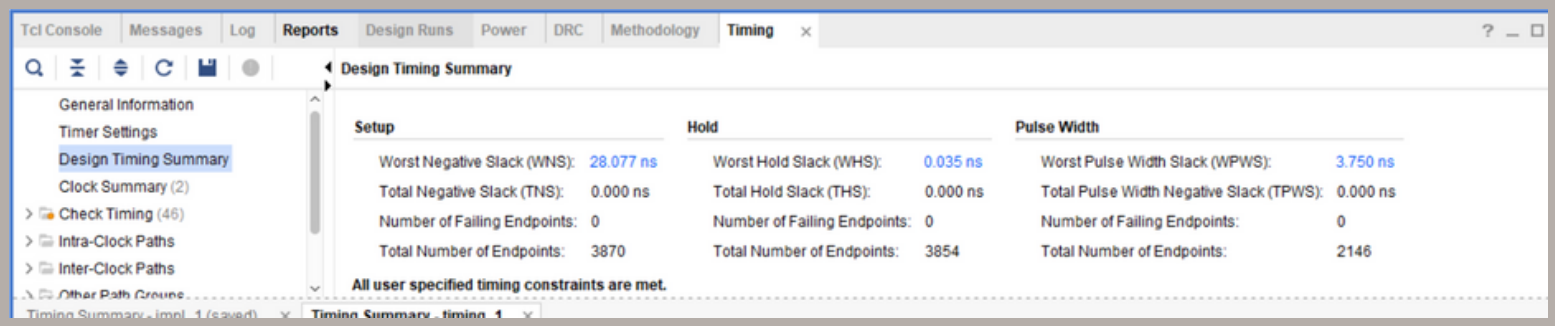
->>Device:



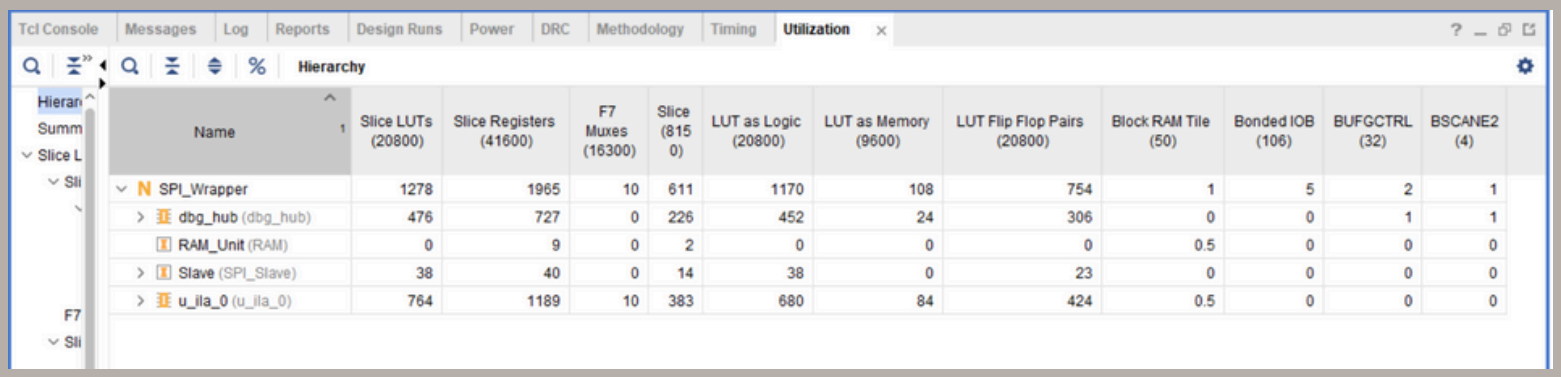
->>Messages:


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Warning (7)
Info (269)
Status (496)
Show All
[Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/SPI_Wrapper.runs/impl_1/SPI_Wrapper_routed.dcp' has been generated.
[IP_Flow 19-1839] IP Catalog is up to date.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file SPI_Wrapper_drc_routed.rpt.
[runtcl-4] Executing : report_drc -file SPI_Wrapper_drc_routed.rpt -pb SPI_Wrapper_drc_routed.pb -rpx SPI_Wrapper_drc_routed.rpx (7 more like this)
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[DRC 23-133] Running Methodology with 2 threads
[Coretcl 2-1520] The results of Report Methodology are in file SPI_Wrapper_methodology_drc_routed.rpt.
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
Implemented Design (2 warnings, 12 infos)
General Messages (2 warnings, 12 infos)
[Netlist 29-17] Analyzing 103 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae
[Timing 38-478] Restoring timing data from binary archive.
[Timing 38-479] Binary timing data restore complete.
[Project 1-856] Restoring constraints from binary archive.
[Project 1-853] Binary constraint restore complete.
[Project 1-111] Unisim Transformation Summary:
A total of 54 instances were transformed.
CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 48 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met. (1 more like this)

->>Timing:

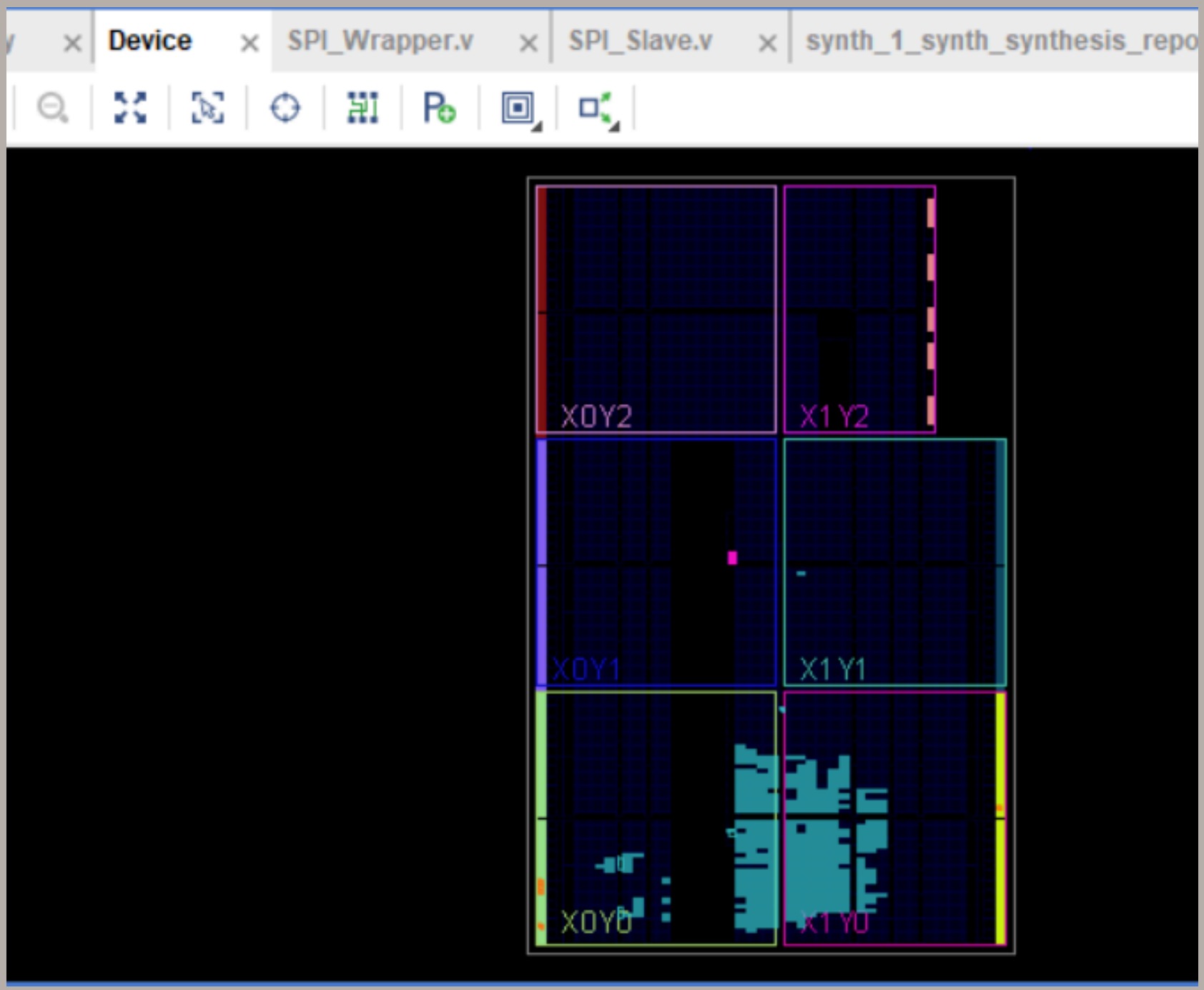


->>Utilization:

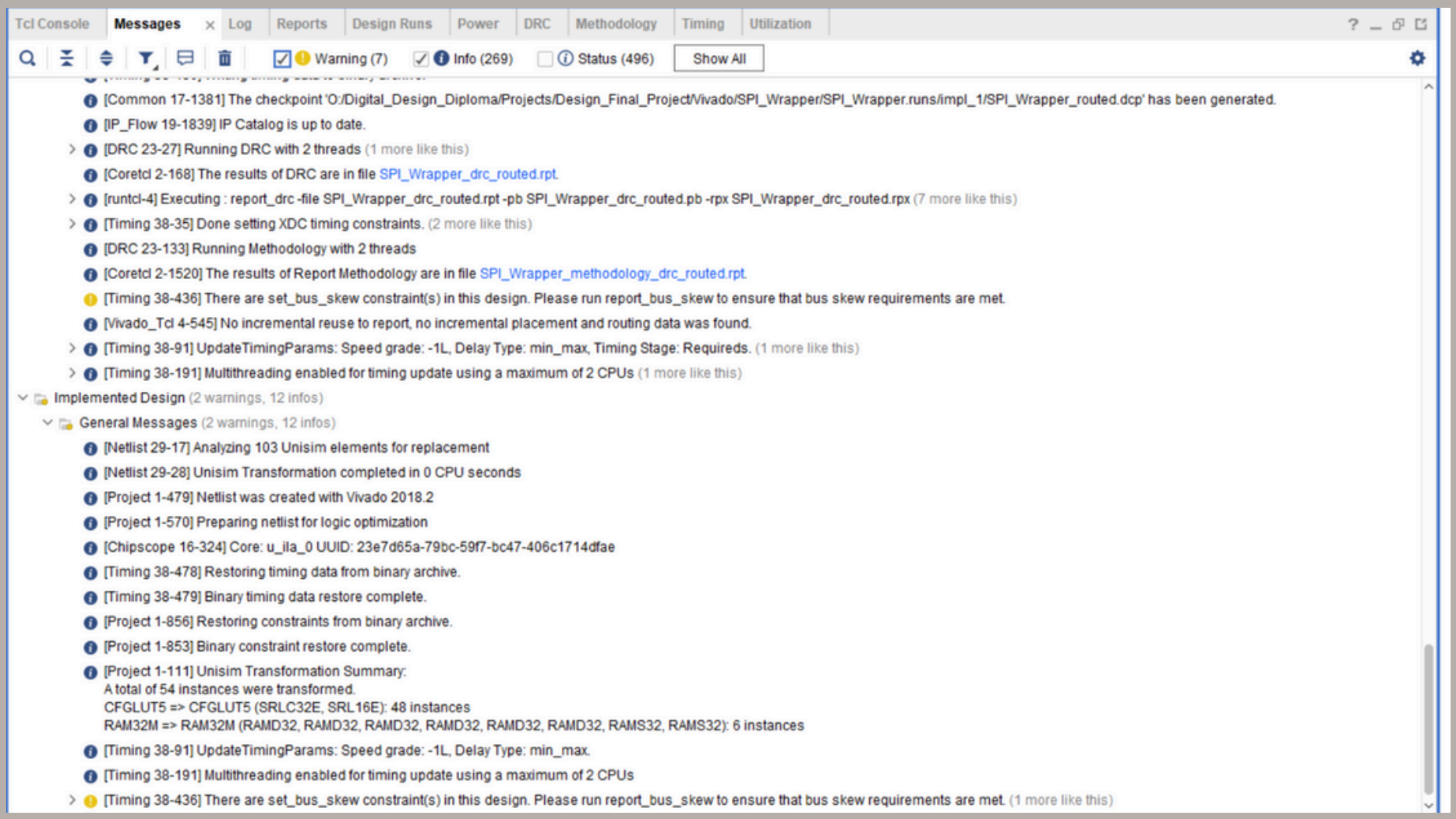


C)Sequential:

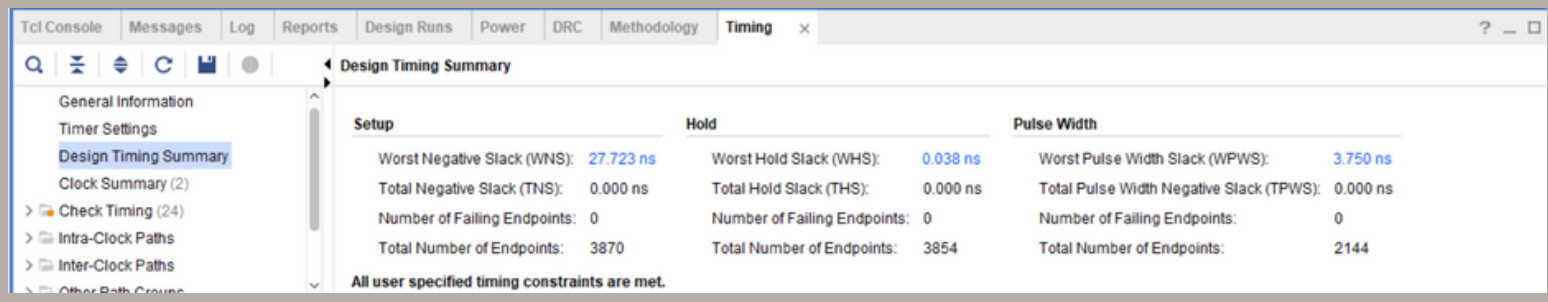
->>Device:



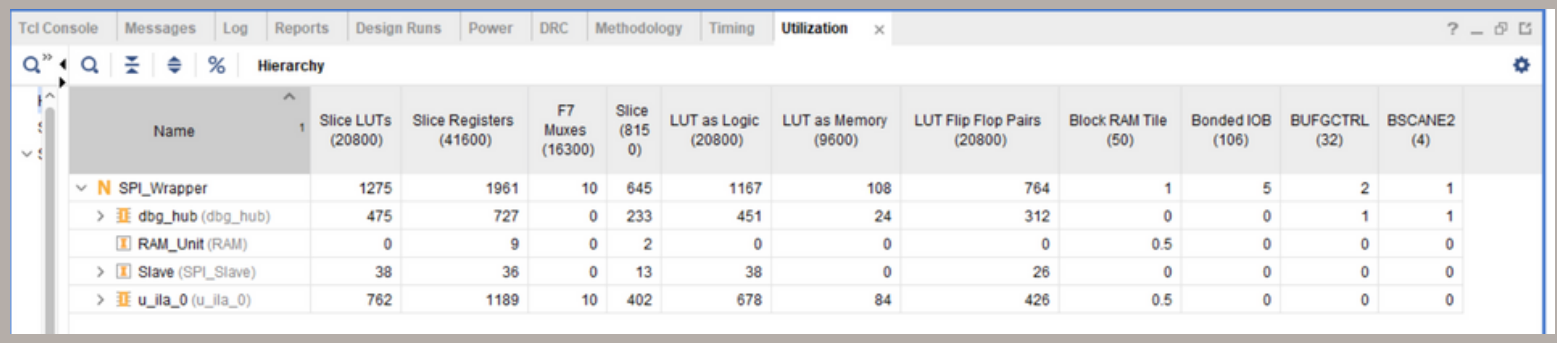
->>Messages:


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Warning (7)
Info (269)
Status (496)
Show All
[Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Design_Final_Project/Vivado/SPI_Wrapper/SPI_Wrapper.runs/impl_1/SPI_Wrapper_routed.dcp' has been generated.
[IP_Flow 19-1839] IP Catalog is up to date.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file SPI_Wrapper_drc_routed.rpt.
[runtcl-4] Executing : report_drc -file SPI_Wrapper_drc_routed.rpt -pb SPI_Wrapper_drc_routed.pb -rpx SPI_Wrapper_drc_routed.rpx (7 more like this)
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[DRC 23-133] Running Methodology with 2 threads
[Coretcl 2-1520] The results of Report Methodology are in file SPI_Wrapper_methodology_drc_routed.rpt.
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
Implemented Design (2 warnings, 12 infos)
General Messages (2 warnings, 12 infos)
[Netlist 29-17] Analyzing 103 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae
[Timing 38-478] Restoring timing data from binary archive.
[Timing 38-479] Binary timing data restore complete.
[Project 1-856] Restoring constraints from binary archive.
[Project 1-853] Binary constraint restore complete.
[Project 1-111] Unisim Transformation Summary:
A total of 54 instances were transformed.
CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 48 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met. (1 more like this)

->>Timing:



->>Utilization:



Conclusion

From the timing reports of synthesis and implementation above, we can decide that using “gray” encoding is much better with respect to frequency

Constraints file

Vivado > SPI_Wrapper > Constraints_basys3.xdc

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk_W]
create_clock -add -name sys_clk_pin -period 100.00 -waveform {0 5} [get_ports clk_W]


## Switches
set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {MOSI_W}]
set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {SS_n_W}]
set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {rst_n_W}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {A_N[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {B_N[0]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {B_N[1]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {B_N[2]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {B_N[3]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {Opcode_N[0]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {Opcode_N[1]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {MISO_W}]
#set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {out[1]}]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {out[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {out[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {out[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {out[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {out[6]}]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {out[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
```

Thank You