ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

# Final project

## FFT 8-Points Radix-2

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# Agenda

- Breif about FFT 8-points Radix-2 arch.
- System modeling.
- RTL design.
- Verification.
- ASIC implementation and results.
- FPGA implementation and results.

# Breif about FFT 8-points Radix-2 arch.

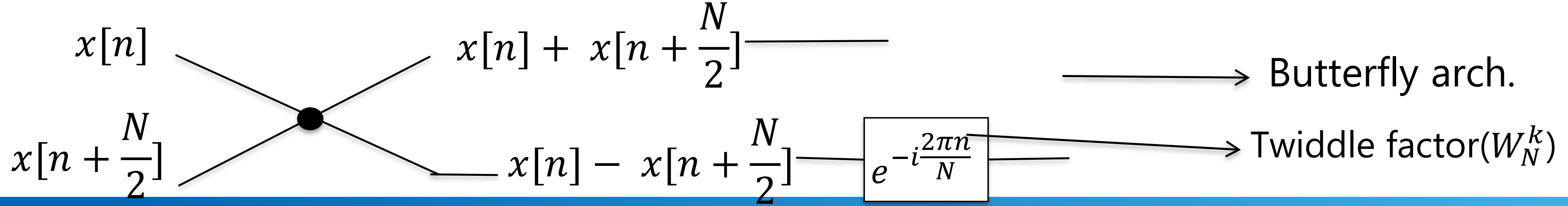
- FFT importance:
  - Can be used to obtain the frequency domain view of signals which gives a different point of view and carries information don't present in time domain.
  - In modern DSP applications (e.g. DSP IP for OFDM Modulators/Demodulators , Range–Doppler Processing, & Audio codecs with noise reduction).
- DFT equation:

$$\tilde{x}[k] = \sum_{n=0}^{N-1} x[n]\, e^{-i\frac{2\pi kn}{N}} \,, k = 0, 1, 2, \dots, N-1 \xrightarrow{\qquad} O(N^2)$$

- FFT equation:

$$\tilde{x}[k] = DFT_{N/2}[x_1[n]] + DFT_{N/2}[x_2[n]]e^{-i\frac{2\pi n}{N}} \,, k = 0, 1, 2, \dots, N-1. \xrightarrow{\qquad} O(\frac{N}{2}\log N)$$

$$x_1[n] = x[n] + x[n+\frac{N}{2}] \; \& \; x_2[n] = x[n] - x[n+\frac{N}{2}]$$



$x[n]$

$x[n+\frac{N}{2}]$

$x[n] + x[n+\frac{N}{2}]$

$x[n] - x[n+\frac{N}{2}]$

$e^{-i\frac{2\pi n}{N}}$

Butterfly arch.

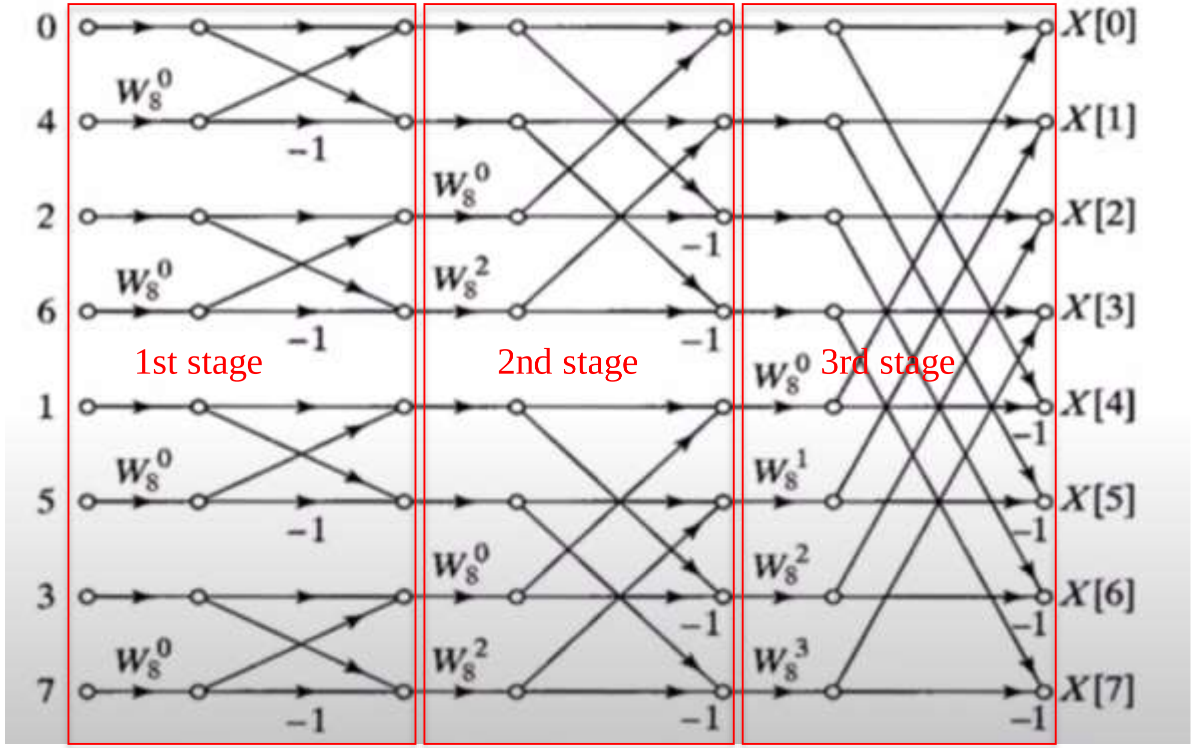
Twiddle factor($W_N^k$)

# Breif about FFT 8-points Radix-2 arch. cont.

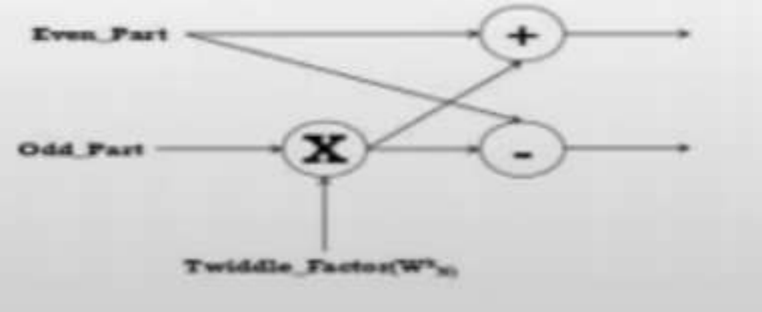
- The used arch. in our RTL can be obtained by expanding the FFT equation for 8-point (8 samples) case and simplify it to be implemented using 2-point blocks. Therefore:

$$\#stages \ = \log_2 8 \ = \ 3 \ stages$$

- Finally, the arch. is:



- Basic building block is **MAC block**:

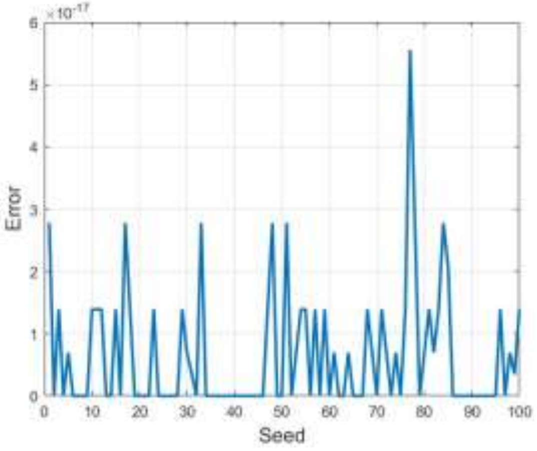


- Required twiddle factors are only: $W_8^0, W_8^1, W_8^2, and\ W_8^3$
- We have two forms:
  - Decimation In Time(DIT):Input is bit-reversed, output is normal order. → 0 | 0, 2 | 0,1,2,3
  - Decimation In Freq.(DIF):Input is normal order, output is bit-reversed. → 0,1,2,3 | 0, 2 | 0

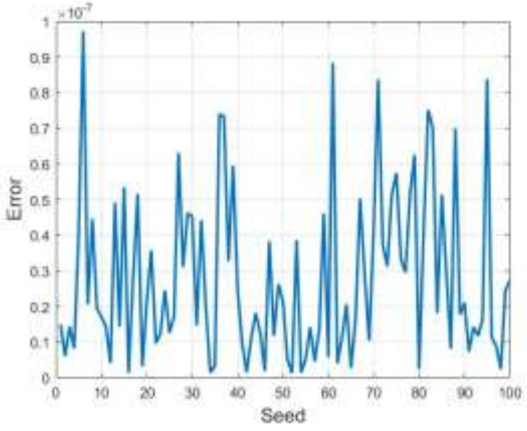
# System modeling

- First write down the chosen architecture exactly similar to signal flow graph. Isolate core algorithm.
- Run double, single, & fixed-point analysis succesively such that in each case calculate the error and do instrumentation. Run is done for 100 seed and assumed to have real inputs only.
- During the double case run, from its instrumentation results extract the integer bit width required for each signal in the flow graph.
- With respect to the twiddle factor: It's assumed to have 2 integer bits.
- Error for double and single runs:
  - double ~ $10^{-17}$
  - single ~ $10^{-7}$

| signal ID | Integer bit width |
|---|---|
| First_INxx_* | 4 |
| First_Multi_OUTx_* | 1 |
| First_OUTx0_* | 2 |
| First_OUTx1_* | 1 |
| Second_Multi_OUT(0,2) | 2 |
| Second_Multi_OUT(1,3) | 1 |
| Second_OUT(00,20) | 3 |
| Second_OUT(01,21) | 2 |
| Second_OUT(10,11,30,31) | 1 |
| Third_Multi_OUT0 | 3 |
| Third_Multi_OUT(1,2,3) | 2 |
| Third_OUTxx_* | 4 |



double

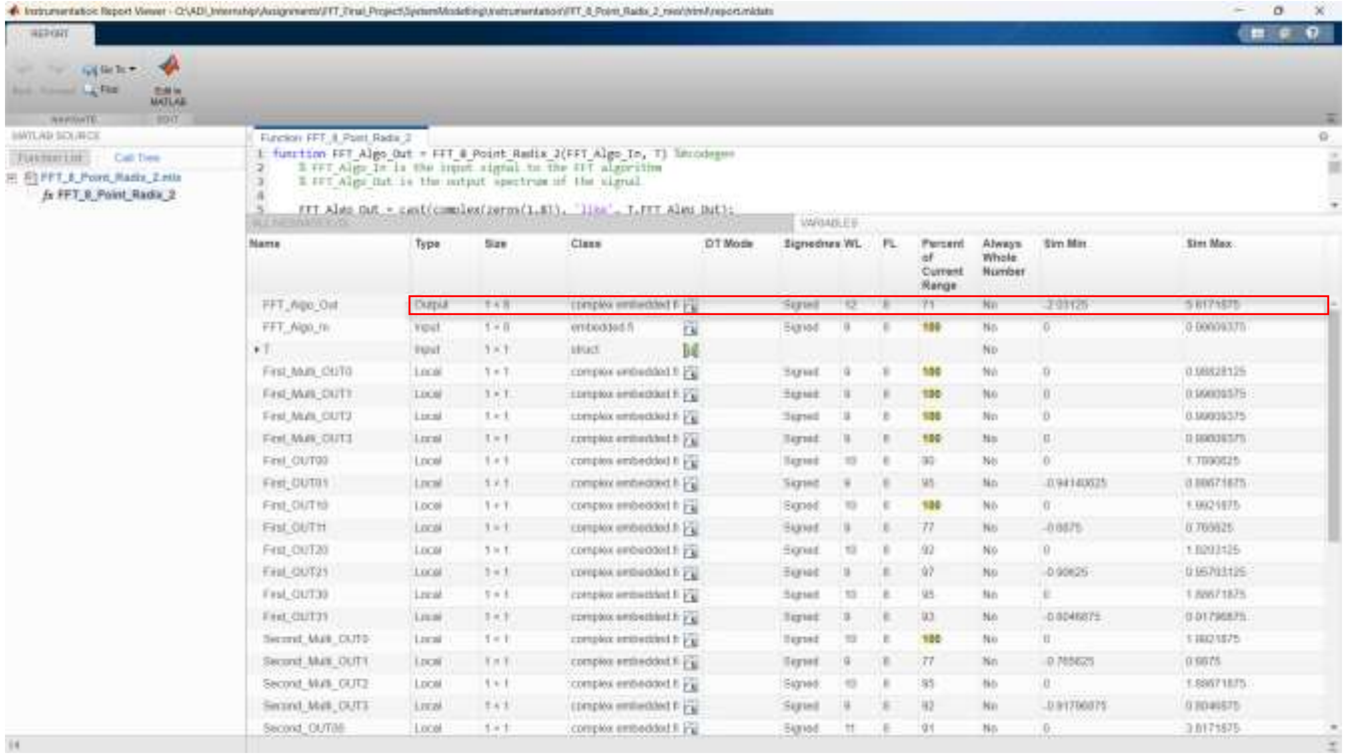


single

# System modeling cont.

- In order to determine the fractional bit width, plot the SQNR vs the fractional bit width:
  - Choose SQNR = 53.4616 dB @ unified fractional bit width for all signals equals 8 bits.
  - Therefore the widest signals in the flow graph are the output signals with width = 4 + 8 = 12 bits.
- Now run the first step in the case of fixed-point after adding the chosen fractional bit width to observe any unwanted difference.

- Error for fixed-point case with 8-bits fractional bit width ~$10^{-3}$
- Fixed-point instrumentation results:

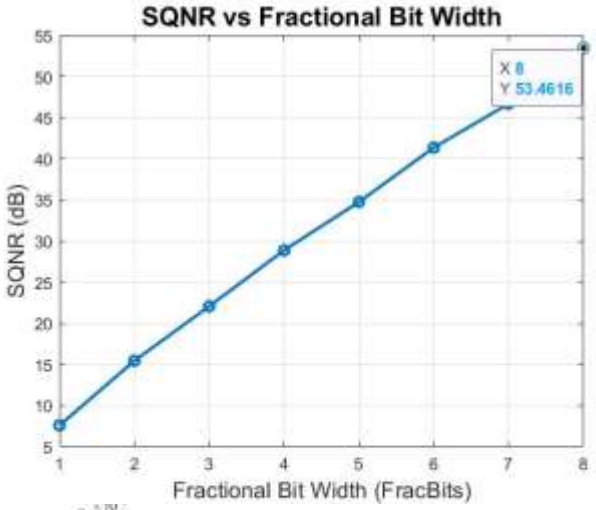


Instrumentation Report Viewer - C:\ADI_Internship\Assignments\FFT_Final_Project\SystemModeling\instrumentation\FFT_8_Point_Radix_2_mex\html\report.mldatx

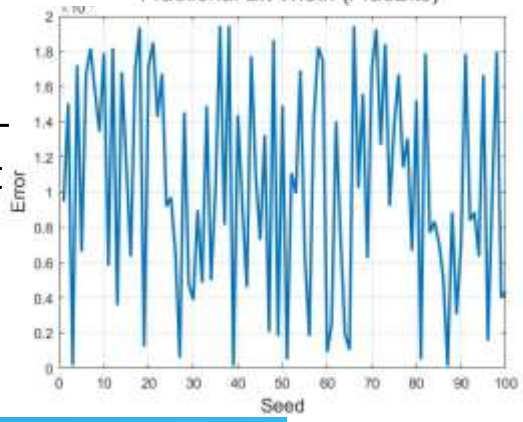
```
function FFT_Algo_Out = FFT_8_Point_Radix_2(FFT_Algo_In, T) %#codegen
    % FFT_Algo_In is the input signal to the FFT algorithm
    % FFT_Algo_Out is the output spectrum of the signal

    FFT_Algo_Out = cast(complex(zeros(1,8)), 'like', T.FFT_Algo_Out);
```

| Name | Type | Size | Class | DT Mode | Signedness | WL | FL | Percent of Current Range | Always Whole Number | Sim Min | Sim Max |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FFT_Algo_Out | Output | 1 × 8 | complex embedded.fi |  | Signed | 12 | 8 | 71 | No | -2.03125 | 5.8171875 |
| FFT_Algo_In | Input | 1 × 8 | embedded.fi |  | Signed | 9 | 8 | 100 | No | 0 | 0.99609375 |
| T | Input | 1 × 1 | struct |  |  |  |  |  | No |  |  |
| First_Mult_OUT0 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 100 | No | 0 | 0.98828125 |
| First_Mult_OUT1 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 100 | No | 0 | 0.99609375 |
| First_Mult_OUT2 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 100 | No | 0 | 0.99609375 |
| First_Mult_OUT3 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 100 | No | 0 | 0.99609375 |
| First_OUT00 | Local | 1 × 1 | complex embedded.fi |  | Signed | 10 | 8 | 90 | No | 0 | 1.7890625 |
| First_OUT01 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 95 | No | -0.94140625 | 0.98671875 |
| First_OUT10 | Local | 1 × 1 | complex embedded.fi |  | Signed | 10 | 8 | 100 | No | 0 | 1.9921875 |
| First_OUT11 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 77 | No | -0.6875 | 0.765625 |
| First_OUT20 | Local | 1 × 1 | complex embedded.fi |  | Signed | 10 | 8 | 92 | No | 0 | 1.8203125 |
| First_OUT21 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 97 | No | -0.90625 | 0.95703125 |
| First_OUT30 | Local | 1 × 1 | complex embedded.fi |  | Signed | 10 | 8 | 95 | No | 0 | 1.88671875 |
| First_OUT31 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 93 | No | -0.8046875 | 0.91796875 |
| Second_Mult_OUT0 | Local | 1 × 1 | complex embedded.fi |  | Signed | 10 | 8 | 100 | No | 0 | 1.9921875 |
| Second_Mult_OUT1 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 77 | No | -0.765625 | 0.6875 |
| Second_Mult_OUT2 | Local | 1 × 1 | complex embedded.fi |  | Signed | 10 | 8 | 95 | No | 0 | 1.88671875 |
| Second_Mult_OUT3 | Local | 1 × 1 | complex embedded.fi |  | Signed | 9 | 8 | 92 | No | -0.91796875 | 0.8046875 |
| Second_OUT00 | Local | 1 × 1 | complex embedded.fi |  | Signed | 11 | 8 | 91 | No | 0 | 3.8171875 |



Fixed-point error



# RTL design

- Design architecture: Serial-IN-Serial-OUT

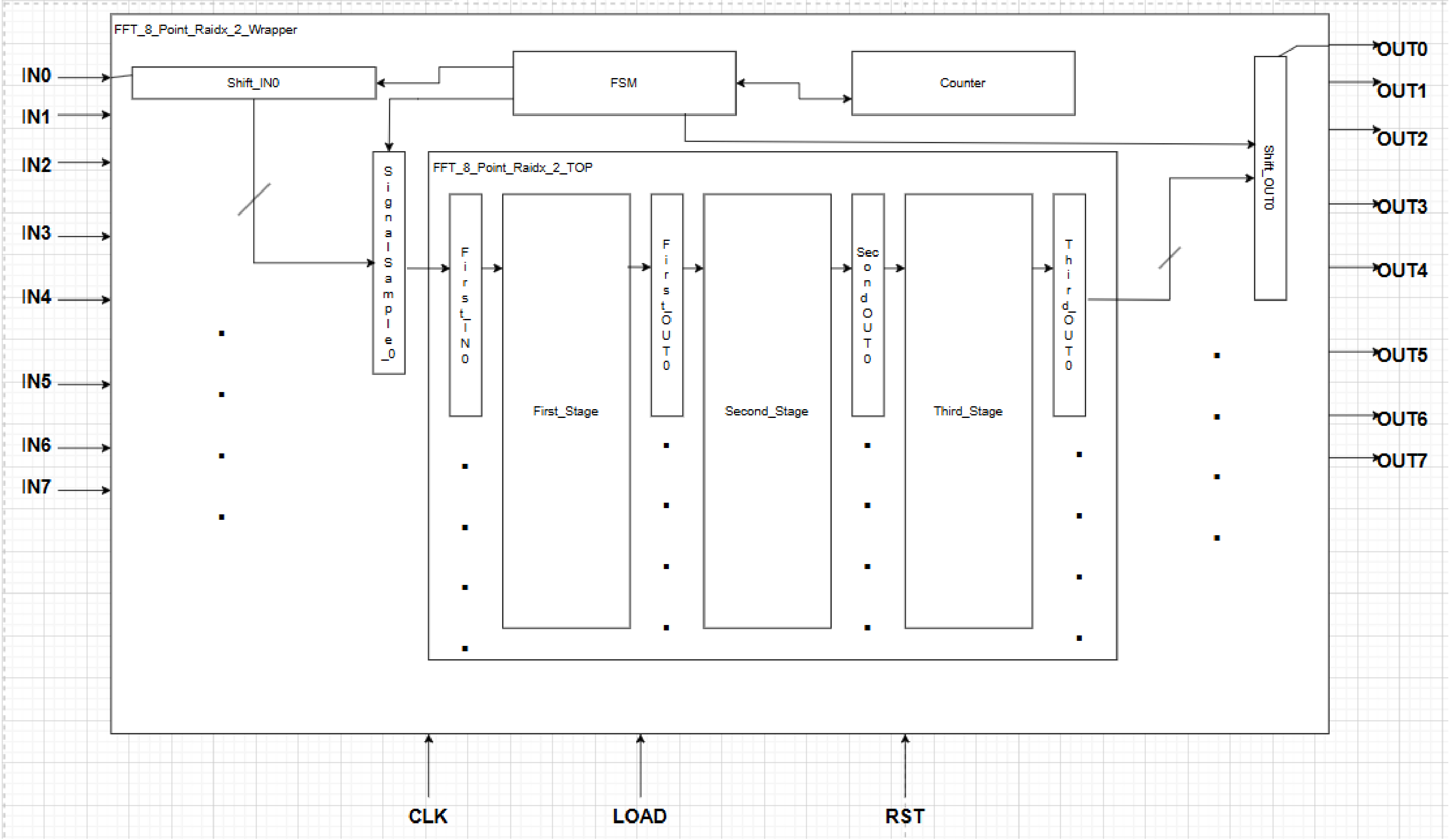
- Only the inputs of the first sample bits (9-bits) are shown.

- <u>Note:</u> Each of the drawn I/P, O/P, & internal signals has to splitted to real signal and imaginary signal (Not drawn).

- Therefore we will have: 8*2+3 = 19 I/P Port (bits).

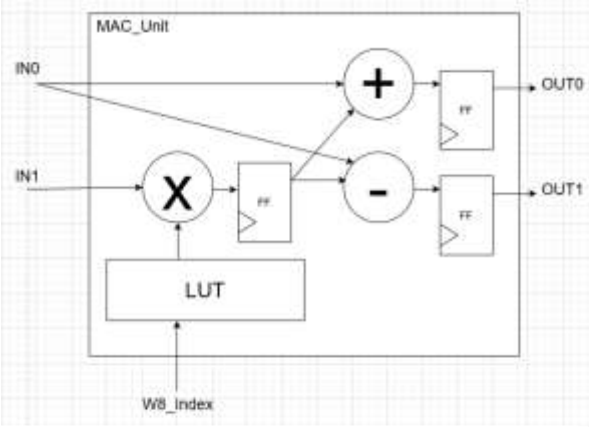
- And 8*2 = 16 O/P ports (bits).

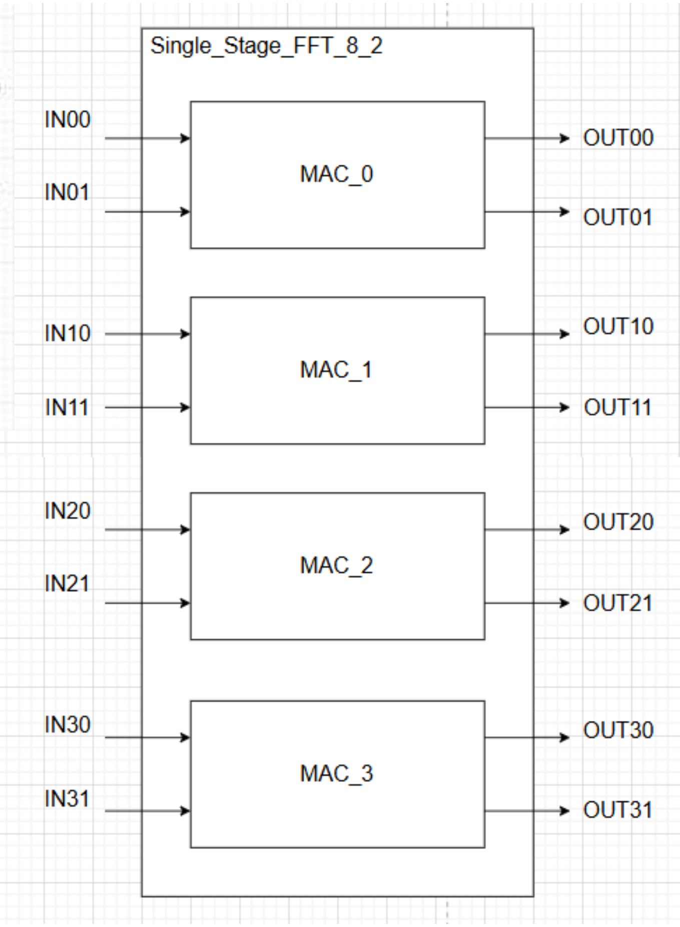
- All inputs are set to be fixed-point representations of notation Qx.8, while outputs are also fixed point representation of notation Q4.8.



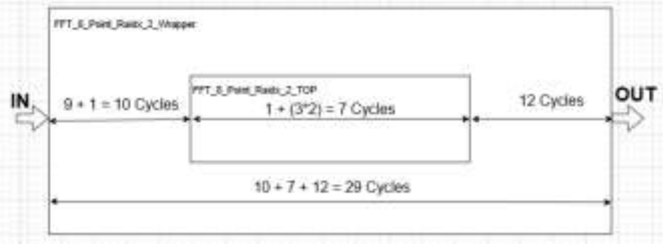
# RTL design cont.

- Single stage has 4 MAC blocks:
- Single stage has the following internal blocks:
  - Single Complex multiplier
  - Single Complex adder.
  - Single Complex subtractor.
  - LUT (Memory) to store twiddle factors. (I should make one LUT for all MACs[Future work]), but the optimizer of the synthesis tool may handle this.





- <u>Complex multiplier:</u> Inputs are Qx.8 and Q2.10(Twiddle facotr), therefore the output in case of full precision will be Q(x+2).18. According to the system modeling step this output is truncated to fit Qy.8. During operation you don’t need to make virtual fractional decimal point alignment bec. it’s multiplication.
- <u>Complex adder and subtractor:</u> **Single module with operation selector** Inputs are Qx.8 and Qy.8(Twiddle facotr), therefore the output in case of full precision will be Q(x+y).8. According to the system modeling step this output is truncated to fit Qz.8. During operation you don’t need to make virtual fractional decimal point alignment bec. it’s multiplication.
- Latency (The number of cycles from the first input sample to the first output sample) = 29 cycles.



# Verification

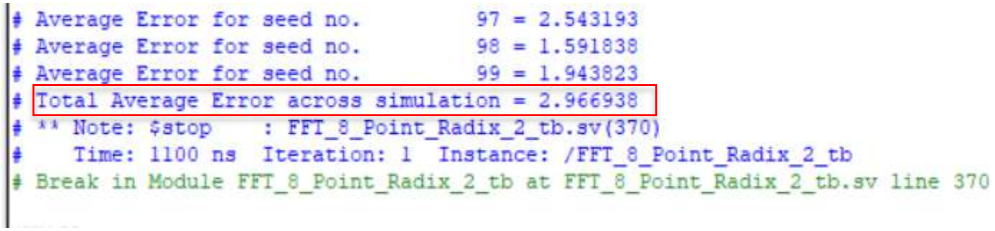
- Verification based on a normal testbench to verify the system operation and compare between the system’s output with the golden model output obtained by Matlab at the system modeling step.

- Inputs come from the randomization process at matlab are saved as fixed-point Q1.8 in a text file (FFT_Golden_In_bin.txt) and read inside testbench using “readmemb” system function. Also the outputs of the golden model of Matlab **real and imaginary parts**.

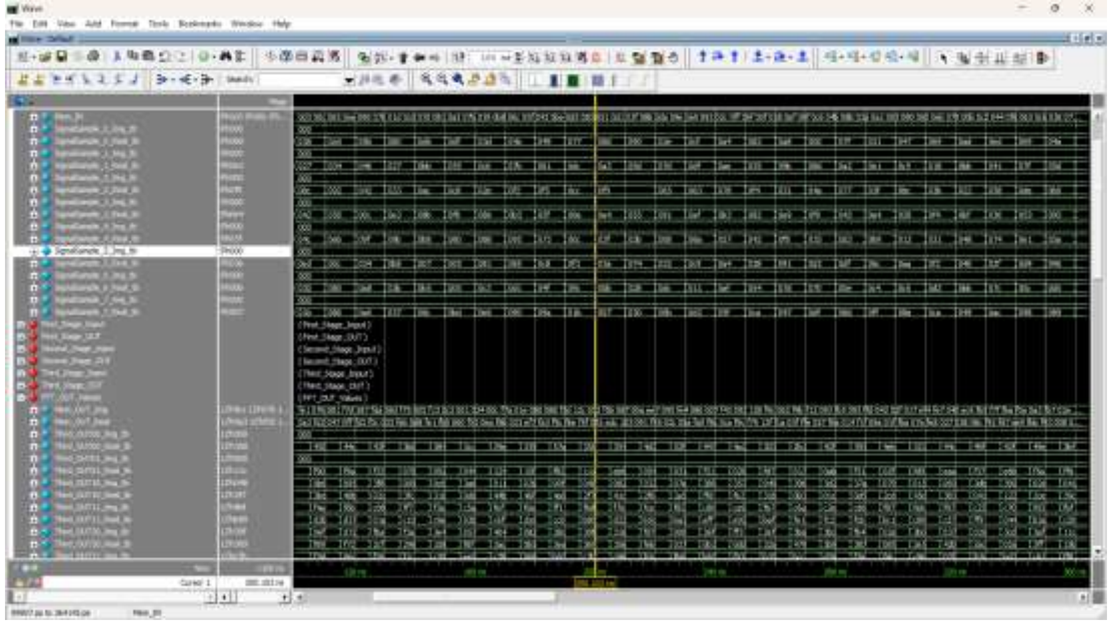
- Error calculation:
  - First = abs(FFT_Module_Real_OUT - FFT_Golden_Real_OUT)
  - Second = abs(FFT_Module_Img_OUT - FFT_Golden_Img_OUT)
  - Error_In_Magnitude = sqrt(First*First - Second*Second) ⟹ Error in one sample
  - Single_Seed_Error = $\sum_0^7 Error\_In\_Magnitude$ ⟹ Error in single seed
  - Error_All_Seeds = $\sum_0^7 Single\_Seed\_Error$
  - Average_Error_All_Seeds = Error_All_Seeds / 100

# Verification

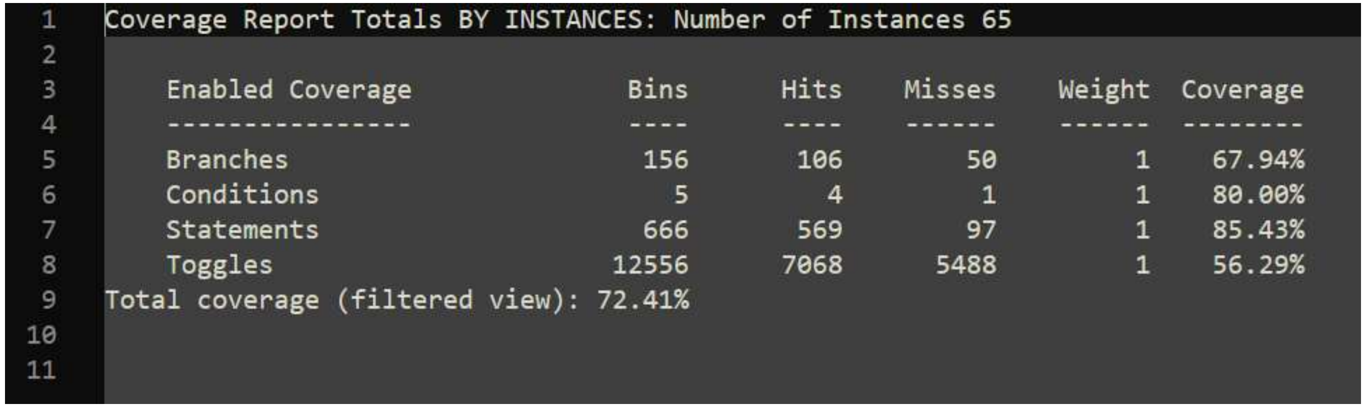
- Verification results:
  - Waveform: No unknowns
  - Transcript:
    - **Average_Error_All_Seeds = 2.966938**
    - **For signle sample = Average_Error_All_Seeds/8 = 0.371**



```
# Average Error for seed no.          97 = 2.543193
# Average Error for seed no.          98 = 1.591838
# Average Error for seed no.          99 = 1.943823
# Total Average Error across simulation = 2.966938
# ** Note: $stop    : FFT_8_Point_Radix_2_tb.sv(370)
#    Time: 1100 ns  Iteration: 1  Instance: /FFT_8_Point_Radix_2_tb
# Break in Module FFT_8_Point_Radix_2_tb at FFT_8_Point_Radix_2_tb.sv line 370
```



- **Code coverage report:**



```
Coverage Report Totals BY INSTANCES: Number of Instances 65

    Enabled Coverage              Bins      Hits    Misses    Weight  Coverage
    ----------------              ----      ----    ------    ------  --------
    Branches                       156       106        50         1    67.94%
    Conditions                       5         4         1         1    80.00%
    Statements                     666       569        97         1    85.43%
    Toggles                      12556      7068      5488         1    56.29%
Total coverage (filtered view): 72.41%
```

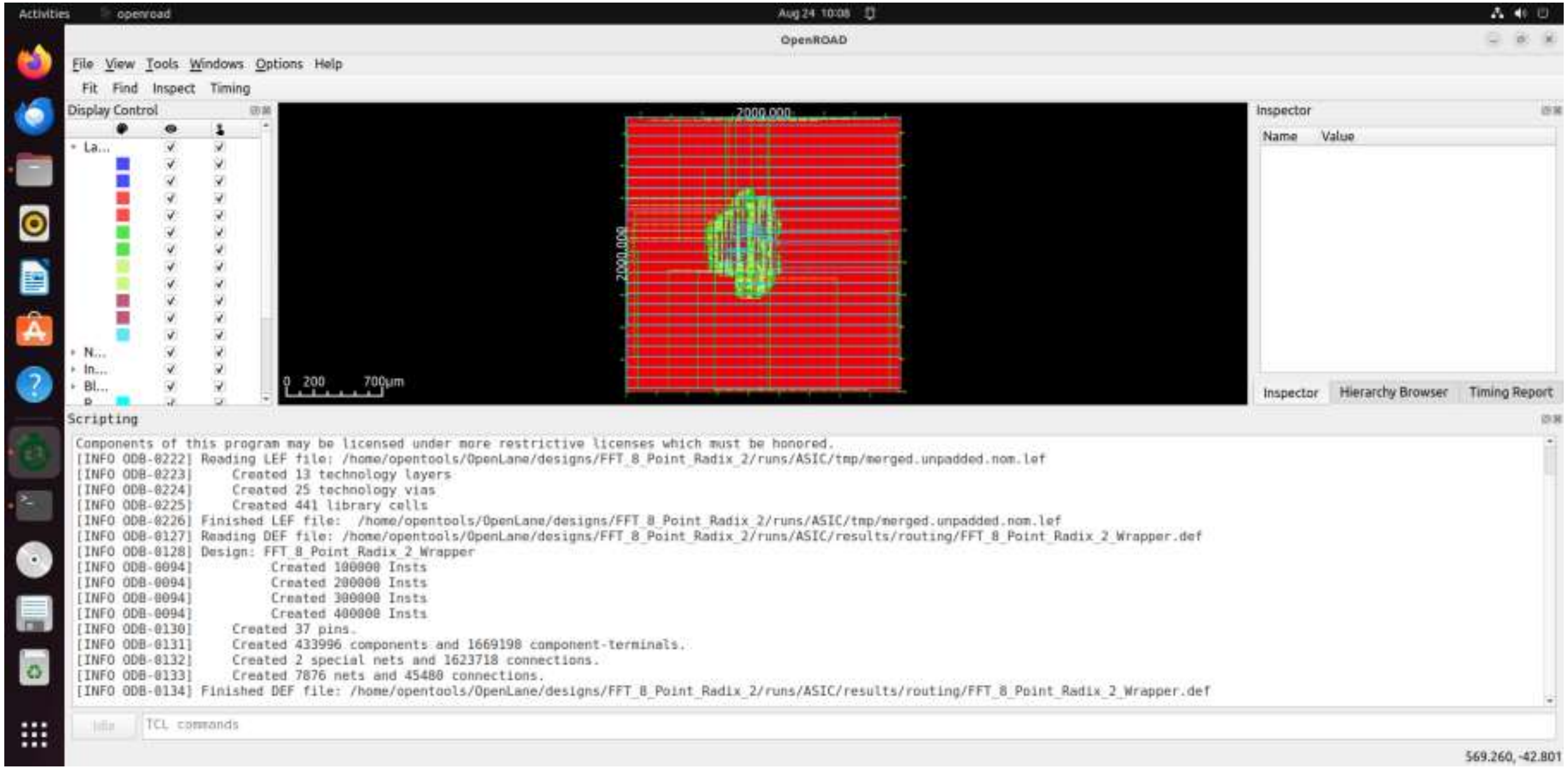
- Future work:

  Class-based verification envirnoment

# ASIC implementation

- OpenLane tool (open-source) is used. Therefore by default the technologyis sky130A PDK and the sky130_fd_sc_hd standard cell library
- Max die area is 2mm * 2mm.
- Constrained clock period is 18ns.
- Final output die from OpenLane: Post-route utilization = 4% @ placement

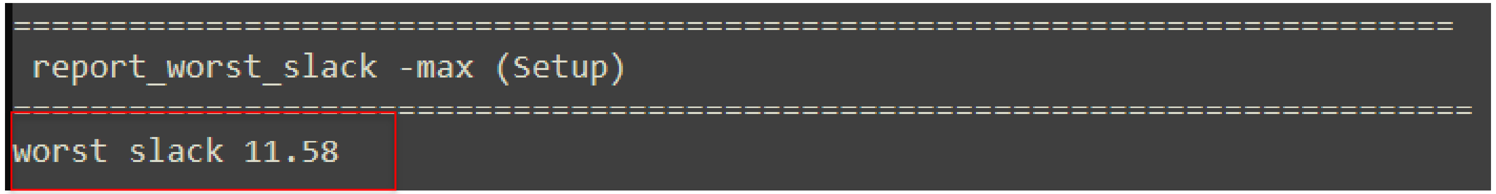
```
==========================================
Design area 155580 u^2 4% utilization.
```



```
Components of this program may be licensed under more restrictive licenses which must be honored.
[INFO ODB-0222] Reading LEF file: /home/opentools/OpenLane/designs/FFT_8_Point_Radix_2/runs/ASIC/tmp/merged.unpadded.nom.lef
[INFO ODB-0223]     Created 13 technology layers
[INFO ODB-0224]     Created 25 technology vias
[INFO ODB-0225]     Created 441 library cells
[INFO ODB-0226] Finished LEF file:  /home/opentools/OpenLane/designs/FFT_8_Point_Radix_2/runs/ASIC/tmp/merged.unpadded.nom.lef
[INFO ODB-0127] Reading DEF file: /home/opentools/OpenLane/designs/FFT_8_Point_Radix_2/runs/ASIC/results/routing/FFT_8_Point_Radix_2_Wrapper.def
[INFO ODB-0128] Design: FFT_8_Point_Radix_2_Wrapper
[INFO ODB-0094]         Created 100000 Insts
[INFO ODB-0094]         Created 200000 Insts
[INFO ODB-0094]         Created 300000 Insts
[INFO ODB-0094]         Created 400000 Insts
[INFO ODB-0130]     Created 37 pins.
[INFO ODB-0131]     Created 433996 components and 1669198 component-terminals.
[INFO ODB-0132]     Created 2 special nets and 1623718 connections.
[INFO ODB-0133]     Created 7876 nets and 45480 connections.
[INFO ODB-0134] Finished DEF file: /home/opentools/OpenLane/designs/FFT_8_Point_Radix_2/runs/ASIC/results/routing/FFT_8_Point_Radix_2_Wrapper.def
```

# ASIC implementation cont.

- Worst Negative Slack (WNS):

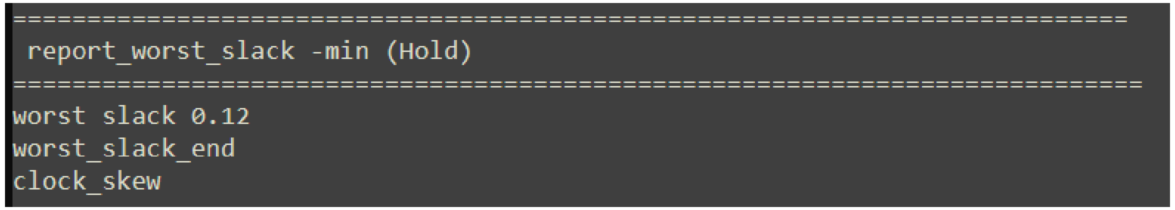


```
==============================================================================
 report_worst_slack -max (Setup)
==============================================================================
worst slack 11.58
```

- Minimum achieveable clock period = CLOCK_PERIOD - WNS = 18.0 – 11.58 = 6.42 ns

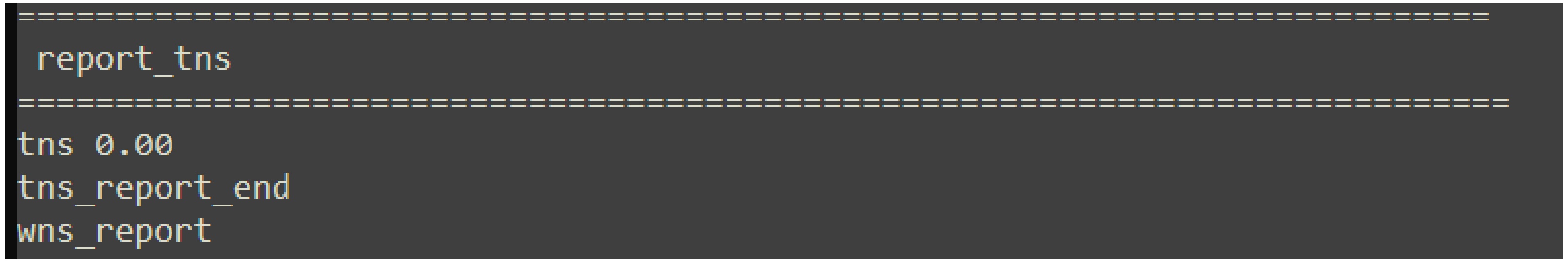
**Therefore the maximum allowed clock = 1 / Minimum achieveable clock period = 155.76MHz**

- Hold Slack :



```
==============================================================================
 report_worst_slack -min (Hold)
==============================================================================
worst slack 0.12
worst_slack_end
clock_skew
```

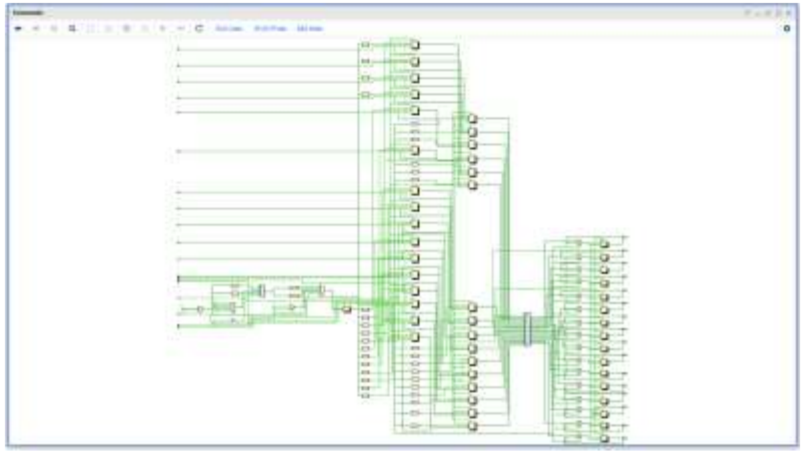
- Total Negative Slack (TNS):

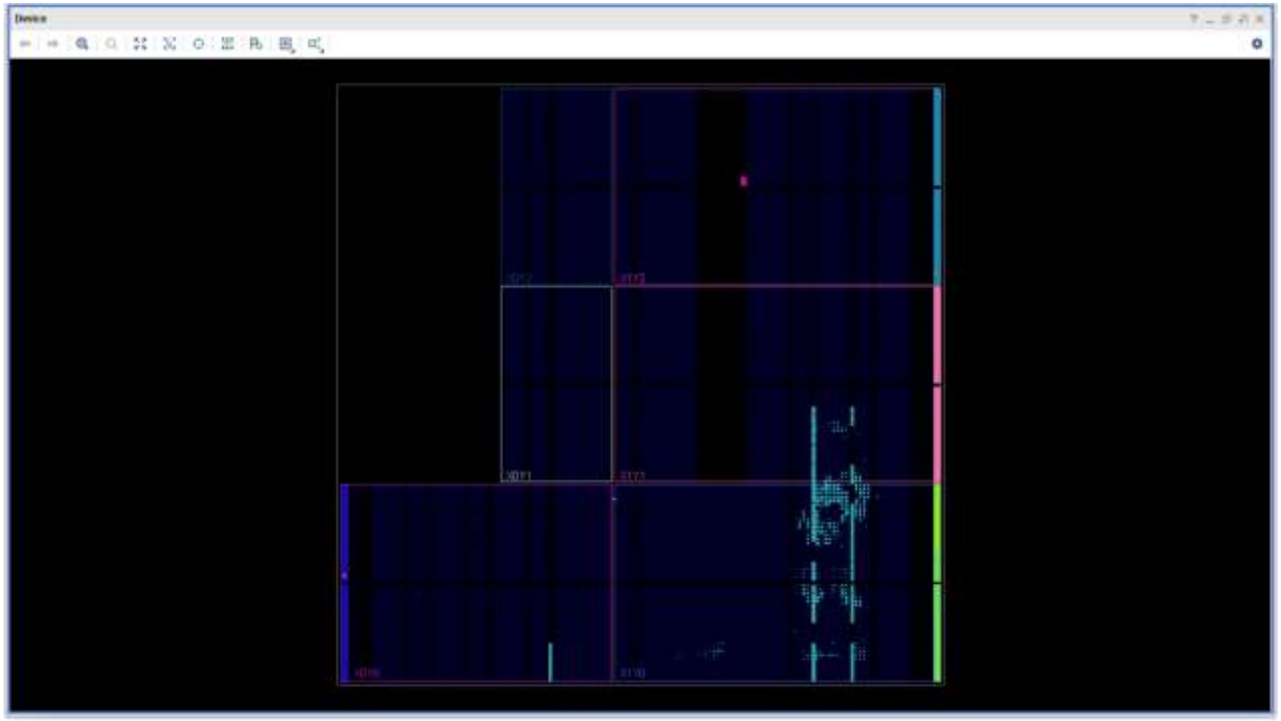


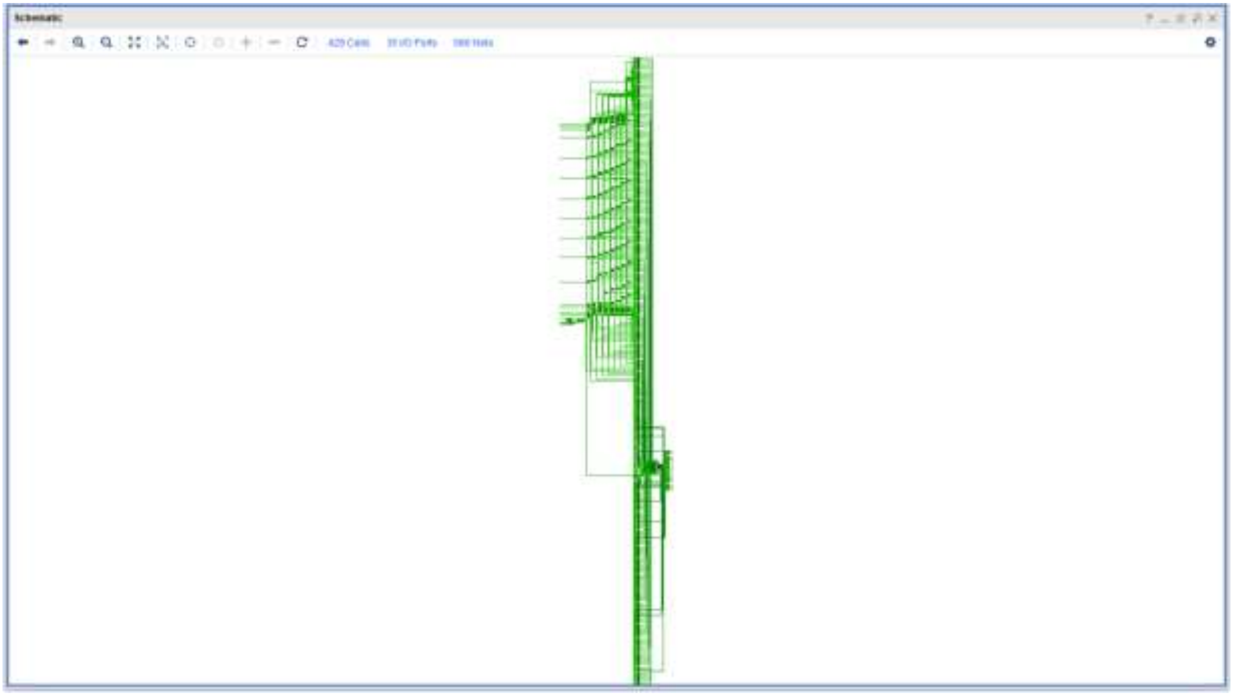
```
==============================================================================
 report_tns
==============================================================================
tns 0.00
tns_report_end
wns_report
```

# FPGA implementation

- Vivado tool is used to synthesize the design for FPGA.
- Implementation is done for the ZYNQ FPGA part no.: xc7z020clg484-2
- Constrained clock period is 10ns.
- Elaborated design:
- Synthesized design:
- Impelementation:

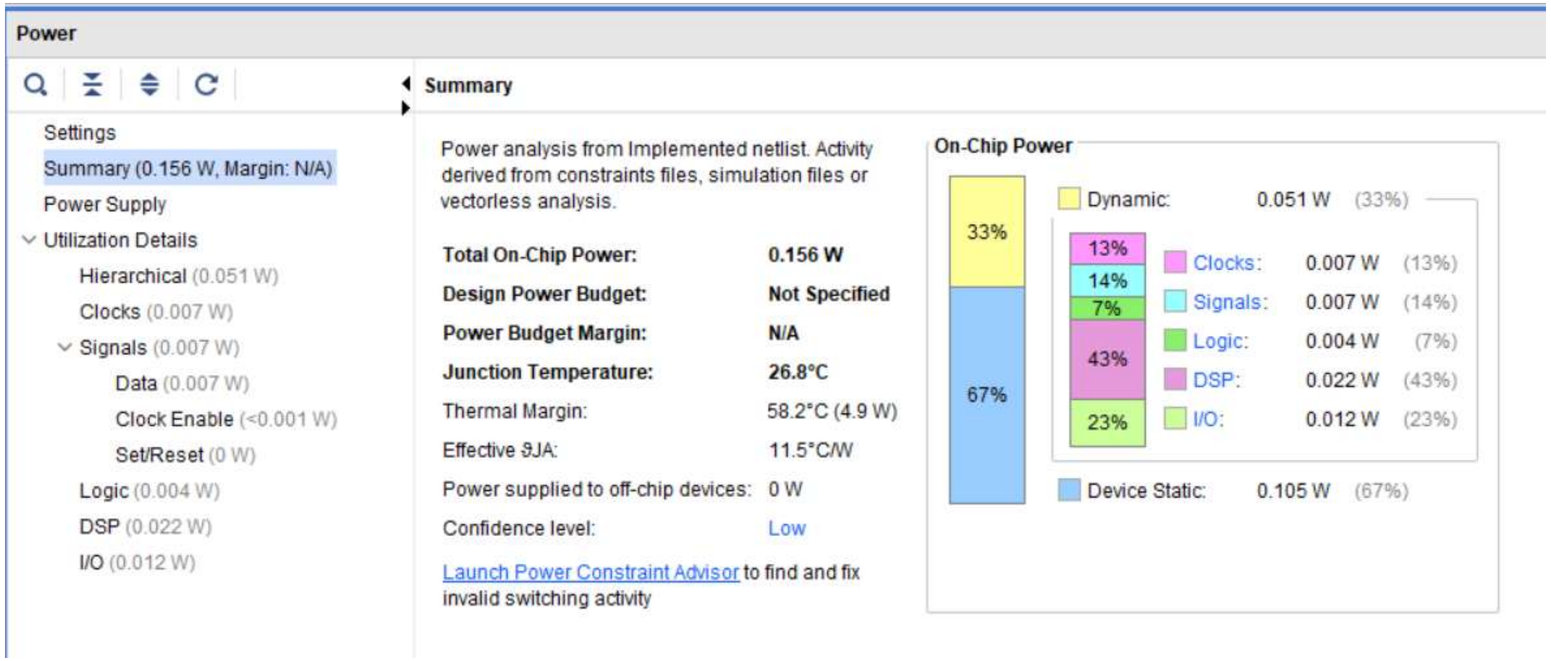






# FPGA implementation cont. (reports)

- Power report:



Power

Settings
Summary (0.156 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.051 W)
Clocks (0.007 W)
Signals (0.007 W)
Data (0.007 W)
Clock Enable (<0.001 W)
Set/Reset (0 W)
Logic (0.004 W)
DSP (0.022 W)
I/O (0.012 W)

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

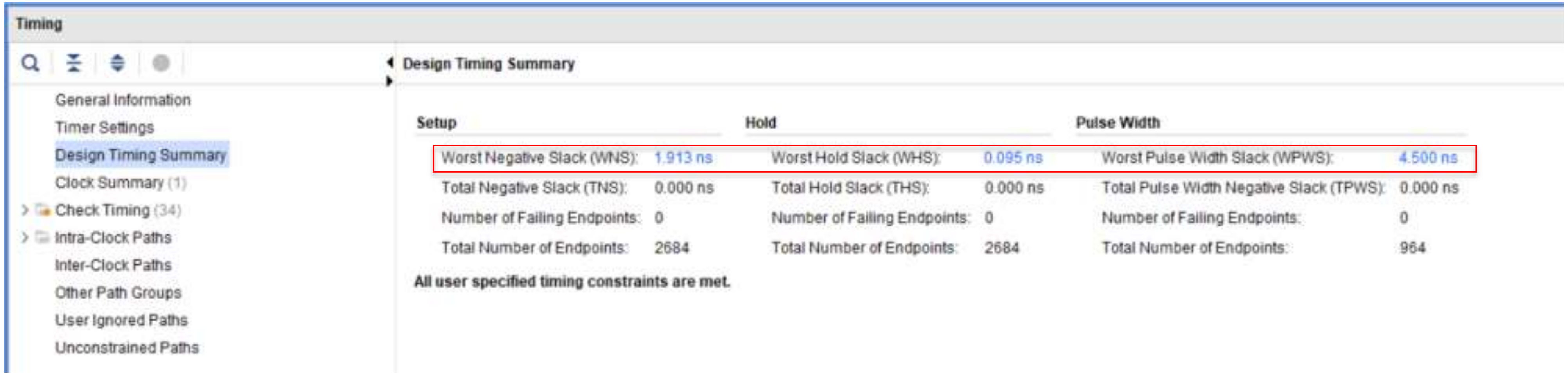
| | |
|---|---|
| **Total On-Chip Power:** | **0.156 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **26.8°C** |
| Thermal Margin: | 58.2°C (4.9 W) |
| Effective ϑJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

| | | |
|---|---|---|
| Dynamic: | 0.051 W | (33%) |
| Clocks: | 0.007 W | (13%) |
| Signals: | 0.007 W | (14%) |
| Logic: | 0.004 W | (7%) |
| DSP: | 0.022 W | (43%) |
| I/O: | 0.012 W | (23%) |
| Device Static: | 0.105 W | (67%) |

- Timing report:



Timing

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (34)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

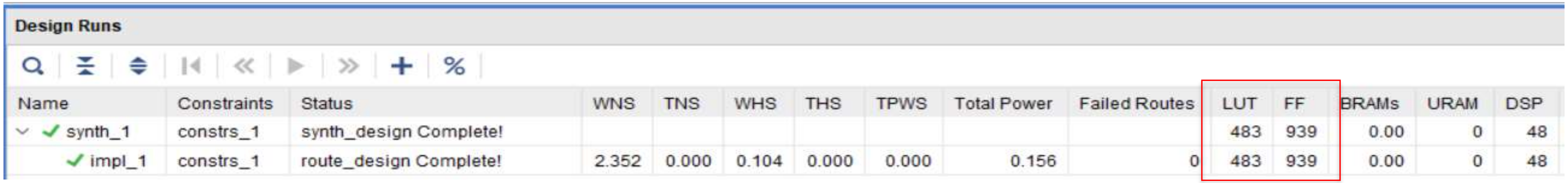
Design Timing Summary

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 1.913 ns | Worst Hold Slack (WHS): | 0.095 ns | Worst Pulse Width Slack (WPWS): | 4.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 2684 | Total Number of Endpoints: | 2684 | Total Number of Endpoints: | 964 |

All user specified timing constraints are met.

# FPGA implementation cont. (reports)

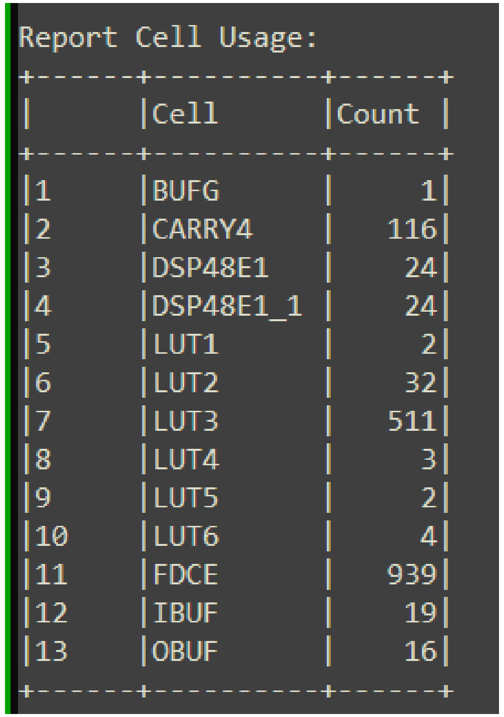
- Total cells used report:



**Design Runs**

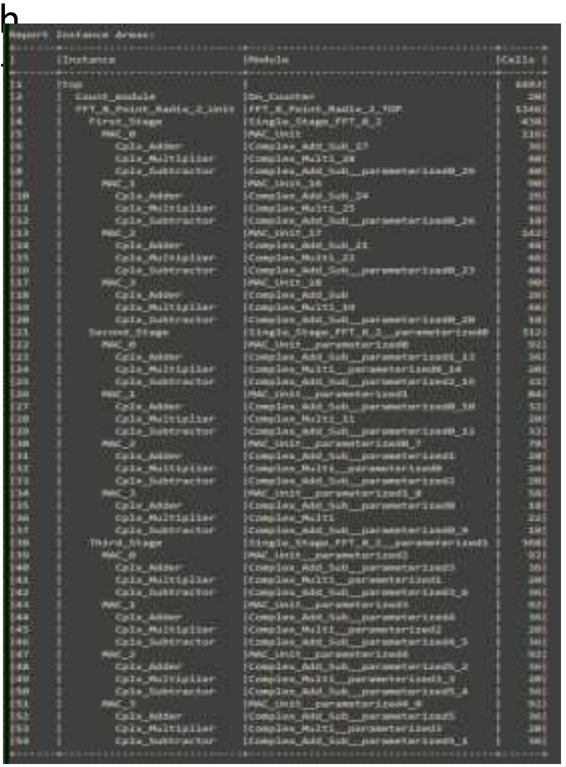
| Name | Constraints | Status | WNS | TNS | WHS | THS | TPWS | Total Power | Failed Routes | LUT | FF | BRAMs | URAM | DSP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ✓ synth_1 | constrs_1 | synth_design Complete! | | | | | | | | 483 | 939 | 0.00 | 0 | 48 |
| ✓ impl_1 | constrs_1 | route_design Complete! | 2.352 | 0.000 | 0.104 | 0.000 | 0.000 | 0.156 | 0 | 483 | 939 | 0.00 | 0 | 48 |

- Cells used  in details report:



```
Report Cell Usage:
+------+----------+------+
|      |Cell      |Count |
+------+----------+------+
|1     |BUFG      |     1|
|2     |CARRY4    |   116|
|3     |DSP48E1   |    24|
|4     |DSP48E1_1 |    24|
|5     |LUT1      |     2|
|6     |LUT2      |    32|
|7     |LUT3      |   511|
|8     |LUT4      |     3|
|9     |LUT5      |     2|
|10    |LUT6      |     4|
|11    |FDCE      |   939|
|12    |IBUF      |    19|
|13    |OBUF      |    16|
+------+----------+------+
```

- Number of cells used for each instantiation  in details report:



```
Report Instance Areas:
+------+--------------------------+-----------------------------------------+------+
|      |Instance                  |Module                                   |Cells |
+------+--------------------------+-----------------------------------------+------+
|1     |top                       |                                         | [illegible]|
|2     |  Count_module            |Dn_Counter                               | [illegible]|
|3     |  FFT_8_Point_Radix_2_Unit|FFT_8_Point_Radix_2_TOP                  | [illegible]|
|4     |    First_Stage           |Single_Stage_FFT_R_2                     | [illegible]|
|5     |      MAC_0               |MAC_Unit                                 |   116|
|6     |        Cplx_Adder        |Complex_Add_Sub_27                       | [illegible]|
|7     |        Cplx_Multiplier   |Complex_Multi_28                         | [illegible]|
|8     |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_29       | [illegible]|
|9     |      MAC_1               |MAC_Unit_16                              | [illegible]|
|10    |        Cplx_Adder        |Complex_Add_Sub_24                       | [illegible]|
|11    |        Cplx_Multiplier   |Complex_Multi_25                         | [illegible]|
|12    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_26       | [illegible]|
|13    |      MAC_2               |MAC_Unit_17                              | [illegible]|
|14    |        Cplx_Adder        |Complex_Add_Sub_21                       | [illegible]|
|15    |        Cplx_Multiplier   |Complex_Multi_22                         | [illegible]|
|16    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_23       | [illegible]|
|17    |      MAC_3               |MAC_Unit_18                              | [illegible]|
|18    |        Cplx_Adder        |Complex_Add_Sub                          | [illegible]|
|19    |        Cplx_Multiplier   |Complex_Multi_19                         | [illegible]|
|20    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_20       | [illegible]|
|21    |    Second_Stage          |Single_Stage_FFT_R_2__parameterized0     |   312|
|22    |      MAC_0               |MAC_Unit__parameterized0                 |    92|
|23    |        Cplx_Adder        |Complex_Add_Sub__parameterized1_13       | [illegible]|
|24    |        Cplx_Multiplier   |Complex_Multi__parameterized0_14         | [illegible]|
|25    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized2_15       | [illegible]|
|26    |      MAC_1               |MAC_Unit__parameterized1                 | [illegible]|
|27    |        Cplx_Adder        |Complex_Add_Sub__parameterized0_10       | [illegible]|
|28    |        Cplx_Multiplier   |Complex_Multi_11                         | [illegible]|
|29    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_12       | [illegible]|
|30    |      MAC_2               |MAC_Unit__parameterized0_7               | [illegible]|
|31    |        Cplx_Adder        |Complex_Add_Sub__parameterized1          | [illegible]|
|32    |        Cplx_Multiplier   |Complex_Multi__parameterized0            | [illegible]|
|33    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized2          | [illegible]|
|34    |      MAC_3               |MAC_Unit__parameterized1_8               | [illegible]|
|35    |        Cplx_Adder        |Complex_Add_Sub__parameterized0          | [illegible]|
|36    |        Cplx_Multiplier   |Complex_Multi                            | [illegible]|
|37    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_9        | [illegible]|
|38    |    Third_Stage           |Single_Stage_FFT_R_2__parameterized3     | [illegible]|
|39    |      MAC_0               |MAC_Unit__parameterized2                 | [illegible]|
|40    |        Cplx_Adder        |Complex_Add_Sub__parameterized3          | [illegible]|
|41    |        Cplx_Multiplier   |Complex_Multi__parameterized1            | [illegible]|
|42    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized2_6        | [illegible]|
|43    |      MAC_1               |MAC_Unit__parameterized3                 | [illegible]|
|44    |        Cplx_Adder        |Complex_Add_Sub__parameterized4          | [illegible]|
|45    |        Cplx_Multiplier   |Complex_Multi__parameterized2            | [illegible]|
|46    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized0_3        | [illegible]|
|47    |      MAC_2               |MAC_Unit__parameterized4                 | [illegible]|
|48    |        Cplx_Adder        |Complex_Add_Sub__parameterized5_2        | [illegible]|
|49    |        Cplx_Multiplier   |Complex_Multi__parameterized3_1          | [illegible]|
|50    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized5_4        | [illegible]|
|51    |      MAC_3               |MAC_Unit__parameterized4_0               | [illegible]|
|52    |        Cplx_Adder        |Complex_Add_Sub__parameterized5          | [illegible]|
|53    |        Cplx_Multiplier   |Complex_Multi__parameterized3            | [illegible]|
|54    |        Cplx_Subtractor   |Complex_Add_Sub__parameterized5_1        | [illegible]|
+------+--------------------------+-----------------------------------------+------+
```

ANALOG DEVICES
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# Thank You!