Project 1: Spartan6 - DSP48A1

RTL code

DFFlop:

D_FFlop.v

```
`define ASYNC     0
`define SYNC      1
module D_FFlop(
    D, rstn, clk_EN, clk, Q
);
parameter RST_TYPE = `SYNC,
          WIDTH    = 1;
input [WIDTH-1 :0] D;
input rstn, clk_EN, clk;
output reg [WIDTH-1 :0] Q;

generate if(RST_TYPE == `ASYNC) begin
        always @(posedge clk or negedge rstn)
        begin
            if(clk_EN) begin
                if(rstn)
                    Q <= 0;
                else
                    Q <= D;
            end
        end
    end
    else begin
        always @(posedge clk)
        begin
            if(clk_EN) begin
                if(rstn)
                    Q <= 0;
                else
                    Q <= D;
            end
        end
    end

endgenerate
endmodule
```

mux 2:

mux_2.v

```
module mux_2(In0, In1, SEL, Out);
parameter WIDTH = 1;

input [WIDTH-1 :0] In0, In1;
input SEL;
output reg [WIDTH-1 :0] Out;

always@(*) begin
    case(SEL)
        1'd0: Out = In0;
        1'd1: Out = In1;
    endcase
end


endmodule
```

Common unit:

D_FFlop_mux2.v

```
`define ASYNC     0
`define SYNC      1
module D_FFlop_mux2(In, SEL_M, rstn_M, clk_EN_M, clk_M, Out_mux);
parameter RST_TYPE_M = `SYNC,
          WIDTH_M    = 1;

input [WIDTH_M-1 : 0] In;
input rstn_M, clk_EN_M, clk_M;
input SEL_M;
output [WIDTH_M-1 : 0] Out_mux;

wire [WIDTH_M-1 : 0] DFFlop_Out;

//Modules instantiation
D_FFlop #(.RST_TYPE(RST_TYPE_M), .WIDTH(WIDTH_M)) DFF(
    .D(In), .rstn(rstn_M), .clk_EN(clk_EN_M), .clk(clk_M), .Q(DFFlop_Out)
);

mux_2 #(.WIDTH(WIDTH_M)) MUX(
    .In0(In), .In1(DFFlop_Out), .SEL(SEL_M), .Out(Out_mux)
);


endmodule
```

mux 4:

mux_4.v

```
module mux_4(In0, In1, In2, In3, SEL_Bus, Out);
parameter WIDTH = 1;

input [WIDTH-1 :0] In0, In1, In2, In3;
input [1 : 0] SEL_Bus;
output reg [WIDTH-1 :0] Out;

always@(*) begin
    case(SEL_Bus)
        4'd0: Out = In0;
        4'd1: Out = In1;
        4'd2: Out = In2;
        4'd3: Out = In3;
    endcase
end


endmodule
```

Spartan6 - DSP48A1:

Spartan6_DSP48A1.v

```
`define NO_REG                  0
`define REG                     1
`define CARRYIN_PARAM           0
`define OPMODE5_PARAM           1
`define DIRECT                  0
`define CASCADE                 1
`define ASYNC                   0
`define SYNC                    1
module Spartan6_DSP48A1(
    A, B, BCIN, C, D, CARRYIN, PCIN, OPMODE,   /*Operation Inputs*/
    CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, /*Clock Enable Input Ports*/
    RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, /*Reset Input Ports:*/
    CLK, M, P, CARRYOUT, CARRYOUTF, BCOUT, PCOUT   /*Operation Outputs*/
);
parameter [0:0] A0REG = `REG, A1REG = `REG,
                B0REG = `REG, B1REG = `REG,
                CREG = `REG, DREG = `REG, MREG = `REG,
                PREG = `REG, CARRYINREG = `REG,
                CARRYOUTREG = `REG, OPMODEREG = `REG,
                CARRYINSEL = `OPMODE5_PARAM, B_INPUT = `DIRECT, RSTTYPE = `DIRECT;

input [17:0] A, B, BCIN, D;
input [47:0] C;
input [7:0] OPMODE;
input CARRYIN, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, /*Clock Enable Input Ports*/
      RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, /*Reset Input Ports:*/
      CLK;
input [47:0] PCIN;
/*Operation outputs*/
output [35:0] M;
output [47:0] P;
output reg [47:0] PCOUT;
output [17:0] BCOUT;
output CARRYOUT;
output reg CARRYOUTF;

wire [7:0] OPMODE_REG_Out;

wire [17:0] A0_Reg_Out, A1_Reg_Out, B0_Reg_In, B0_Reg_Out, B1_Reg_In_mux_2_Out, D_REG_Out;
reg  [17:0] Pre_Add_Sub_Out;

wire [47:0] C_REG_Out, X_Mux_Out, Z_Mux_Out;

wire [35:0] M_REG_Out;
reg  [35:0] Multiplier_Out;

wire CYI_Reg_In, CYI_Reg_Out;

```

Spartan6_DSP48A1.v

```

wire CYI_Reg_In, CYI_Reg_Out;

reg CYO_Reg_In;

reg [47:0] Post_Add_Sub_Out;

genvar i;

//Modules instantiations
/*OPMODE register*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(8)) OPMODE_REG(
    .In(OPMODE), .SEL_M(OPMODEREG), .rstn_M(RSTOPMODE), .clk_EN_M(CEOPMODE), .clk_M(CLK), .Out_mux(OPMODE_REG_Out)
);

/*A Input*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(18)) A0_REG(
    .In(A), .SEL_M(A0REG), .rstn_M(RSTA), .clk_EN_M(CEA), .clk_M(CLK), .Out_mux(A0_Reg_Out)
);

D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(18)) A1_REG(
    .In(A0_Reg_Out), .SEL_M(A1REG), .rstn_M(RSTA), .clk_EN_M(CEA), .clk_M(CLK), .Out_mux(A1_Reg_Out)
);

/*B Input*/
mux_2 #(.WIDTH(18)) B0_In_mux_2(.In0(B), .In1(BCIN), .SEL(B_INPUT), .Out(B0_Reg_In));

D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(18)) B0_REG(
    .In(B0_Reg_In), .SEL_M(B0REG), .rstn_M(RSTB), .clk_EN_M(CEB), .clk_M(CLK), .Out_mux(B0_Reg_Out)
);

mux_2 #(.WIDTH(18)) B1_Reg_In_mux_2(.In0(Pre_Add_Sub_Out), .In1(B0_Reg_Out), .SEL(OPMODE_REG_Out[4]), .Out(B1_Reg_In_mux_2_Out));

D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(18)) B1_REG(
    .In(B1_Reg_In_mux_2_Out), .SEL_M(B1REG), .rstn_M(RSTB), .clk_EN_M(CEB), .clk_M(CLK), .Out_mux(BCOUT)
);

/*C Input*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(48)) C_REG(
    .In(C), .SEL_M(CREG), .rstn_M(RSTC), .clk_EN_M(CEC), .clk_M(CLK), .Out_mux(C_REG_Out)
);

/*D Input*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(18)) D_REG(
    .In(D), .SEL_M(DREG), .rstn_M(RSTD), .clk_EN_M(CED), .clk_M(CLK), .Out_mux(D_REG_Out)
);

```

```
/*M register(Multiplier register)*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(36)) M_REG(
    .In(Multiplier_Out), .SEL_M(MREG), .rstn_M(RSTM), .clk_EN_M(CEM), .clk_M(CLK), .Out_mux(M_REG_Out)
);
generate for(i = 0; i < 36; i=i+1) begin
        buf M_buffer(M[i], M_REG_Out[i]);
    end
endgenerate

/*CYI register*/
mux_2 CarryIn_Sel_Mux2(.In0(OPMODE_REG_Out[5]), .In1(CARRYIN), .SEL(CARRYINSEL), .Out(CYI_Reg_In));

D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(1)) CYI_REG(
    .In(CYI_Reg_In), .SEL_M(CARRYINREG), .rstn_M(RSTCARRYIN), .clk_EN_M(CECARRYIN), .clk_M(CLK), .Out_mux(CYI_Reg_Out)
);

/*X multiplexier*/
mux_4 #(.WIDTH(48)) X_Mux_4(
    .In0(48'h000000), .In1({13'b0,M_REG_Out}), .In2(P), .In3({3'b0,D[11:0], A[17:0],B[17:0]}), .SEL_Bus(OPMODE_REG_Out[1:0]), .Out(X_Mux_Out)
);

/*Z multiplexier*/
mux_4 #(.WIDTH(48)) Z_Mux_4(
    .In0(48'h000000), .In1(PCIN), .In2(P), .In3(C_REG_Out), .SEL_Bus(OPMODE_REG_Out[3:2]), .Out(Z_Mux_Out)
);

/*CYO register*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(1)) CYO_REG(
    .In(CYO_Reg_In), .SEL_M(CARRYOUTREG), .rstn_M(RSTCARRYIN), .clk_EN_M(CECARRYIN), .clk_M(CLK), .Out_mux(CARRYOUT)
);

/*P register*/
D_FFlop_mux2 #(.RST_TYPE_M(RSTTYPE), .WIDTH_M(48)) P_REG(
    .In(Post_Add_Sub_Out), .SEL_M(PREG), .rstn_M(RSTP), .clk_EN_M(CEP), .clk_M(CLK), .Out_mux(P)
);

//Core code

/*Pre-Adder/Subractor*/
always @(*) begin
    case(OPMODE_REG_Out[6])
    1'b0: Pre_Add_Sub_Out = D_REG_Out + B0_Reg_Out;
    1'b1: Pre_Add_Sub_Out = D_REG_Out - B0_Reg_Out;
    endcase
end
```

```
    /*Pre-Adder/Subractor*/
    always @(*) begin
        case(OPMODE_REG_Out[6])
        1'b0: Pre_Add_Sub_Out = D_REG_Out + B0_Reg_Out;
        1'b1: Pre_Add_Sub_Out = D_REG_Out - B0_Reg_Out;
        endcase
    end

    /*Multiplier*/
    always @(*) begin
        Multiplier_Out = BCOUT * A1_Reg_Out;
    end

    /*Post-Adder/Subractor*/
    always @(*) begin
        case(OPMODE_REG_Out[7])
        1'b0: {CYO_Reg_In, Post_Add_Sub_Out} = Z_Mux_Out + X_Mux_Out + CYI_Reg_Out;
        1'b1: {CYO_Reg_In, Post_Add_Sub_Out} = Z_Mux_Out - (X_Mux_Out + CYI_Reg_Out);
        endcase
    end

    /*Concatination*/
    always @(*) begin
        PCOUT = P;
        CARRYOUTF = CARRYOUT;
    end

    endmodule
```

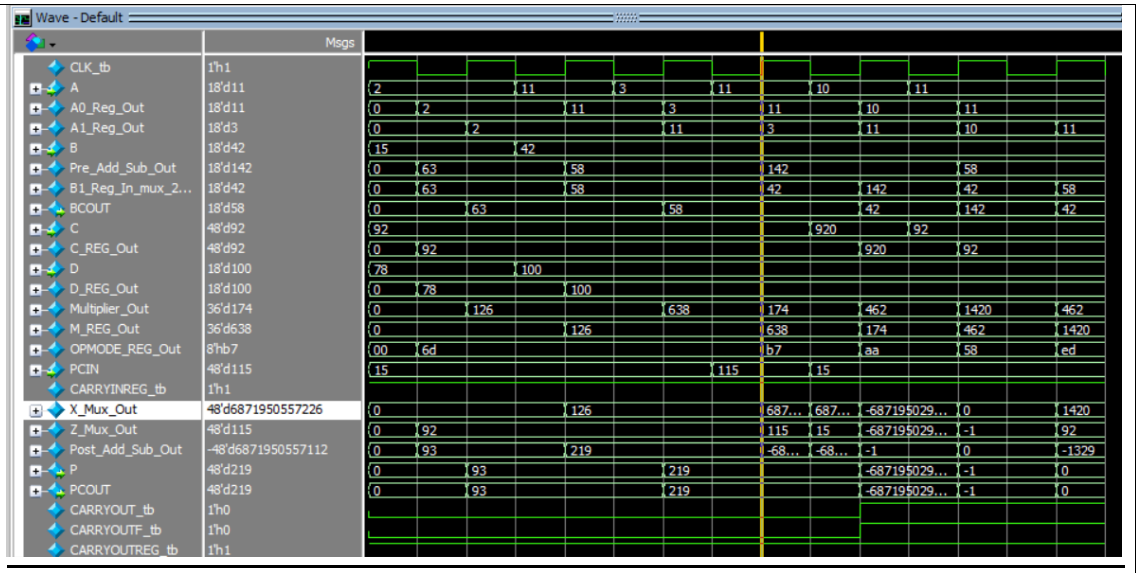
Testbench

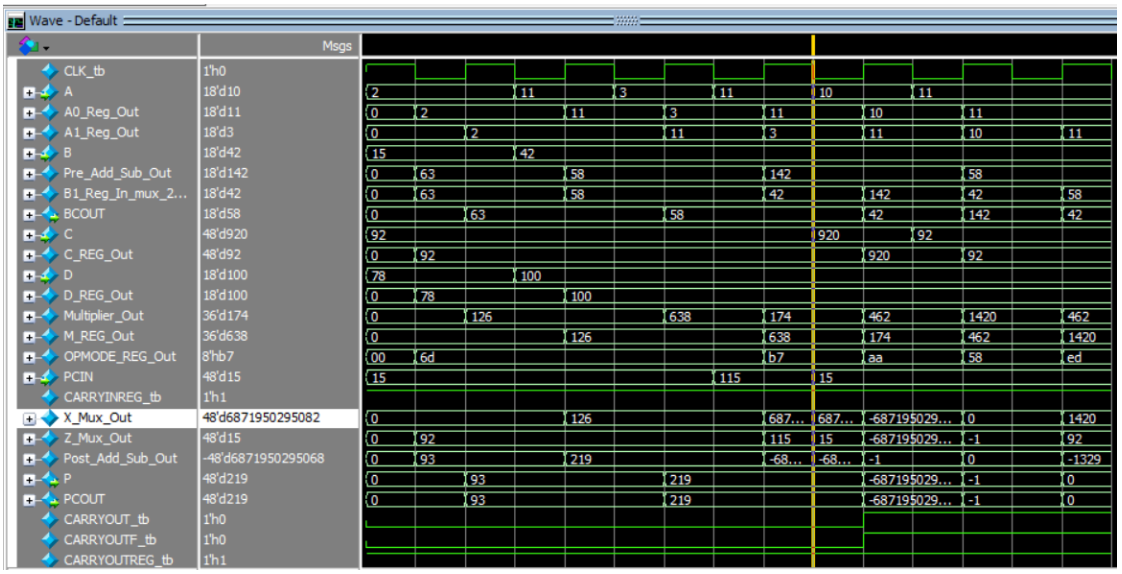
Spartan6_DSP48A1_tb.v

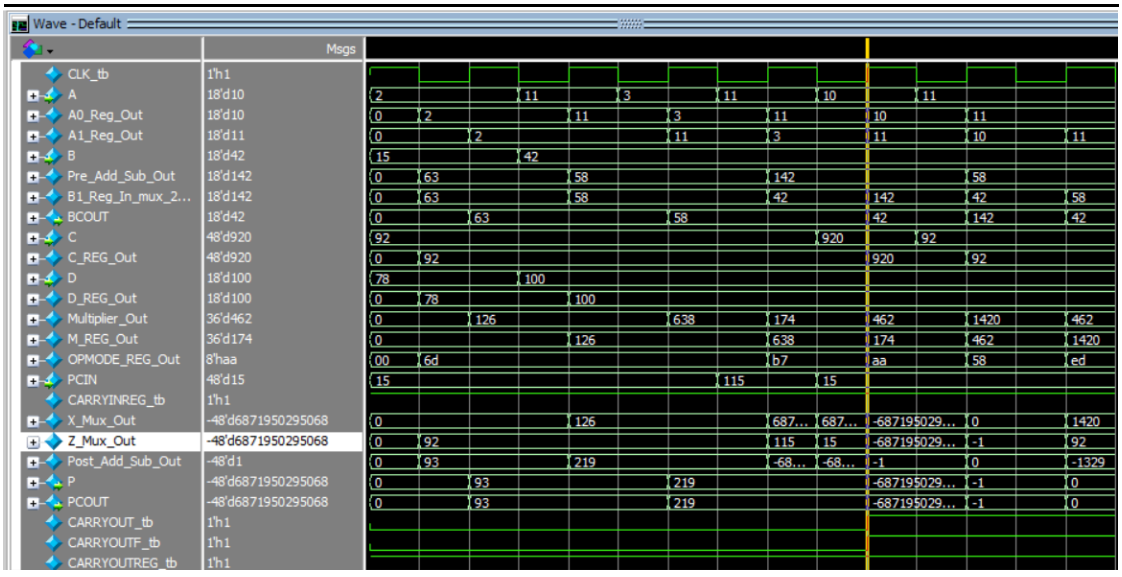
```
`define NO_REG                  0
`define REG                     1
`define CARRYIN_PARAM           0
`define OPMODE5_PARAM           1
`define DIRECT                  0
`define CASCADE                 1
`define ASYNC                   0
`define SYNC                    1
module Sparatan6_DPS48A1_tb();
//Signals declaration
parameter [0:0] A0REG_tb = `REG, A1REG_tb = `REG,
                B0REG_tb = `REG, B1REG_tb = `REG,
                CREG_tb = `REG, DREG_tb = `REG, MREG_tb = `REG,
                PREG_tb = `REG, CARRYINREG_tb = `REG,
                CARRYOUTREG_tb = `REG, OPMODEREG_tb = `REG,
                CARRYINSEL_tb = `OPMODE5_PARAM, B_INPUT_tb = `DIRECT, RSTTYPE_tb = `DIRECT;

reg [17:0] A_tb, B_tb, BCIN_tb, D_tb;
reg [47:0] C_tb;
reg [7:0] OPMODE_tb;
reg CARRYIN_tb, CEA_tb, CEB_tb, CEC_tb, CECARRYIN_tb, CED_tb, CEM_tb, CEOPMODE_tb, CEP_tb, /*Clock Enable Input Ports*/
     RSTA_tb, RSTB_tb, RSTC_tb, RSTCARRYIN_tb, RSTD_tb, RSTM_tb, RSTOPMODE_tb, RSTP_tb, /*Reset Input Ports:*/
     CLK_tb;
reg [47:0] PCIN_tb;
/*Operation outputs*/
wire [35:0] M_tb;
wire [47:0] P_tb;
wire [47:0] PCOUT_tb;
wire [17:0] BCOUT_tb;
wire CARRYOUT_tb;
wire CARRYOUTF_tb;


//Module instantiation
Spartan6_DSP48A1 DSP(
    .A(A_tb), .B(B_tb), .BCIN(BCIN_tb), .C(C_tb), .D(D_tb), .CARRYIN(CARRYIN_tb), .PCIN(PCIN_tb), .OPMODE(OPMODE_tb),   /*Operation Inputs*/
    .CEA(CEA_tb), .CEB(CEB_tb), .CEC(CEC_tb), .CECARRYIN(CECARRYIN_tb), .CED(CED_tb), .CEM(CEM_tb), .CEOPMODE(CEOPMODE_tb), .CEP(CEP_tb), /*Clock Enable Input Ports*/
    .RSTA(RSTA_tb), .RSTB(RSTB_tb), .RSTC(RSTC_tb), .RSTCARRYIN(RSTCARRYIN_tb), .RSTD(RSTD_tb), .RSTM(RSTM_tb), .RSTOPMODE(RSTOPMODE_tb), .RSTP(RSTP_tb), /*Reset Input Ports:*/
    .CLK(CLK_tb), .M(M_tb), .P(P_tb), .CARRYOUT(CARRYOUT_tb), .CARRYOUTF(CARRYOUTF_tb), .BCOUT(BCOUT_tb), .PCOUT(PCOUT_tb)   /*Operation Outputs*/
);

initial begin
     CLK_tb = 1;
     forever #1 CLK_tb =~ CLK_tb;
end

initial begin
```

```
initial begin
     //Reset the system
     CEA_tb = 1; CEB_tb = 1; CEC_tb = 1; CECARRYIN_tb = 1; CED_tb = 1; CEM_tb = 1; CEOPMODE_tb = 1; CEP_tb = 1; /*Clock Enable Input Ports*/
     RSTA_tb = 1; RSTB_tb = 1; RSTC_tb = 1; RSTCARRYIN_tb = 1; RSTD_tb = 1; RSTM_tb = 1; RSTOPMODE_tb = 1; RSTP_tb = 1;
     A_tb = 2; B_tb = 15; BCIN_tb = 55; D_tb = 78;
     CARRYIN_tb = 1;
     C_tb = 92;
     OPMODE_tb = 8'h6D;
     PCIN_tb = 15;
     @(negedge CLK_tb);
     RSTA_tb = 0; RSTB_tb = 0; RSTC_tb = 0; RSTCARRYIN_tb = 0; RSTD_tb = 0; RSTM_tb = 0; RSTOPMODE_tb = 0; RSTP_tb = 0;
     //Output value is ignored
     @(negedge CLK_tb);
     A_tb = 11; B_tb = 42; BCIN_tb = 87; D_tb = 100;
     //Output value is ignored
     @(negedge CLK_tb);
     A_tb = 3; B_tb = 42; BCIN_tb = 87; D_tb = 100;
     //Output value is ignored
     @(negedge CLK_tb);
     A_tb = 11; B_tb = 42; BCIN_tb = 87; D_tb = 100;
     C_tb = 92;
     OPMODE_tb = 8'hB7;
     PCIN_tb = 115;
     //Output value is 219
     @(negedge CLK_tb);
     A_tb = 10; B_tb = 42; BCIN_tb = 87; D_tb = 100;
     C_tb = 920;
     OPMODE_tb = 8'hAA;
     PCIN_tb = 15;
     //Output value is 14
     @(negedge CLK_tb);
     A_tb = 11; B_tb = 42; BCIN_tb = 87; D_tb = 100;
     C_tb = 92;
     OPMODE_tb = 8'h58;
     PCIN_tb = 15;
     //Output value is 0
     @(negedge CLK_tb);
     A_tb = 11; B_tb = 42; BCIN_tb = 87; D_tb = 100;
     C_tb = 92;
     OPMODE_tb = 8'hED;
     PCIN_tb = 15;
     //Output value is 1
     @(negedge CLK_tb);
     //Output value is 339
     $stop;
end
```

Waveform


Wave - Default
Msgs
CLK_tb 1'h1
A 18'd11
A0_Reg_Out 18'd11
A1_Reg_Out 18'd3
B 18'd42
Pre_Add_Sub_Out 18'd142
B1_Reg_In_mux_2... 18'd42
BCOUT 18'd58
C 48'd92
C_REG_Out 48'd92
D 18'd100
D_REG_Out 18'd100
Multiplier_Out 36'd174
M_REG_Out 36'd638
OPMODE_REG_Out 8'hb7
PCIN 48'd115
CARRYINREG_tb 1'h1
X_Mux_Out 48'd6871950557226
Z_Mux_Out 48'd115
Post_Add_Sub_Out -48'd6871950557112
P 48'd219
PCOUT 48'd219
CARRYOUT_tb 1'h0
CARRYOUTF_tb 1'h0
CARRYOUTREG_tb 1'h1


Wave - Default
Msgs
CLK_tb 1'h0
A 18'd10
A0_Reg_Out 18'd11
A1_Reg_Out 18'd3
B 18'd42
Pre_Add_Sub_Out 18'd142
B1_Reg_In_mux_2... 18'd42
BCOUT 18'd58
C 48'd920
C_REG_Out 48'd92
D 18'd100
D_REG_Out 18'd100
Multiplier_Out 36'd174
M_REG_Out 36'd638
OPMODE_REG_Out 8'hb7
PCIN 48'd15
CARRYINREG_tb 1'h1
X_Mux_Out 48'd6871950295082
Z_Mux_Out 48'd15
Post_Add_Sub_Out -48'd6871950295068
P 48'd219
PCOUT 48'd219
CARRYOUT_tb 1'h0
CARRYOUTF_tb 1'h0
CARRYOUTREG_tb 1'h1


Wave - Default
Msgs
CLK_tb 1'h1
A 18'd10
A0_Reg_Out 18'd10
A1_Reg_Out 18'd11
B 18'd42
Pre_Add_Sub_Out 18'd142
B1_Reg_In_mux_2... 18'd142
BCOUT 18'd42
C 48'd920
C_REG_Out 48'd920
D 18'd100
D_REG_Out 18'd100
Multiplier_Out 36'd462
M_REG_Out 36'd174
OPMODE_REG_Out 8'haa
PCIN 48'd15
CARRYINREG_tb 1'h1
X_Mux_Out -48'd6871950295068
Z_Mux_Out -48'd6871950295068
Post_Add_Sub_Out -48'd1
P -48'd6871950295068
PCOUT -48'd6871950295068
CARRYOUT_tb 1'h1
CARRYOUTF_tb 1'h1
CARRYOUTREG_tb 1'h1

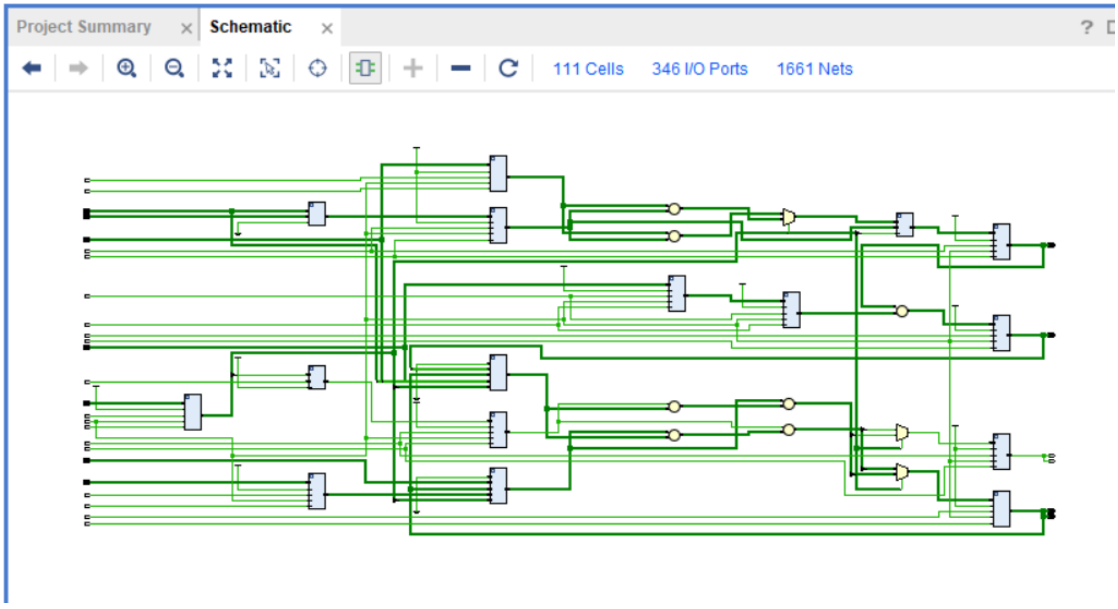
DO

Spartan6_DSP48A1_Do_file.do

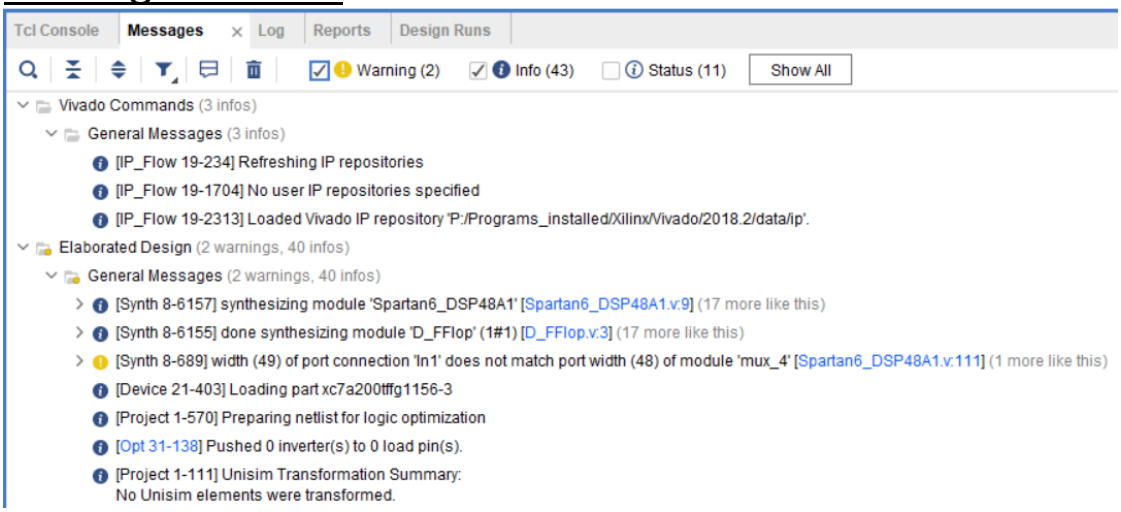
```
1   vlib work
2
3   vlog Spartan6_DSP48A1_tb.v Spartan6_DSP48A1.v mux_4.v mux_2.v D_FFlop.v D_FFlop_mux2.v
4
5   vsim -voptargs=+acc work.Sparatan6_DPS48A1_tb
6
7   add wave *
8
9   run -all
10
```

Elaboration

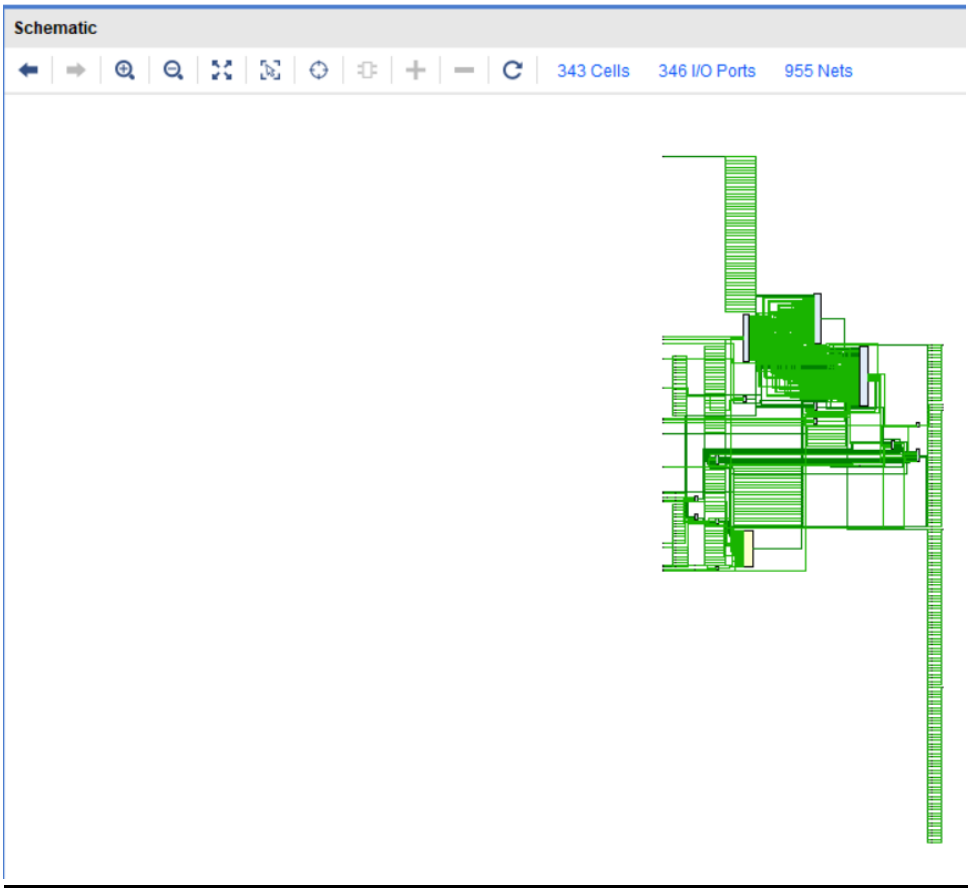
Schematic:



Message window



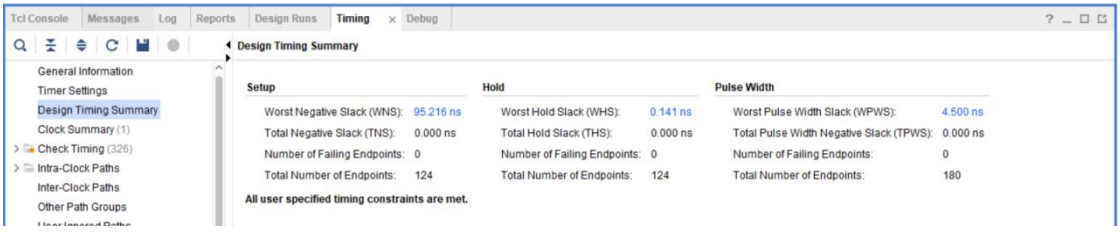
Synthesis

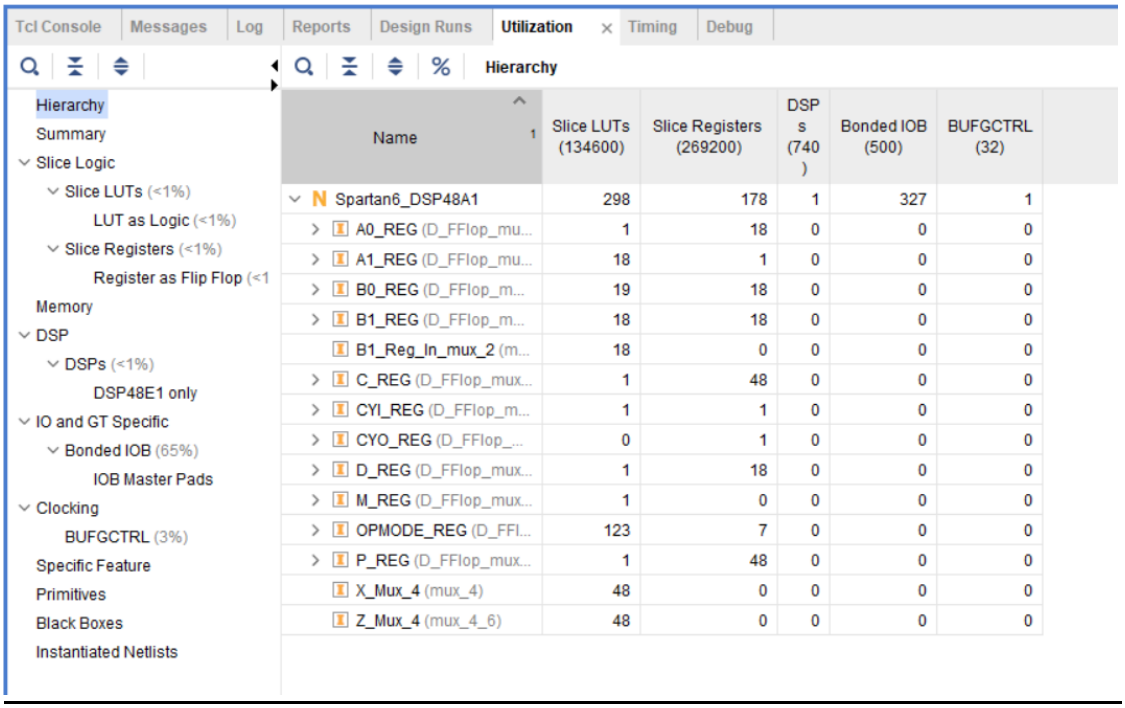


Tcl Console | Messages | Log | Reports | Design Runs | Debug

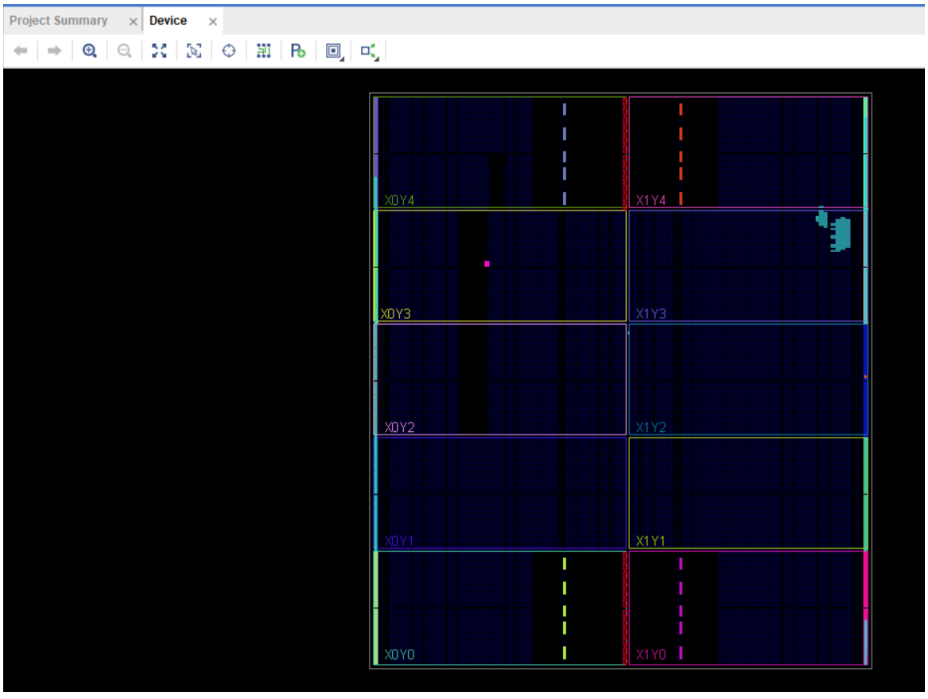
Warning (22) | Info (62) | Status (19) | Show All

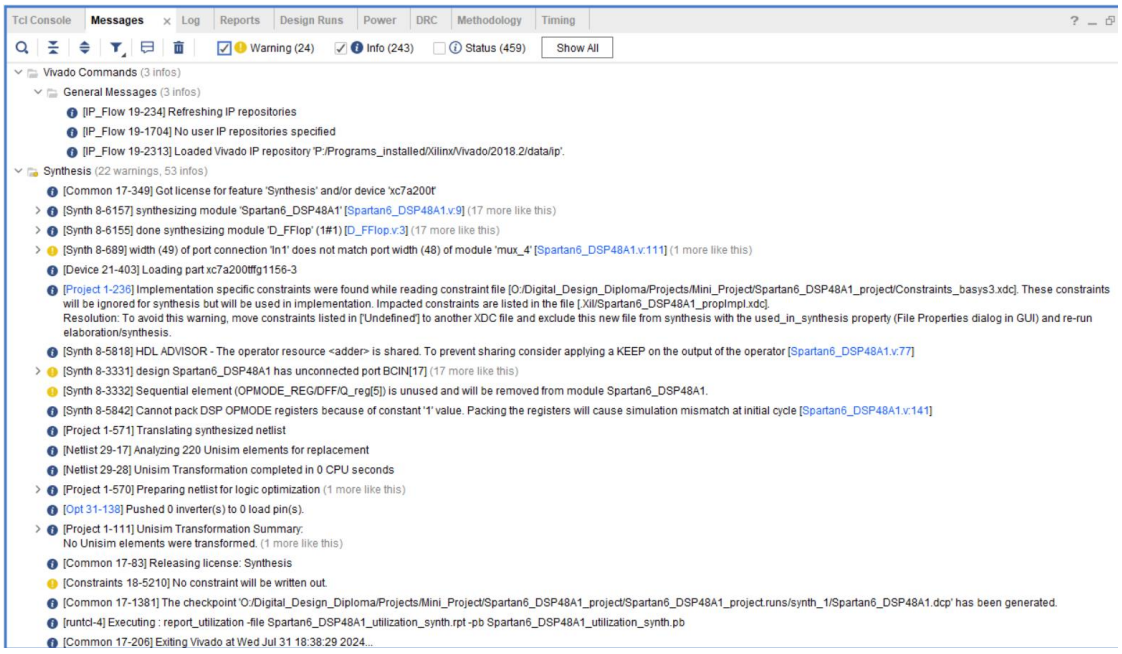
- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'P:/Programs_installed/Xilinx/Vivado/2018.2/data/ip'.
- Synthesis (22 warnings, 53 infos)
  - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
  - [Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [Spartan6_DSP48A1.v:9] (17 more like this)
  - [Synth 8-6155] done synthesizing module 'D_FFlop' (1#1) [D_FFlop.v:3] (17 more like this)
  - [Synth 8-689] width (49) of port connection 'In1' does not match port width (48) of module 'mux_4' [Spartan6_DSP48A1.v:111] (1 more like this)
  - [Device 21-403] Loading part xc7a200tffg1156-3
  - [Project 1-236] Implementation specific constraints were found while reading constraint file [O:/Digital_Design_Diploma/Projects/Mini_Project/Spartan6_DSP48A1_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Spartan6_DSP48A1_propImpl.xdc].
    Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  - [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [Spartan6_DSP48A1.v:77]
  - [Synth 8-3331] design Spartan6_DSP48A1 has unconnected port BCIN[17] (17 more like this)
  - [Synth 8-3332] Sequential element (OPMODE_REG/DFF/Q_reg[5]) is unused and will be removed from module Spartan6_DSP48A1.
  - [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [Spartan6_DSP48A1.v:141]
  - [Project 1-571] Translating synthesized netlist
  - [Netlist 29-17] Analyzing 220 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  - [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
  - [Common 17-83] Releasing license: Synthesis
  - [Constraints 18-5210] No constraint will be written out.
  - [Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Mini_Project/Spartan6_DSP48A1_project/Spartan6_DSP48A1_project.runs/synth_1/Spartan6_DSP48A1.dcp' has been generated.
  - [runtcl-4] Executing : report_utilization -file Spartan6_DSP48A1_utilization_synth.rpt -pb Spartan6_DSP48A1_utilization_synth.pb
  - [Common 17-206] Exiting Vivado at Wed Jul 31 18:38:29 2024...

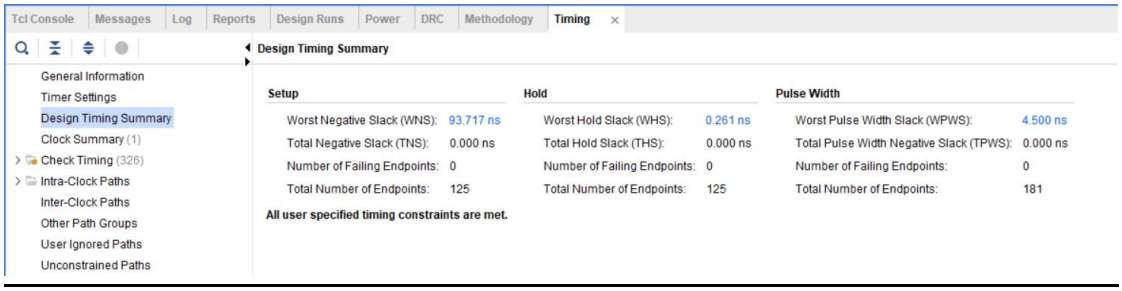

Tcl Console
Messages
Log
Reports
Design Runs
Timing
Debug
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Setup
Worst Negative Slack (WNS): 95.216 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 124
Hold
Worst Hold Slack (WHS): 0.141 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 124
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 180
All user specified timing constraints are met.

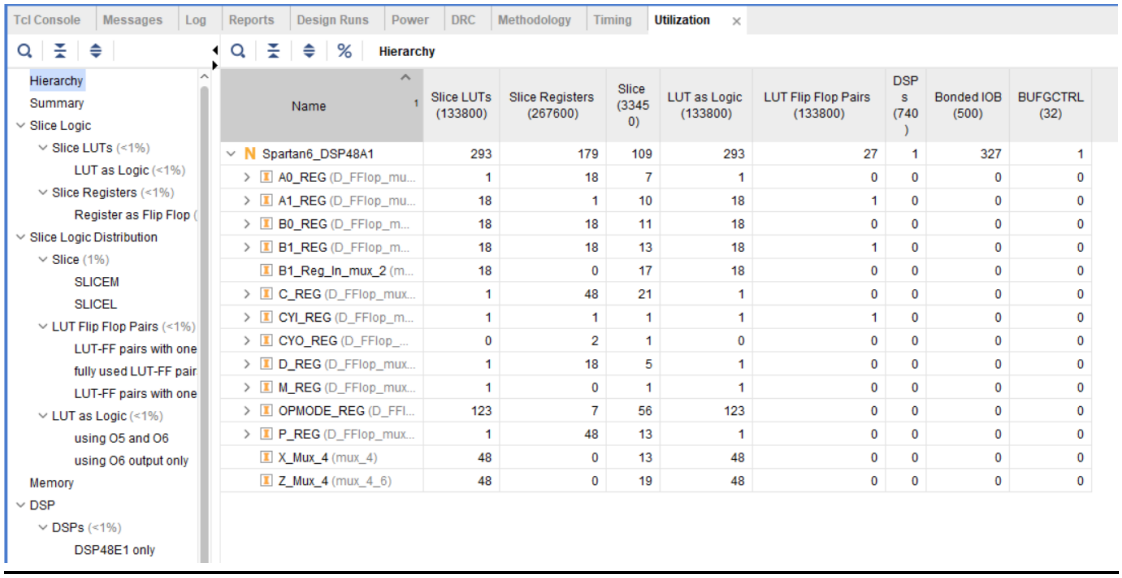

Tcl Console
Messages
Log
Reports
Design Runs
Utilization
Timing
Debug
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop (<1
Memory
DSP
DSPs (<1%)
DSP48E1 only
IO and GT Specific
Bonded IOB (65%)
IOB Master Pads
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists
Name
Slice LUTs (134600)
Slice Registers (269200)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
Spartan6_DSP48A1 298 178 1 327 1
A0_REG (D_FFlop_mu... 1 18 0 0 0
A1_REG (D_FFlop_mu... 18 1 0 0 0
B0_REG (D_FFlop_m... 19 18 0 0 0
B1_REG (D_FFlop_m... 18 18 0 0 0
B1_Reg_In_mux_2 (m... 18 0 0 0 0
C_REG (D_FFlop_mux... 1 48 0 0 0
CYI_REG (D_FFlop_m... 1 1 0 0 0
CYO_REG (D_FFlop_... 0 1 0 0 0
D_REG (D_FFlop_mux... 1 18 0 0 0
M_REG (D_FFlop_mux... 1 0 0 0 0
OPMODE_REG (D_FFl... 123 7 0 0 0
P_REG (D_FFlop_mux... 1 48 0 0 0
X_Mux_4 (mux_4) 48 0 0 0 0
Z_Mux_4 (mux_4_6) 48 0 0 0 0

Implement


Project Summary
Device
X0Y4
X1Y4
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Warning (24)
Info (243)
Status (459)
Show All
Vivado Commands (3 infos)
General Messages (3 infos)
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'P:/Programs_installed/Xilinx/Vivado/2018.2/data/ip'.
Synthesis (22 warnings, 53 infos)
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
[Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [Spartan6_DSP48A1.v:9] (17 more like this)
[Synth 8-6155] done synthesizing module 'D_FFlop' (1#1) [D_FFlop.v:3] (17 more like this)
[Synth 8-689] width (49) of port connection 'In1' does not match port width (48) of module 'mux_4' [Spartan6_DSP48A1.v:111] (1 more like this)
[Device 21-403] Loading part xc7a200tffg1156-3
[Project 1-236] Implementation specific constraints were found while reading constraint file [O:/Digital_Design_Diploma/Projects/Mini_Project/Spartan6_DSP48A1_project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Spartan6_DSP48A1_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
[Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [Spartan6_DSP48A1.v:77]
[Synth 8-3331] design Spartan6_DSP48A1 has unconnected port BCIN[17] (17 more like this)
[Synth 8-3332] Sequential element (OPMODE_REG/DFF/Q_reg[5]) is unused and will be removed from module Spartan6_DSP48A1.
[Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [Spartan6_DSP48A1.v:141]
[Project 1-571] Translating synthesized netlist
[Netlist 29-17] Analyzing 220 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-570] Preparing netlist for logic optimization (1 more like this)
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
[Common 17-83] Releasing license: Synthesis
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'O:/Digital_Design_Diploma/Projects/Mini_Project/Spartan6_DSP48A1_project/Spartan6_DSP48A1_project.runs/synth_1/Spartan6_DSP48A1.dcp' has been generated.
[runtcl-4] Executing : report_utilization -file Spartan6_DSP48A1_utilization_synth.rpt -pb Spartan6_DSP48A1_utilization_synth.pb
[Common 17-206] Exiting Vivado at Wed Jul 31 18:38:29 2024...


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): 93.717 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 125
Hold
Worst Hold Slack (WHS): 0.261 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 125
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 181
All user specified timing constraints are met.


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop
Slice Logic Distribution
Slice (1%)
SLICEM
SLICEL
LUT Flip Flop Pairs (<1%)
LUT-FF pairs with one
fully used LUT-FF pair
LUT-FF pairs with one
LUT as Logic (<1%)
using O5 and O6
using O6 output only
Memory
DSP
DSPs (<1%)
DSP48E1 only
Name
Slice LUTs (133800)
Slice Registers (267600)
Slice (33450)
LUT as Logic (133800)
LUT Flip Flop Pairs (133800)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
Spartan6_DSP48A1 293 179 109 293 27 1 327 1
A0_REG (D_FFlop_mu... 1 18 7 1 0 0 0 0
A1_REG (D_FFlop_mu... 18 1 10 18 1 0 0 0
B0_REG (D_FFlop_m... 18 18 11 18 0 0 0 0
B1_REG (D_FFlop_m... 18 18 13 18 1 0 0 0
B1_Reg_In_mux_2 (m... 18 0 17 18 0 0 0 0
C_REG (D_FFlop_mux... 1 48 21 1 0 0 0 0
CYI_REG (D_FFlop_m... 1 1 1 1 1 0 0 0
CYO_REG (D_FFlop_... 0 2 1 0 0 0 0 0
D_REG (D_FFlop_mux... 1 18 5 1 0 0 0 0
M_REG (D_FFlop_mux... 1 0 1 1 0 0 0 0
OPMODE_REG (D_FFl... 123 7 56 123 0 0 0 0
P_REG (D_FFlop_mux... 1 48 13 1 0 0 0 0
X_Mux_4 (mux_4) 48 0 13 48 0 0 0 0
Z_Mux_4 (mux_4_6) 48 0 19 48 0 0 0 0

Constraint file	Spartan6_DSP48A1_project > Constraints_basys3.xdc

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 100.00 -waveform {0 5} [get_ports CLK]


## Switches
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {A_N[0]}]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {A_N[1]}]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {A_N[2]}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {A_N[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {B_N[0]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {B_N[1]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {B_N[2]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {B_N[3]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {Opcode_N[0]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {Opcode_N[1]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {out[0]}]
#set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {out[1]}]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {out[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {out[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {out[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {out[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {out[6]}]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {out[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
#set_property -dict { PACKAGE_PIN V3    IOSTANDARD LVCMOS33 } [get_ports {led[9]}]
#set_property -dict { PACKAGE_PIN W3    IOSTANDARD LVCMOS33 } [get_ports {led[10]}]
#set_property -dict { PACKAGE_PIN U3    IOSTANDARD LVCMOS33 } [get_ports {led[11]}]
#set_property -dict { PACKAGE_PIN P3    IOSTANDARD LVCMOS33 } [get_ports {led[12]}]
#set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports {led[13]}]
#set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports {led[14]}]
#set_property -dict { PACKAGE_PIN L1    IOSTANDARD LVCMOS33 } [get_ports {led[15]}]

```