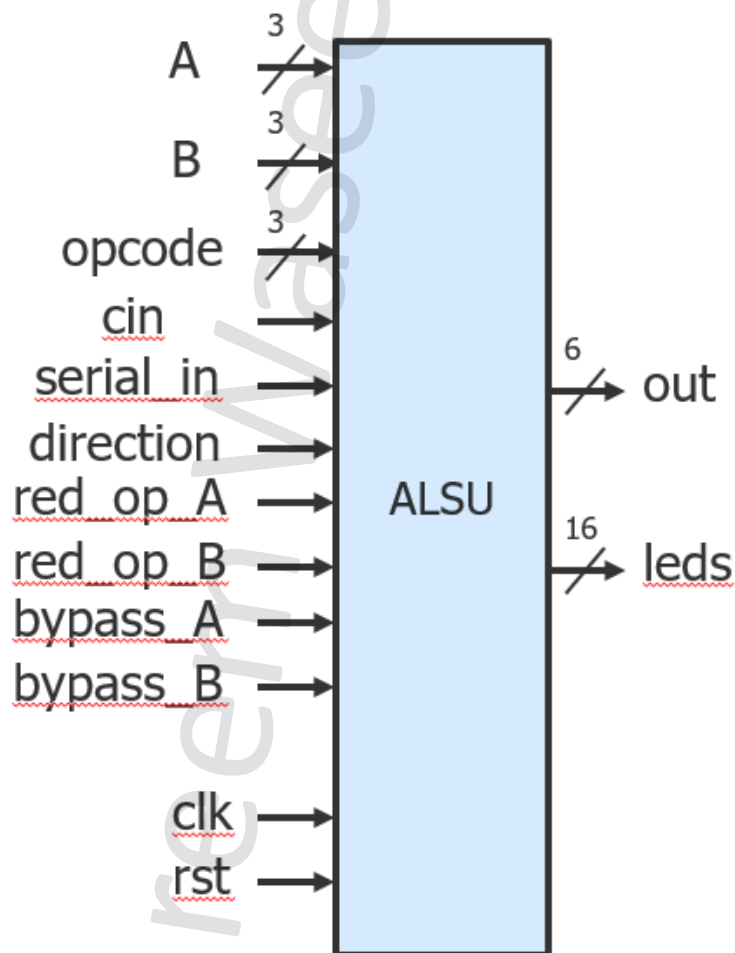


Q3.

ALSU is a logic unit that can perform logical, arithmetic, and shift operations on input ports

- Input ports A and B have various operations that can take place depending on the value of the opcode.
- Each input bit except for the clk and rst will be sampled at the rising edge before any processing so a D-FF is expected for each input bit at the design entry.
- The output of the ALSU is registered and is available at the rising edge of the clock.



Inputs

Each input bit except for the clk and rst will have a DFF in front of its port. Any processing will take place from the DFF output.

| Input | Width | Description |
|-----------|-------|--|
| clk | 1 | Input clock |
| rst | 1 | Active high asynchronous reset |
| A | 3 | Input port A |
| B | 3 | Input port B |
| cin | 1 | Carry in bit, only valid to be used if the parameter FULL_ADDER is "ON" |
| serial_in | 1 | Serial in bit, used in shift operations only |
| red_op_A | 1 | When set to high, this indicates that reduction operation would be executed on A rather than bitwise operations on A and B when the opcode indicates OR and XOR operations |
| red_op_B | 1 | When set to high, this indicates that reduction operation would be executed on B rather than bitwise operations on A and B when the opcode indicates OR and XOR operations |
| opcode | 3 | Opcode has a separate table to describe the different operations executed |
| bypass_A | 1 | When set to high, this indicates that port A will be registered to the output ignoring the opcode operation |
| bypass_B | 1 | When set to high, this indicates that port B will be registered to the output ignoring the opcode operation |
| direction | 1 | The direction of the shift or rotation operation is left when this input is set to high; otherwise, it is right. |

Outputs and parameters

| Output | Width | Description |
|--------|-------|---|
| leds | 16 | When an invalid operation occurs, all bits blink (bits turn on and then off with each clock cycle). Blinking serves as a warning; otherwise, if a valid operation occurs, it is set to low. |
| out | 6 | Output of the ALSU |

| Parameter | Default value | Description |
|----------------|---------------|---|
| INPUT_PRIORITY | A | Priority is given to the port set by this parameter whenever there is a conflict. Conflicts can occur in two scenarios, red_op_A and red_op_B are both set to high or bypass_A and bypass_B are both set to high. Legal values for this parameter are A and B |
| FULL_ADDER | ON | When this parameter has value "ON" then cin input must be considered in the addition operation between A and B. Legal values for this parameter are ON and OFF |

Opcodes & Handling invalid cases

Invalid cases

1. Opcode bits are set to 110 or 111
2. red_op_A or red_op_B are set to high and the opcode is not OR or XOR operation

Output when invalid cases occurs

1. leds are blinking
2. out bits are set to low

| Opcode | Operation |
|--------|---------------------------------|
| 000 | OR |
| 001 | XOR |
| 010 | ADD |
| 011 | MULT |
| 100 | SHIFT (Shift output by 1 bit) |
| 101 | ROTATE (Rotate output by 1 bit) |
| 110 | Invalid opcode |
| 111 | Invalid opcode |