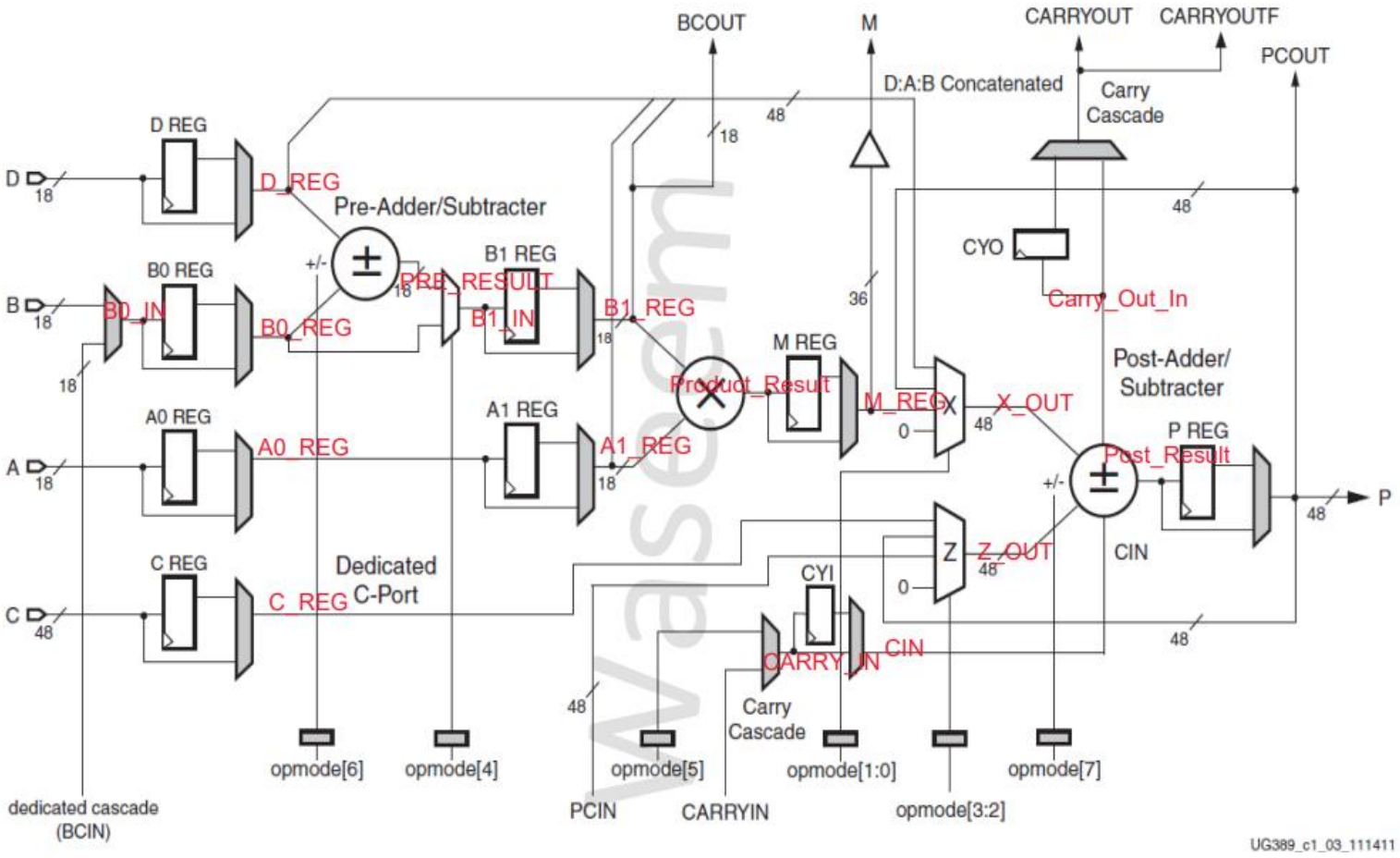
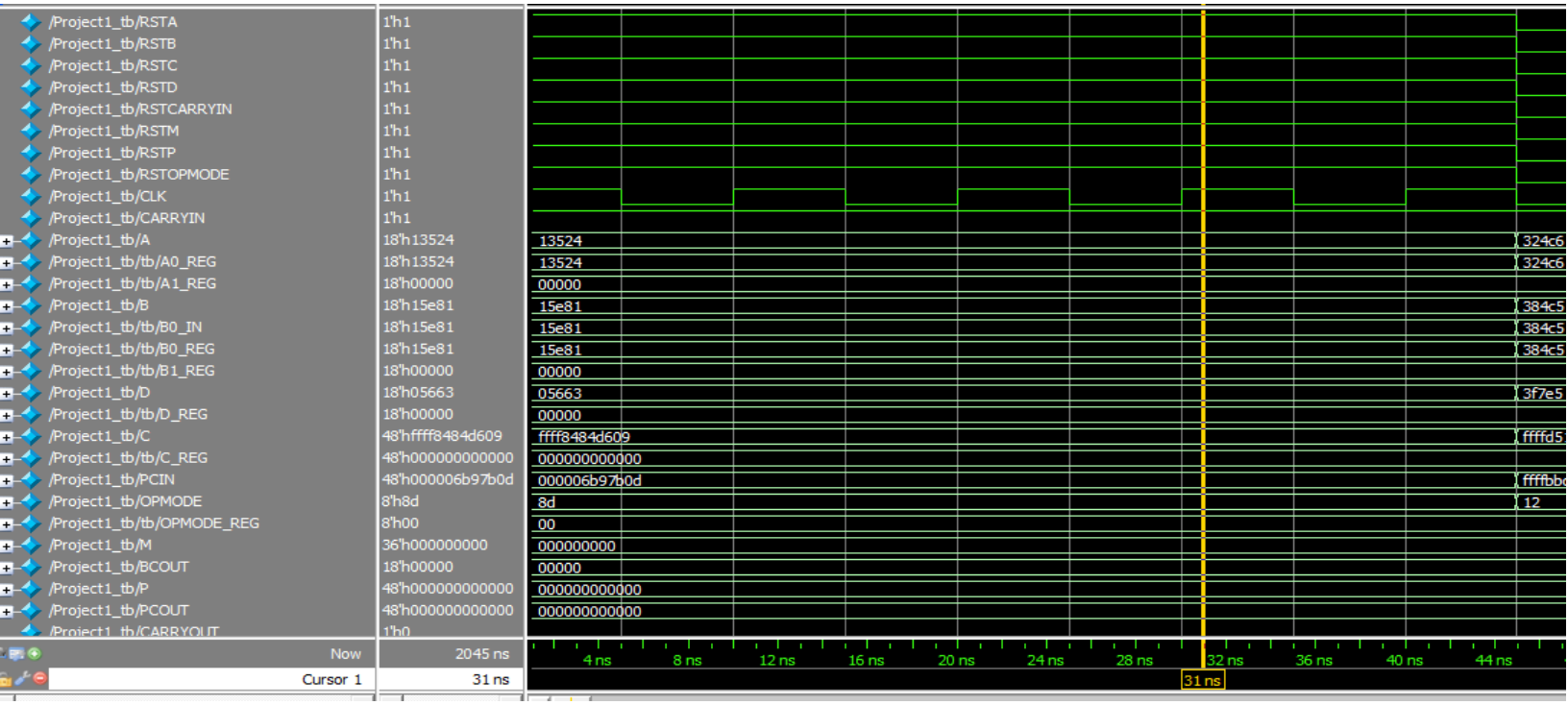
The following Is the spartan6 dsp48a1 with the internal signals used in the design labeled on it:



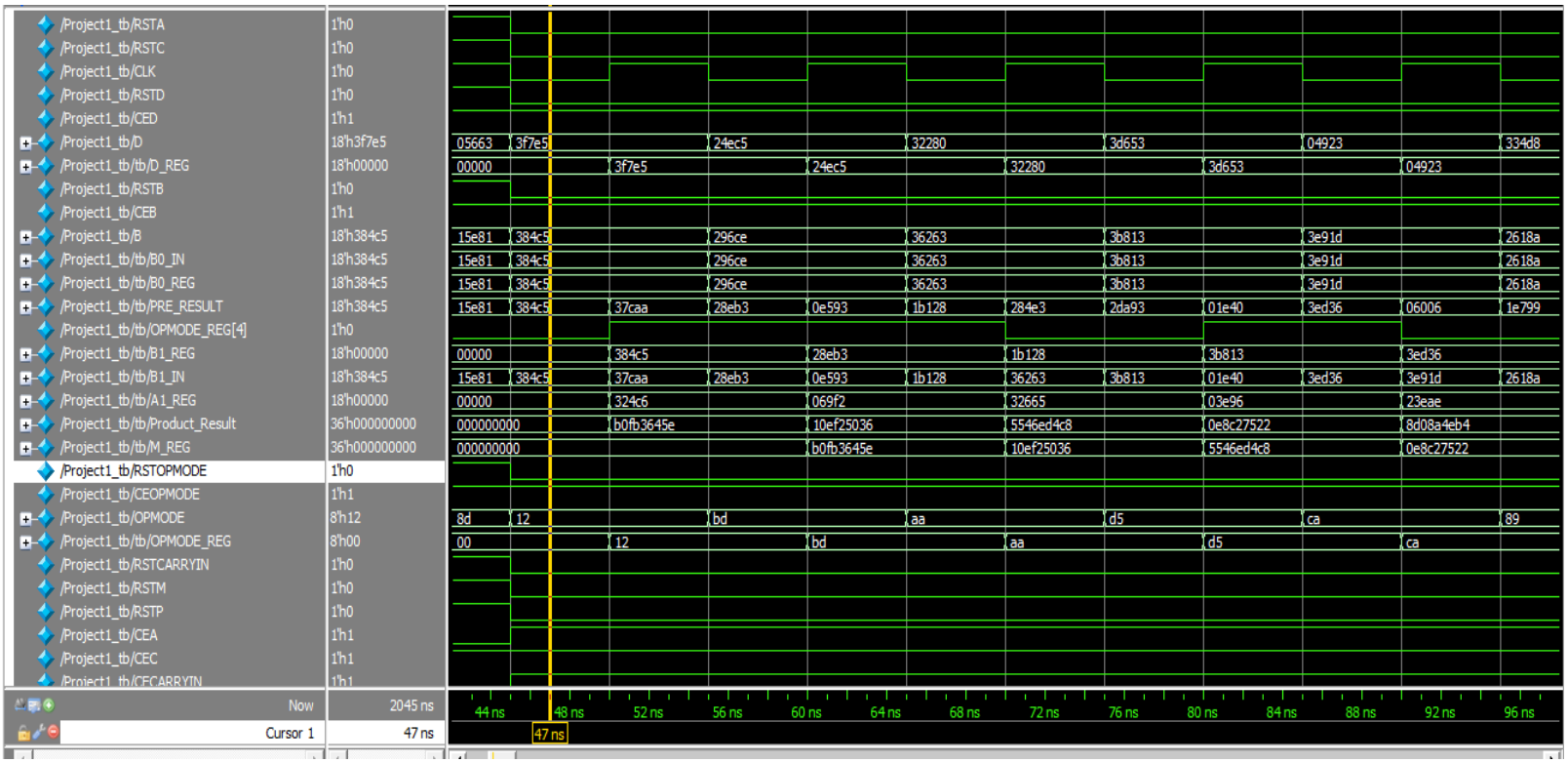
QuestaSim Waveform Results (Using Default Values):

Reset Test:

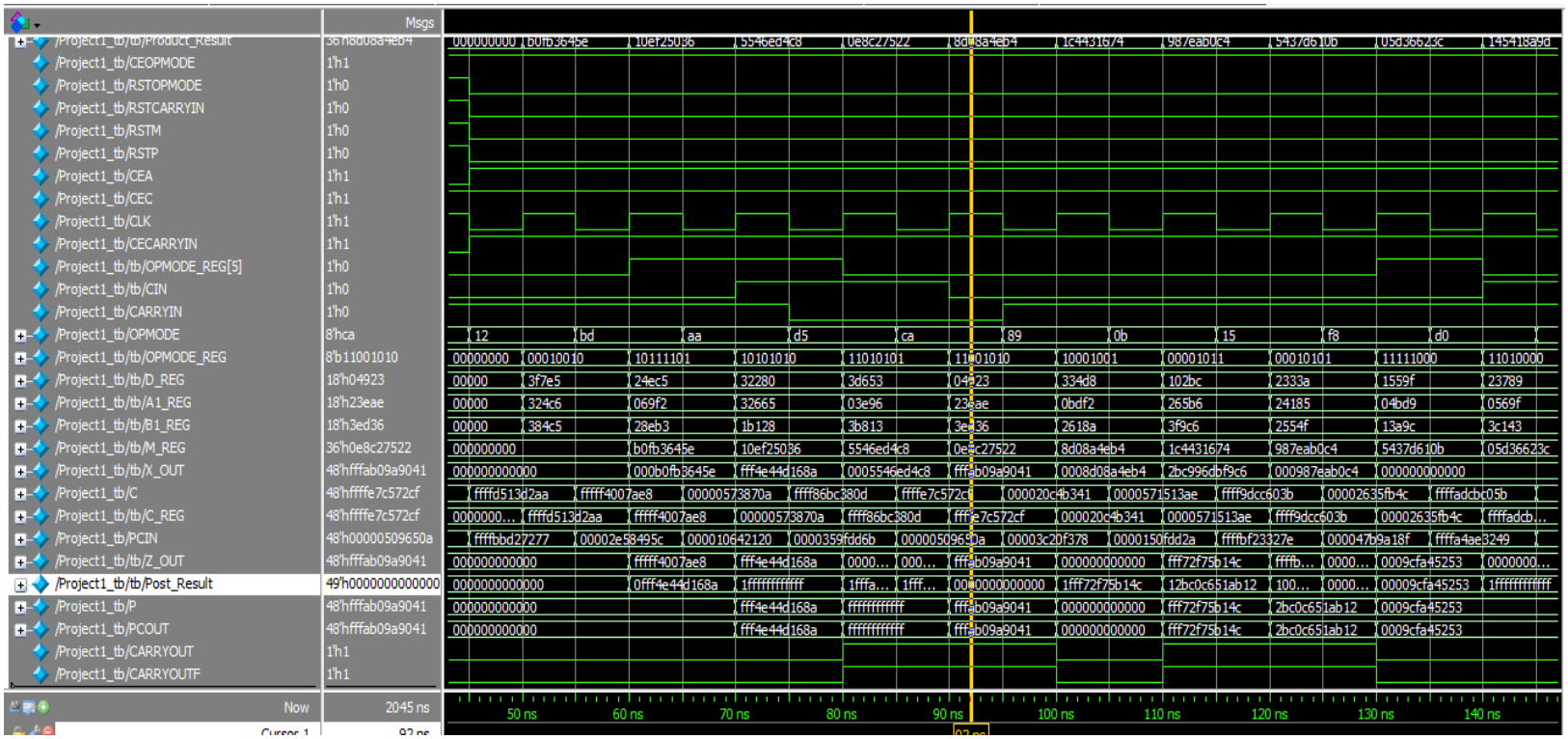


High CLOCK Enable Operation Test:

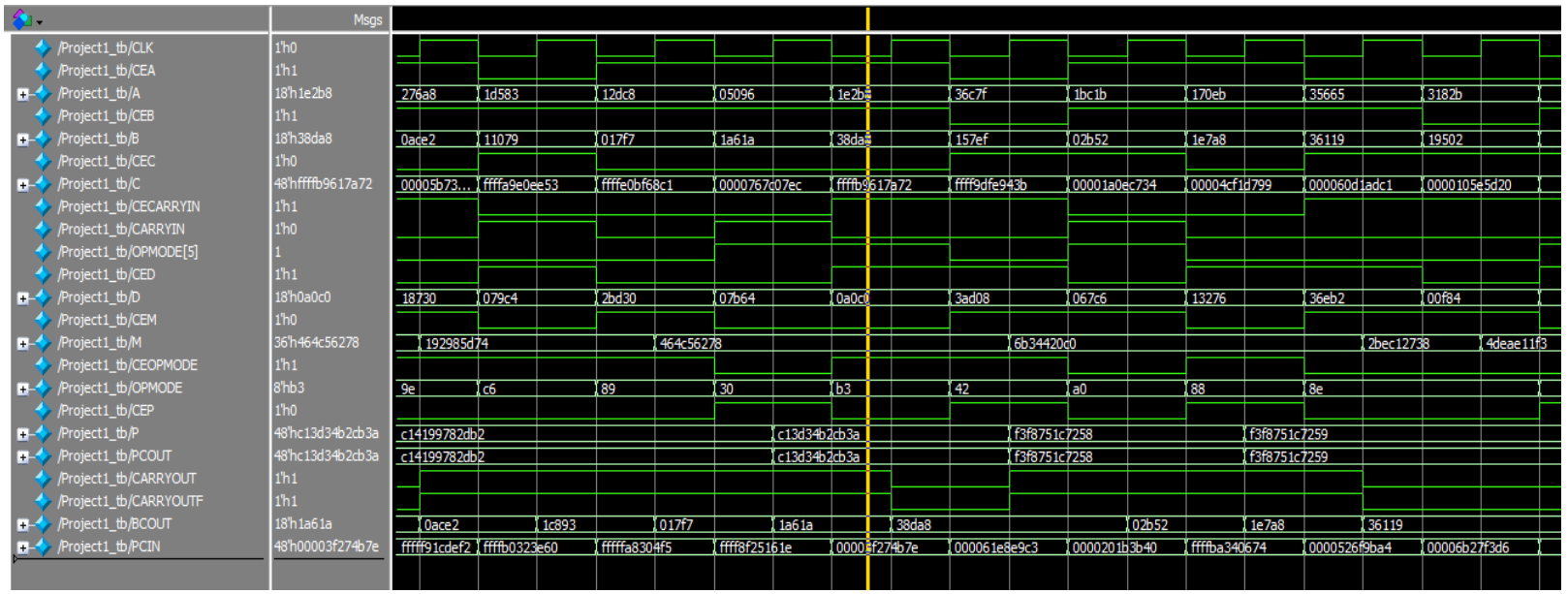
-Addition and Multiplication Operation:



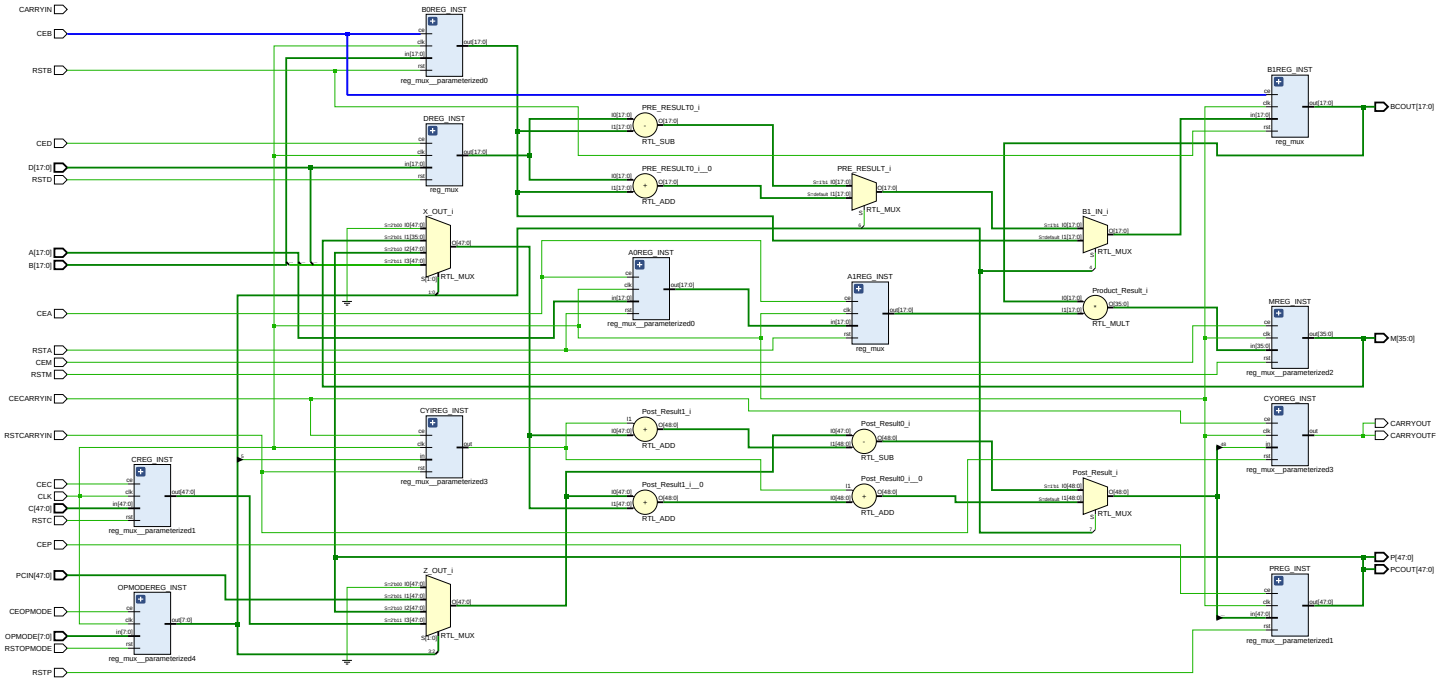
Z and X Multiplexers Operations, The Post adder, The carries and P Register Operations:



Testing the Ports Clock Enables:



The Elaborated Design Using Xilinx Vivado tool:


CARRYIN
CEB
RSTB
CED
D[17:0]
RSTD
A[17:0]
B[17:0]
CEA
RSTA
CEM
RSTM
CECARRYIN
RSTCARRYIN
CEC
CLK
C[47:0]
RSTC
CEP
PCIN[47:0]
CEOPMODE
OPMODE[7:0]
RSTOPMODE
RSTP
BOREG_INST
reg_mux__parameterized0
DREG_INST
reg_mux
X_OUT_i
RTL_MUX
PRE_RESULT0_i
RTL_SUB
PRE_RESULT0_i__0
RTL_ADD
PRE_RESULT_i
RTL_MUX
AOREG_INST
reg_mux__parameterized0
A1REG_INST
reg_mux
B1_IN_i
RTL_MUX
Product_Result_i
RTL_MULT
B1REG_INST
reg_mux
BCOUT[17:0]
MREG_INST
reg_mux__parameterized2
M[35:0]
CYOREG_INST
reg_mux__parameterized3
CARRYOUT
CARRYOUTF
CYIREG_INST
reg_mux__parameterized3
Post_Result1_i
RTL_ADD
Post_Result0_i
RTL_SUB
Post_Result1_i__0
RTL_ADD
Post_Result0_i__0
RTL_ADD
Post_Result_i
RTL_MUX
CREG_INST
reg_mux__parameterized1
OPMODEREG_INST
reg_mux__parameterized4
Z_OUT_i
RTL_MUX
PREG_INST
reg_mux__parameterized1
P[47:0]
PCOUT[47:0]