FIFO

Objective: Verify the given buggy Design by fixing all its bugs and reporting them.

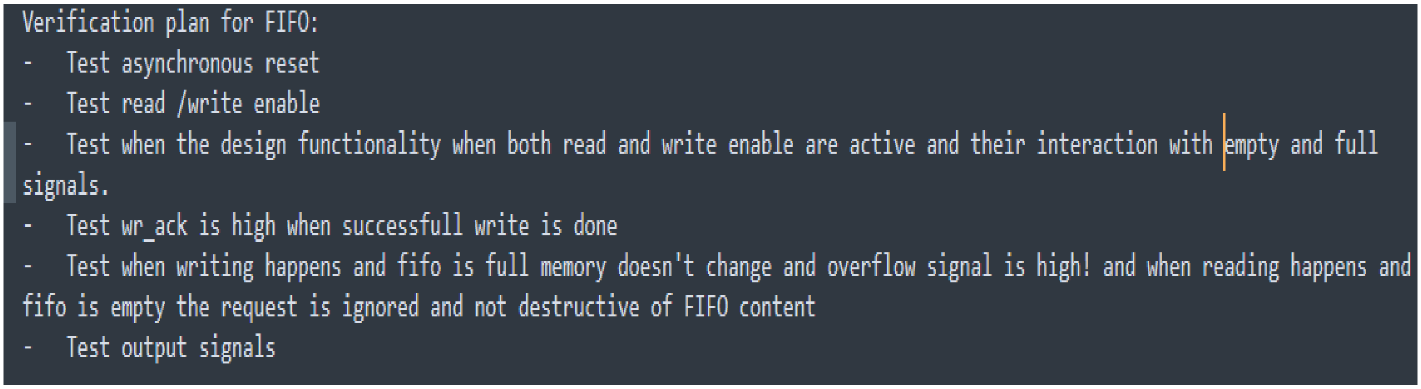
Parameters

- FIFO_WIDTH: DATA in/out and memory word width (default: 16)
- FIFO_DEPTH: Memory depth (default: 32)

Ports

Port	Direction	Function
data_in	Input	Write Data: The input data bus used when writing the FIFO.
wr_en		Write Enable: If the FIFO is not full, asserting this signal causes data (on data_in) to be written into the FIFO
rd_en		Read Enable: If the FIFO is not empty, asserting this signal causes data (on data_out) to be read from the FIFO
clk		Clock signal
rst_n		Active low asynchronous reset
data_out	Output	Read Data: The sequential output data bus used when reading from the FIFO.
full		Full Flag: When asserted, this combinational output signal indicates that the FIFO is full. Write requests are ignored when the FIFO is full, initiating a write when the FIFO is full is not destructive to the contents of the FIFO.
almostfull		Almost Full: When asserted, this combinational output signal indicates that only one more write can be performed before the FIFO is full.
empty		Empty Flag: When asserted, this combinational output signal indicates that the FIFO is empty. Read requests are ignored when the FIFO is empty, initiating a read while empty is not destructive to the FIFO.
almostempty		Almost Empty: When asserted, this output combinational signal indicates that only one more read can be performed before the FIFO goes to empty.
overflow		Overflow: This sequential output signal indicates that a write request (wr_en) was rejected because the FIFO is full. Overflowing the FIFO is not destructive to the contents of the FIFO.
underflow		Underflow: This sequential output signal Indicates that the read request (rd_en) was rejected because the FIFO is empty. Under flowing the FIFO is not destructive to the FIFO.
wr_ack	Output	Write Acknowledge: This sequential output signal indicates that a write request (wr_en) has succeeded.

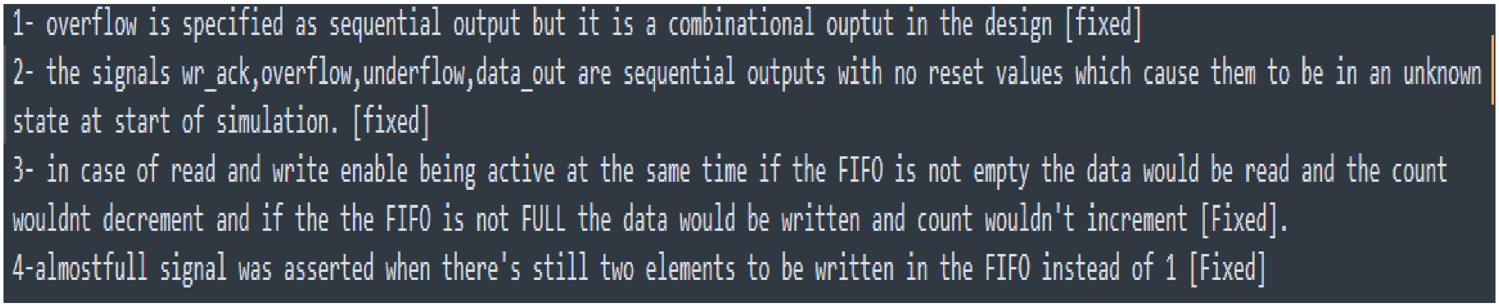
Verification Plan:



Verification plan for FIFO:

- Test asynchronous reset
- Test read /write enable
- Test when the design functionality when both read and write enable are active and their interaction with empty and full signals.
- Test wr_ack is high when successfull write is done
- Test when writing happens and fifo is full memory doesn't change and overflow signal is high! and when reading happens and fifo is empty the request is ignored and not destructive of FIFO content
- Test output signals

Bug Report



1- overflow is specified as sequential output but it is a combinational ouptut in the design [fixed]

2- the signals wr_ack,overflow,underflow,data_out are sequential outputs with no reset values which cause them to be in an unknown state at start of simulation. [fixed]

3- in case of read and write enable being active at the same time if the FIFO is not empty the data would be read and the count wouldnt decrement and if the the FIFO is not FULL the data would be written and count wouldn't increment [Fixed].

4-almostfull signal was asserted when there's still two elements to be written in the FIFO instead of 1 [Fixed]

Assertion Features:

Feature	Assertion
When FIFO is full then only Full signal should be high	@(posedge clk) disable iff(~rst_n) count==FIFO_DEPTH |-> (full && ~empty && ~almostempty && ~almostfull)
When FIFO is almost full then only almost full signal should be high	@(posedge clk) disable iff(~rst_n) count==(FIFO_DEPTH-1) |-> (almostfull && ~full && ~empty && ~almostempty)
When FIFO is almost empty then only almost empty signal should be high	@(posedge clk) disable iff(~rst_n) count==1 |-> (almostempty && ~full && ~empty && ~almostfull)
When FIFO is empty then only empty signal should be high	@(posedge clk) disable iff(~rst_n) count==0 |-> (empty && ~full && ~almostempty && ~almostfull)
When FIFO is Full and a write request happens then overflow should be high	@(posedge clk) disable iff(~rst_n) (full && wr_en) |=> (overflow)
When FIFO is empty and a write request happens then underflow should be high	@(posedge clk) disable iff(~rst_n) (empty && rd_en) |=> (underflow)
Whenever FIFO is written then wr_ack should be high	@(posedge clk) disable iff(~rst_n) (wr_en && !full) |=> (wr_ack)
Assert FIFO element Counter incrementing functionality	logic[max_fifo_addr:0] old_count; @(posedge clk) disable iff(~rst_n) (wr_en && ~rd_en && ~full,old_count=count) |=> (count==old_count+1)
Assert FIFO element Counter no change functionality	@(posedge clk) disable iff(~rst_n) (wr_en && rd_en && ~full && ~empty) |=> $stable(count);
Assert FIFO element Counter decrementing functionality	logic[max_fifo_addr:0] old_count; @(posedge clk) disable iff(~rst_n) (~wr_en && rd_en && ~empty,old_count=count) |=> (count==old_count-1)

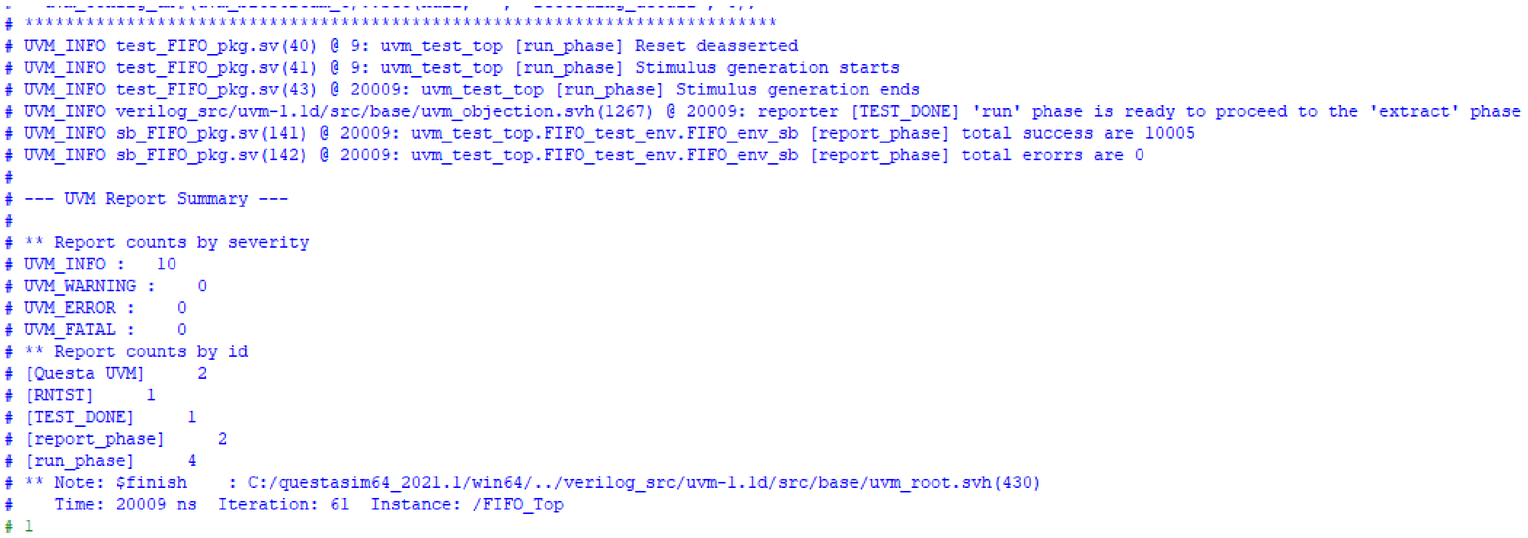
When FIFO is empty and read and write enables are high then element counter should increment	logic[max_fifo_addr:0] old_count;
	@(posedge clk) disable iff(~rst_n) (wr_en && rd_en && ~full && empty,old_count=count) |=> (count==old_count+1);

When FIFO is Full and read and write enables are high then element counter should decrement	logic[max_fifo_addr:0] old_count; @(posedge clk) disable iff(~rst_n) (wr_en && rd_en && full,old_count=count) |=> (count==old_count-1) ;
Read pointer should increase when FIFO is read	logic[$clog2(FIFO_DEPTH)-1:0] old_read; @(posedge clk) disable iff(~rst_n) (rd_en && ~empty,old_read=rd_ptr) |=> (rd_ptr==old_read+1'b1)

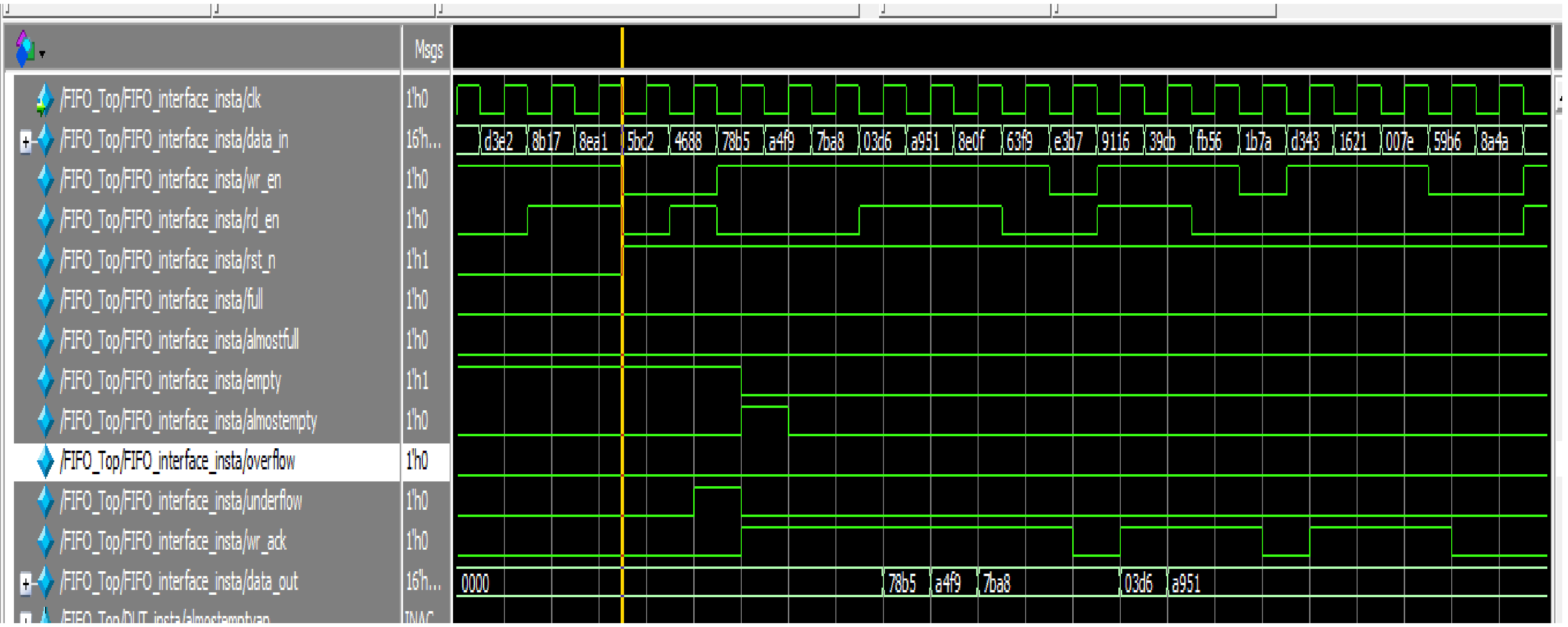
Write pointer should increase when FIFO is written	logic[$clog2(FIFO_DEPTH)-1:0] old_write;
	@(posedge clk) disable iff(~rst_n) (wr_en && ~full,old_write=wr_ptr) |=> (wr_ptr==old_write+1'b1);

Read pointer should not change if read enable is active but FIFO is empty	@(posedge clk) disable iff(~rst_n) (rd_en && empty) |=> $stable(rd_ptr);
Write pointer should not change if write enable is active but FIFO is empty	@(posedge clk) disable iff(~rst_n) (wr_en && full) |=> ($stable(wr_ptr));

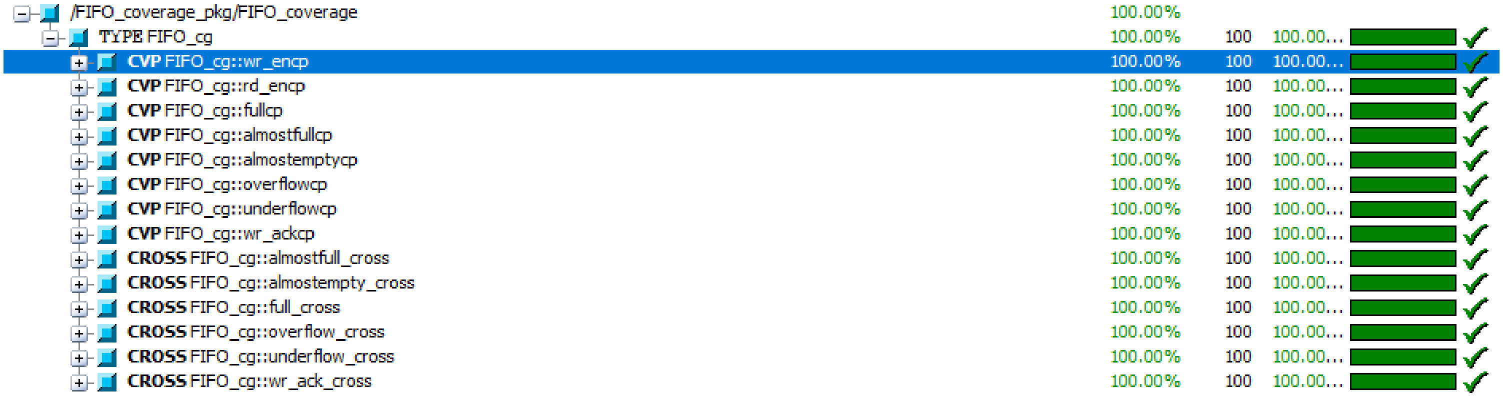
Questa Snippets:



```
# ***************************************************************************
# UVM_INFO test_FIFO_pkg.sv(40) @ 9: uvm_test_top [run_phase] Reset deasserted
# UVM_INFO test_FIFO_pkg.sv(41) @ 9: uvm_test_top [run_phase] Stimulus generation starts
# UVM_INFO test_FIFO_pkg.sv(43) @ 20009: uvm_test_top [run_phase] Stimulus generation ends
# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 20009: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# UVM_INFO sb_FIFO_pkg.sv(141) @ 20009: uvm_test_top.FIFO_test_env.FIFO_env_sb [report_phase] total success are 10005
# UVM_INFO sb_FIFO_pkg.sv(142) @ 20009: uvm_test_top.FIFO_test_env.FIFO_env_sb [report_phase] total erorrs are 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :   10
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [RNTST]     1
# [TEST_DONE]     1
# [report_phase]     2
# [run_phase]     4
# ** Note: $finish    : C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 20009 ns  Iteration: 61  Instance: /FIFO_Top
# 1
```

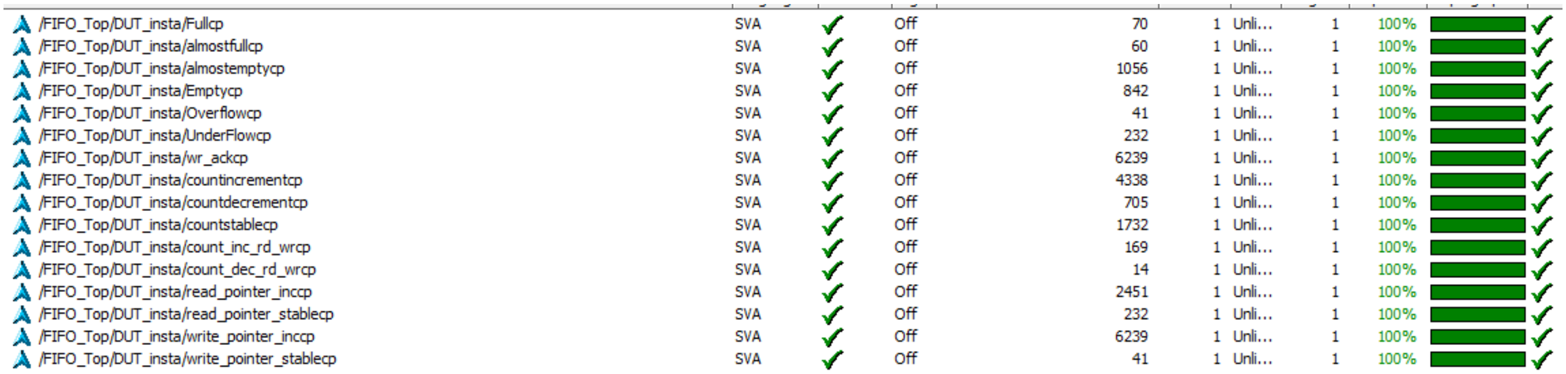

Msgs
/FIFO_Top/FIFO_interface_insta/clk 1'h0
/FIFO_Top/FIFO_interface_insta/data_in 16'h...
d3e2 8b17 8ea1 5bc2 4688 78b5 a4f9 7ba8 03d6 a951 8e0f 63f9 e3b7 9116 39db fb56 1b7a d343 1621 007e 59b6 8a4a
/FIFO_Top/FIFO_interface_insta/wr_en 1'h0
/FIFO_Top/FIFO_interface_insta/rd_en 1'h0
/FIFO_Top/FIFO_interface_insta/rst_n 1'h1
/FIFO_Top/FIFO_interface_insta/full 1'h0
/FIFO_Top/FIFO_interface_insta/almostfull 1'h0
/FIFO_Top/FIFO_interface_insta/empty 1'h1
/FIFO_Top/FIFO_interface_insta/almostempty 1'h0
/FIFO_Top/FIFO_interface_insta/overflow 1'h0
/FIFO_Top/FIFO_interface_insta/underflow 1'h0
/FIFO_Top/FIFO_interface_insta/wr_ack 1'h0
/FIFO_Top/FIFO_interface_insta/data_out 16'h...
0000 78b5 a4f9 7ba8 03d6 a951

Functional Coverage:

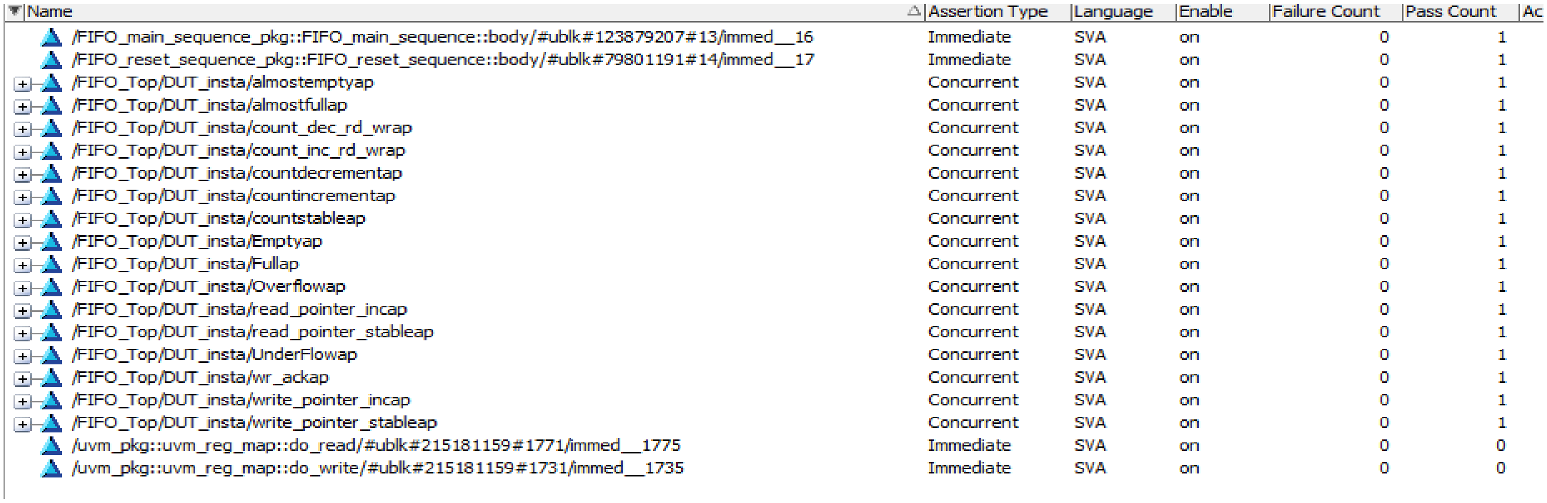


/FIFO_coverage_pkg/FIFO_coverage	100.00%				
TYPE FIFO_cg	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::wr_encp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::rd_encp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::fullcp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::almostfullcp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::almostemptycp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::overflowcp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::underflowcp	100.00%	100	100.00...	🟩	✓
CVP FIFO_cg::wr_ackcp	100.00%	100	100.00...	🟩	✓
CROSS FIFO_cg::almostfull_cross	100.00%	100	100.00...	🟩	✓
CROSS FIFO_cg::almostempty_cross	100.00%	100	100.00...	🟩	✓
CROSS FIFO_cg::full_cross	100.00%	100	100.00...	🟩	✓
CROSS FIFO_cg::overflow_cross	100.00%	100	100.00...	🟩	✓
CROSS FIFO_cg::underflow_cross	100.00%	100	100.00...	🟩	✓
CROSS FIFO_cg::wr_ack_cross	100.00%	100	100.00...	🟩	✓

Assertion Coverage:

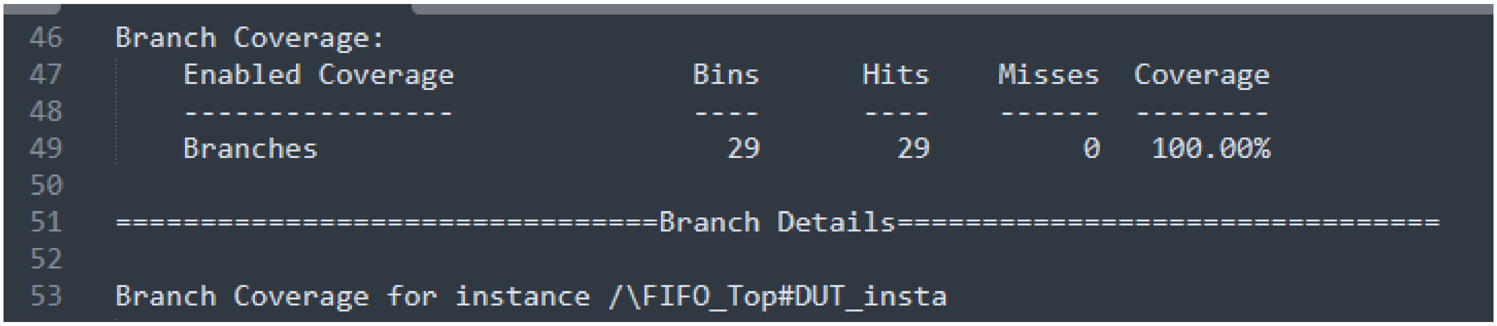


/FIFO_Top/DUT_insta/Fullcp	SVA	✓	Off	70	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/almostfullcp	SVA	✓	Off	60	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/almostemptycp	SVA	✓	Off	1056	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/Emptycp	SVA	✓	Off	842	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/Overflowcp	SVA	✓	Off	41	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/UnderFlowcp	SVA	✓	Off	232	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/wr_ackcp	SVA	✓	Off	6239	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/countincrementcp	SVA	✓	Off	4338	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/countdecrementcp	SVA	✓	Off	705	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/countstablecp	SVA	✓	Off	1732	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/count_inc_rd_wrcp	SVA	✓	Off	169	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/count_dec_rd_wrcp	SVA	✓	Off	14	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/read_pointer_inccp	SVA	✓	Off	2451	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/read_pointer_stablecp	SVA	✓	Off	232	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/write_pointer_inccp	SVA	✓	Off	6239	1	Unli...	1	100%	🟩	✓
/FIFO_Top/DUT_insta/write_pointer_stablecp	SVA	✓	Off	41	1	Unli...	1	100%	🟩	✓

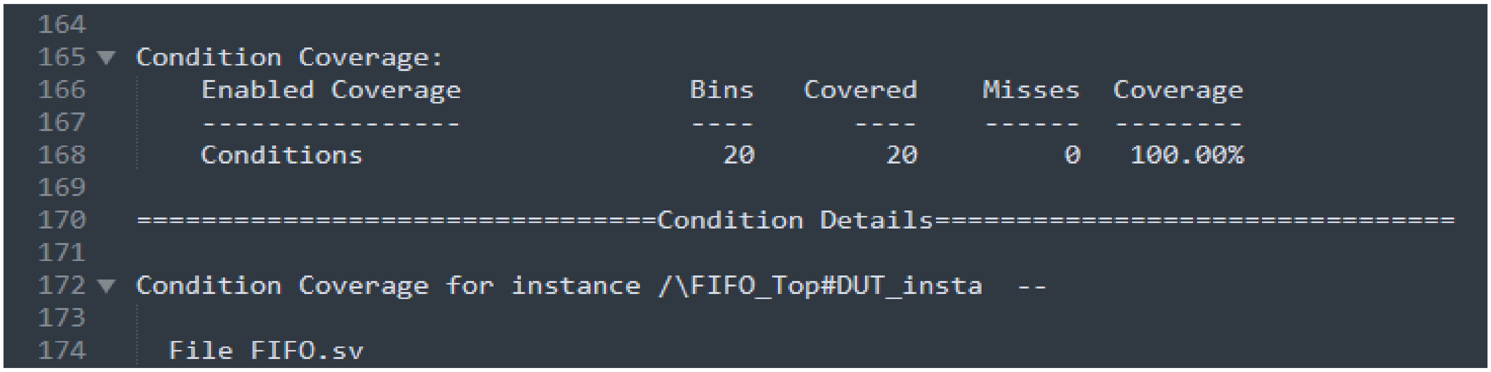


Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Ac
/FIFO_main_sequence_pkg::FIFO_main_sequence::body/#ublk#123879207#13/immed__16	Immediate	SVA	on	0	1	
/FIFO_reset_sequence_pkg::FIFO_reset_sequence::body/#ublk#79801191#14/immed__17	Immediate	SVA	on	0	1	
/FIFO_Top/DUT_insta/almostemptyap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/almostfullap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/count_dec_rd_wrap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/count_inc_rd_wrap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/countdecrementap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/countincrementap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/countstableap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/Emptyap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/Fullap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/Overflowap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/read_pointer_incap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/read_pointer_stableap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/UnderFlowap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/wr_ackap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/write_pointer_incap	Concurrent	SVA	on	0	1	
/FIFO_Top/DUT_insta/write_pointer_stableap	Concurrent	SVA	on	0	1	
/uvm_pkg::uvm_reg_map::do_read/#ublk#215181159#1771/immed__1775	Immediate	SVA	on	0	0	
/uvm_pkg::uvm_reg_map::do_write/#ublk#215181159#1731/immed__1735	Immediate	SVA	on	0	0	

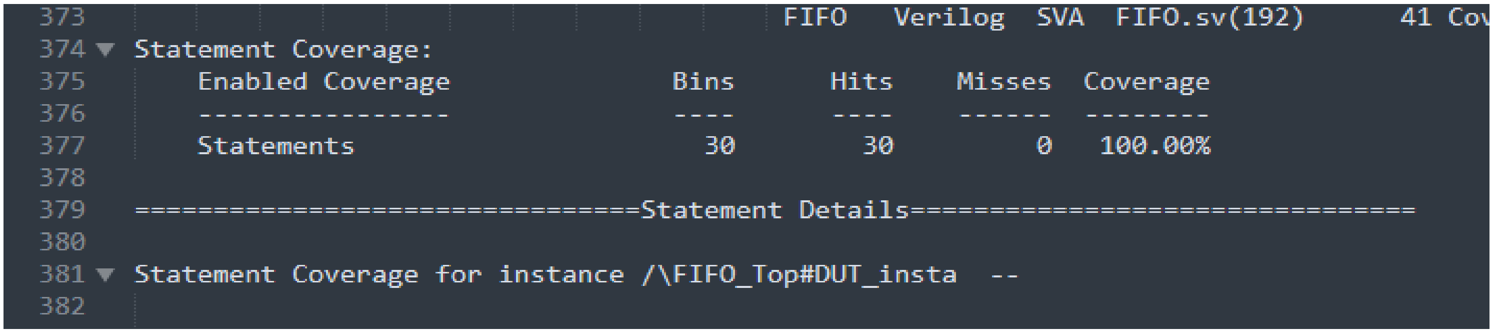
Code Coverage:



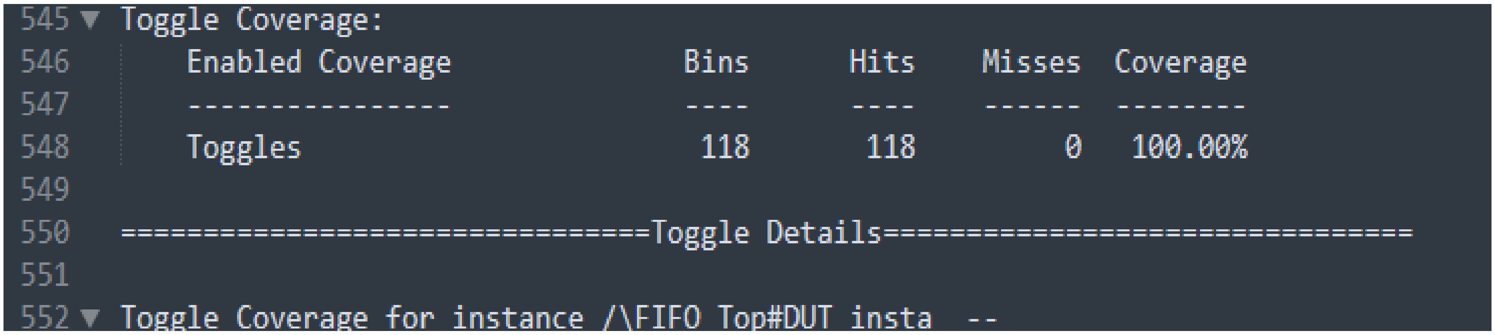
```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        29        29         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\FIFO_Top#DUT_insta
```



```
Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      20        20         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\FIFO_Top#DUT_insta  --

  File FIFO.sv
```



```
                                                FIFO   Verilog  SVA  FIFO.sv(192)      41 Cov
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      30        30         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\FIFO_Top#DUT_insta  --
```



```
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        118       118         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\FIFO Top#DUT insta  --
```