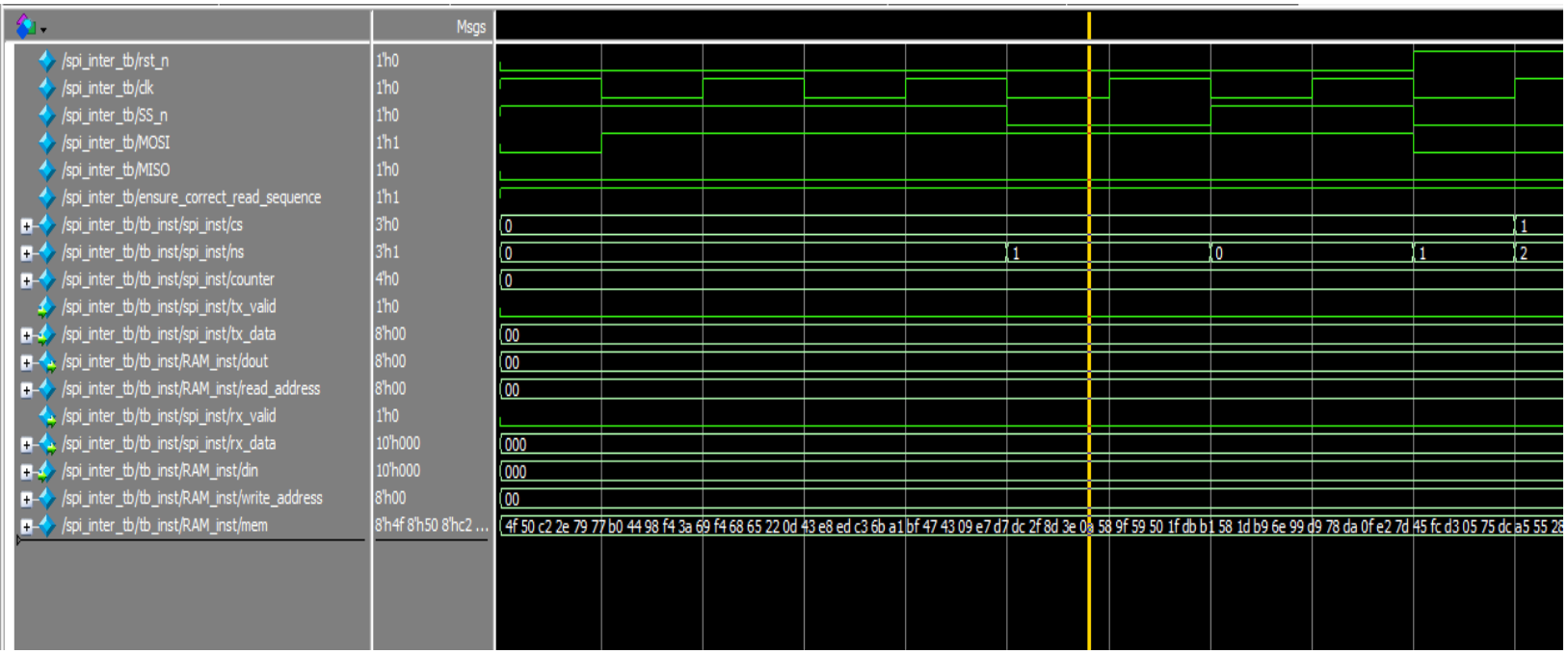
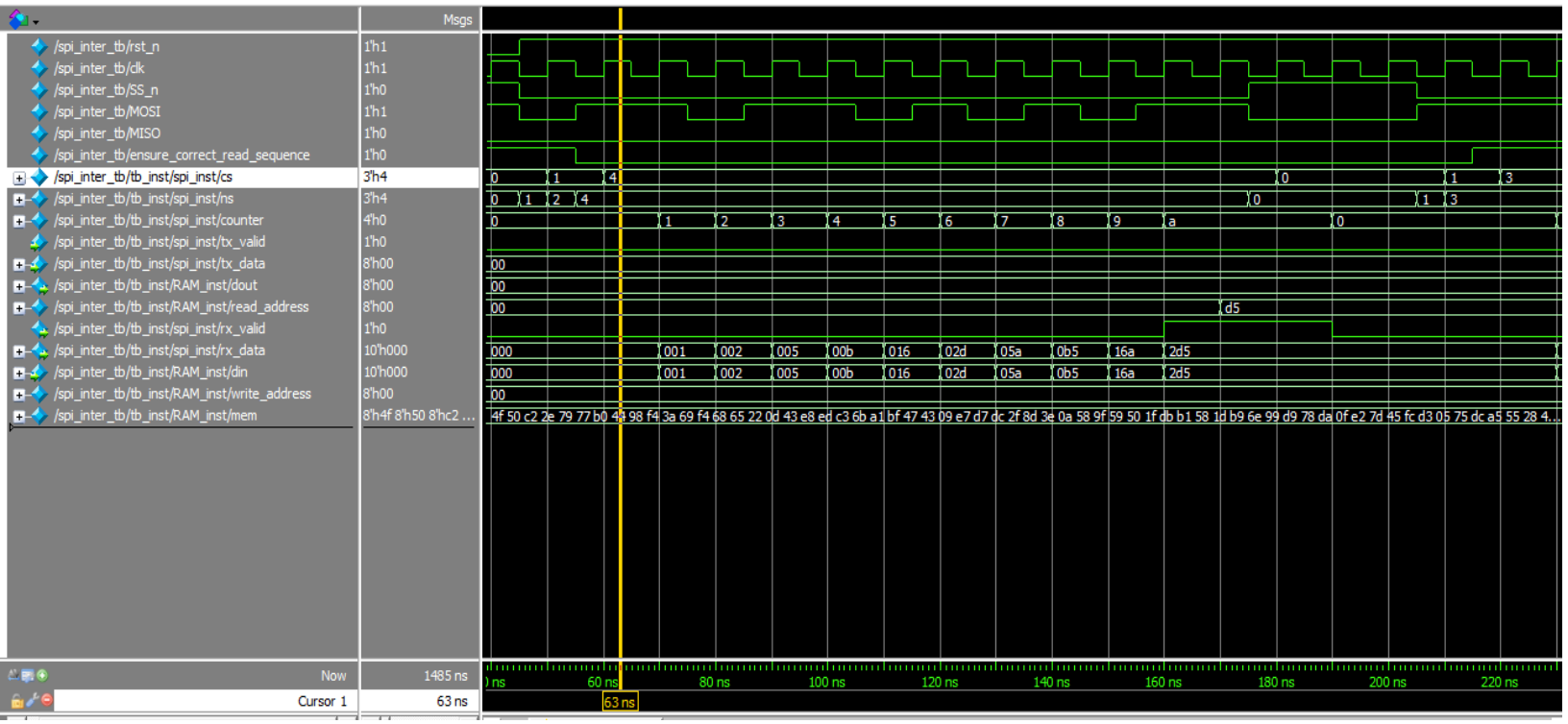
QuestaSim Snippets: [Sequential FSM encoding]

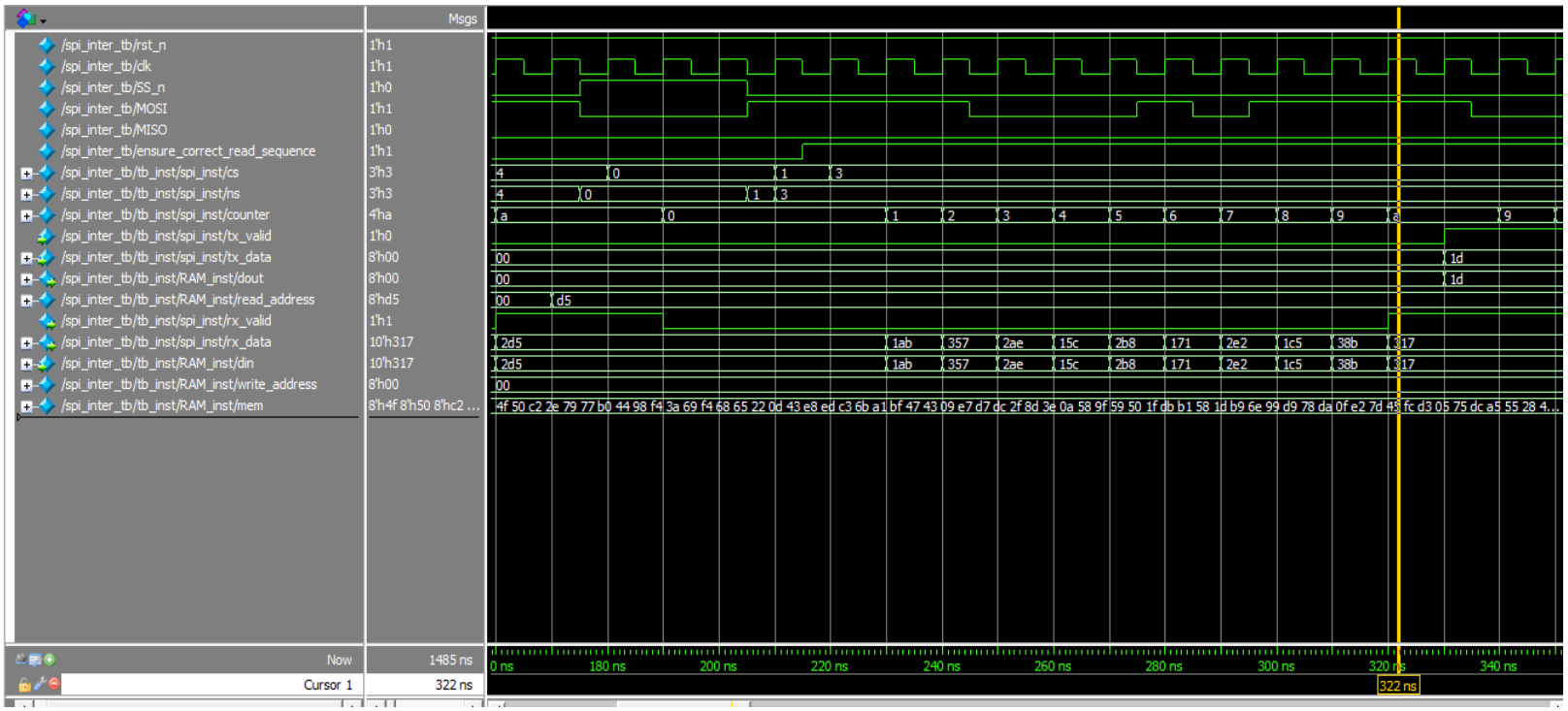
Testing Reset Functionality:



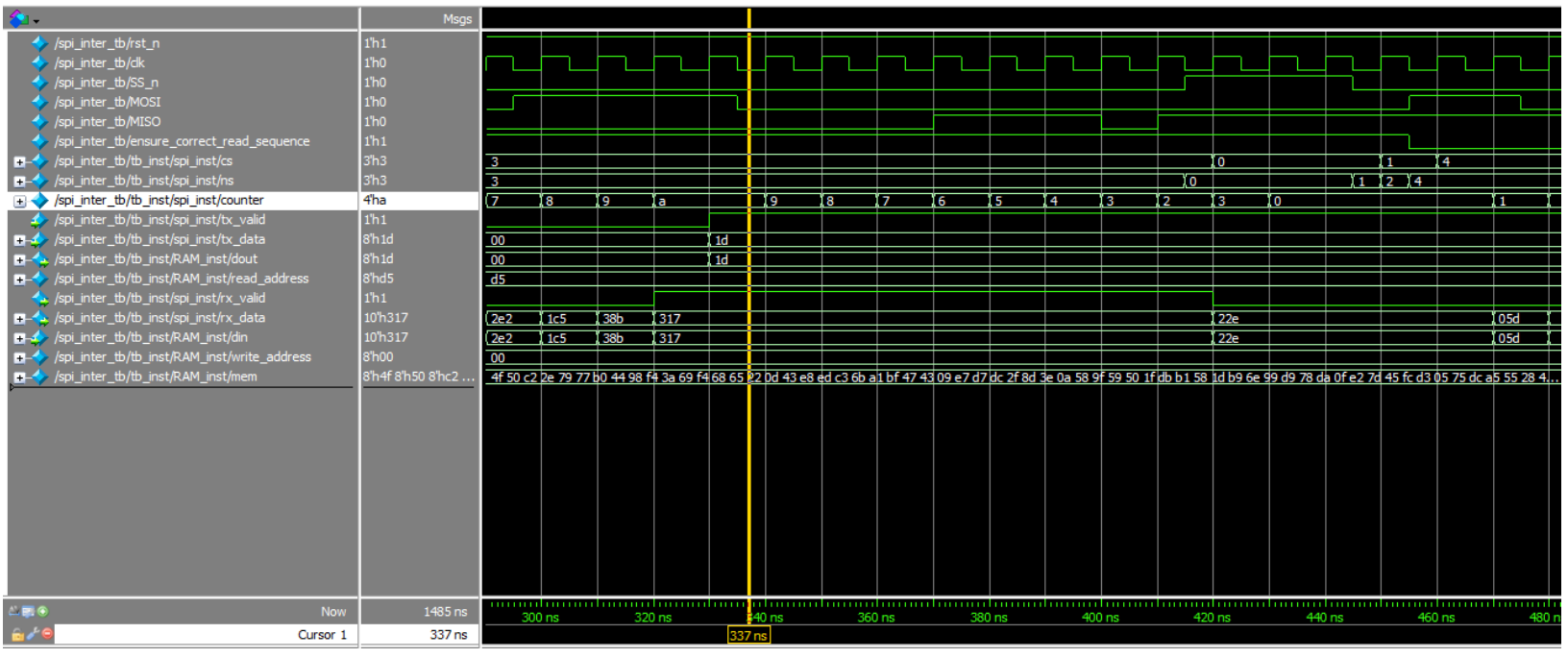
Testing Read Operation: first hold read address



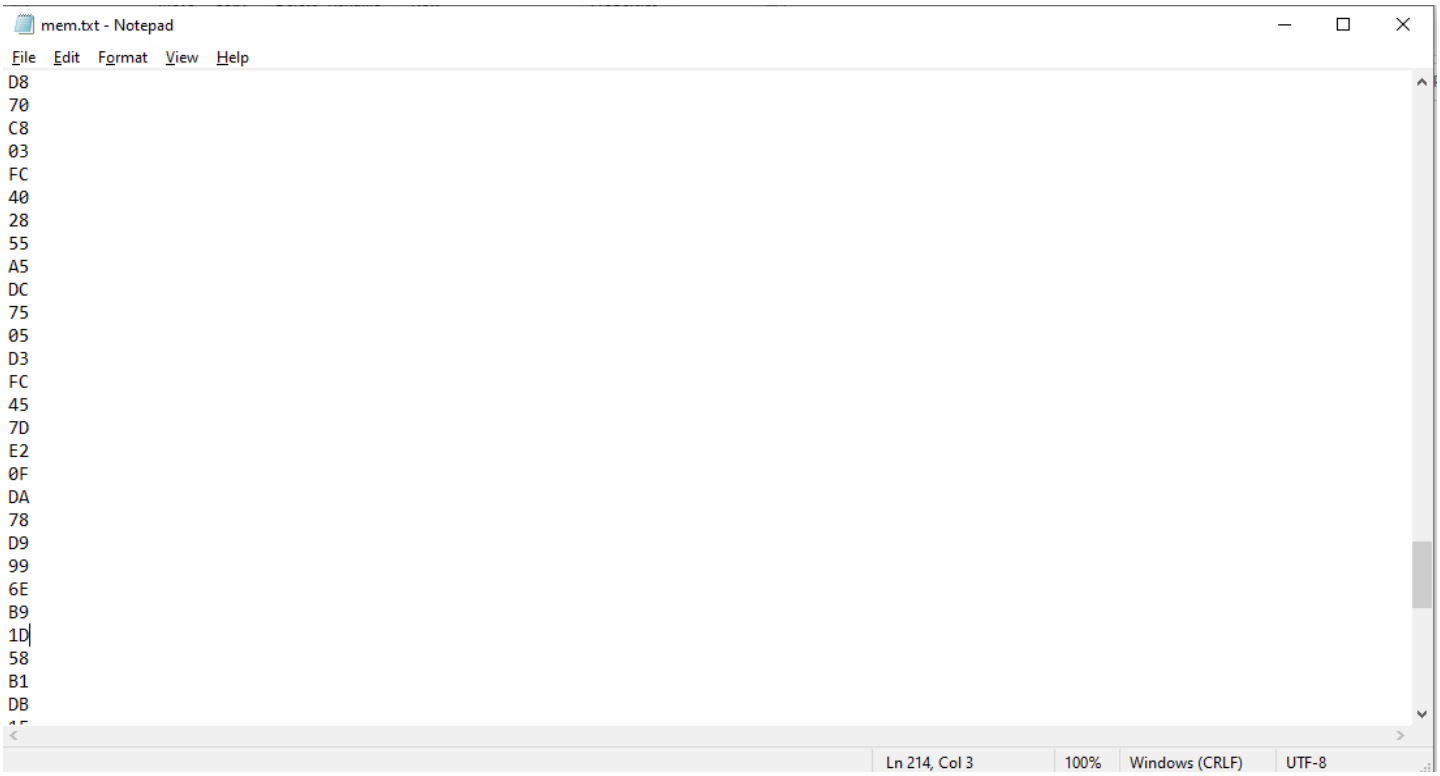
After that read data in held read address:



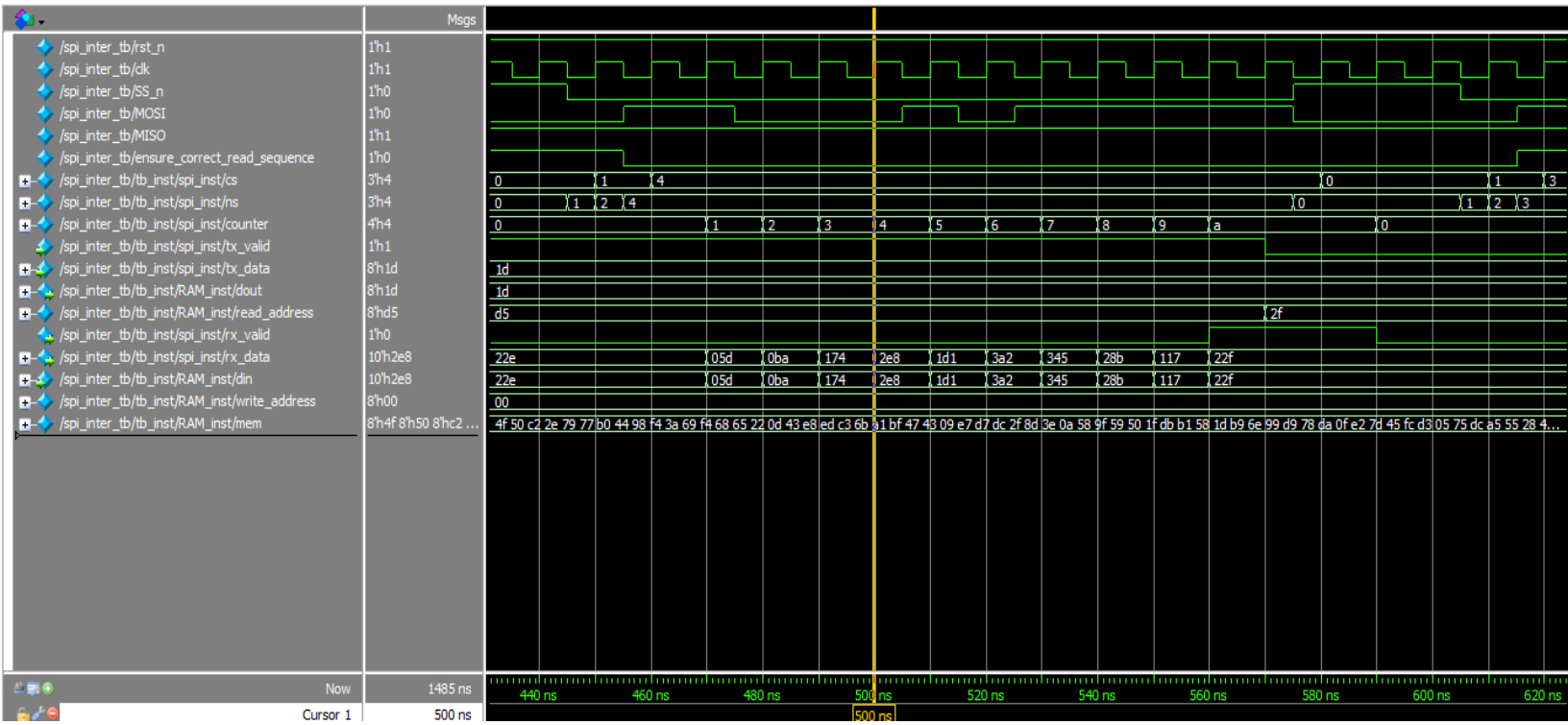
After that enable tx_valid and Convert Parallel data in tx_data to serial bits in MISO through 8 cycles:



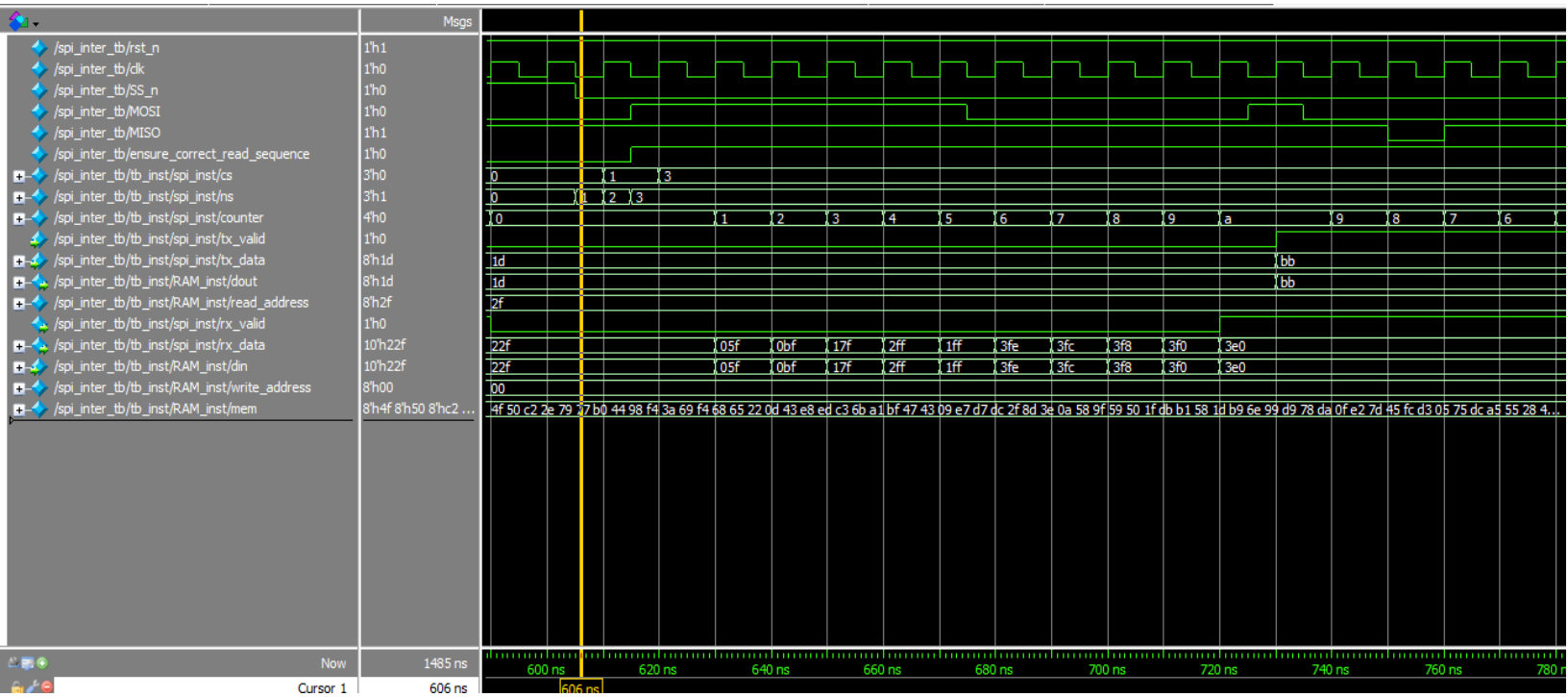
Held address data in mem.txt file: [1D]



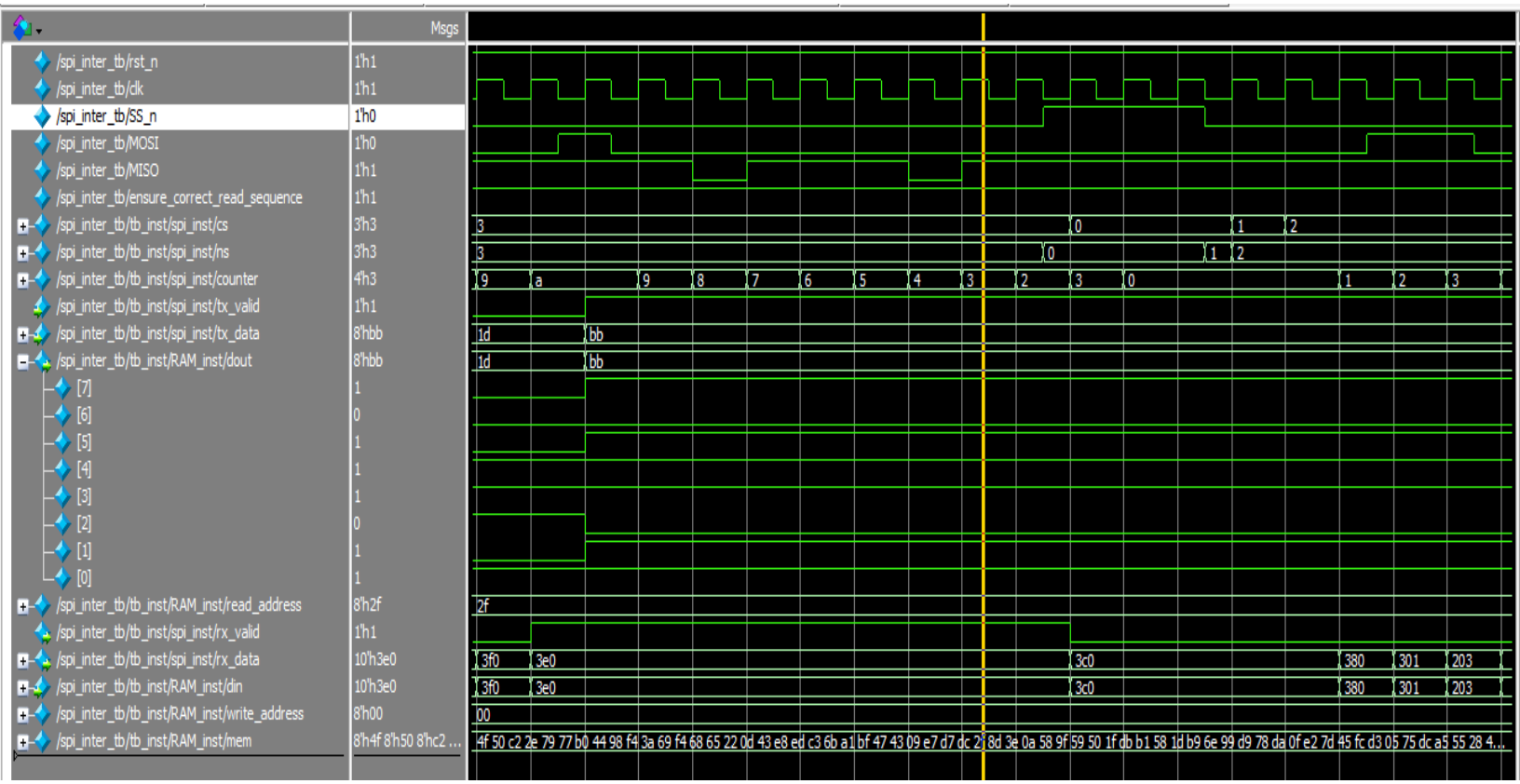
Another Hold Read Address case:



Another Read Data case:

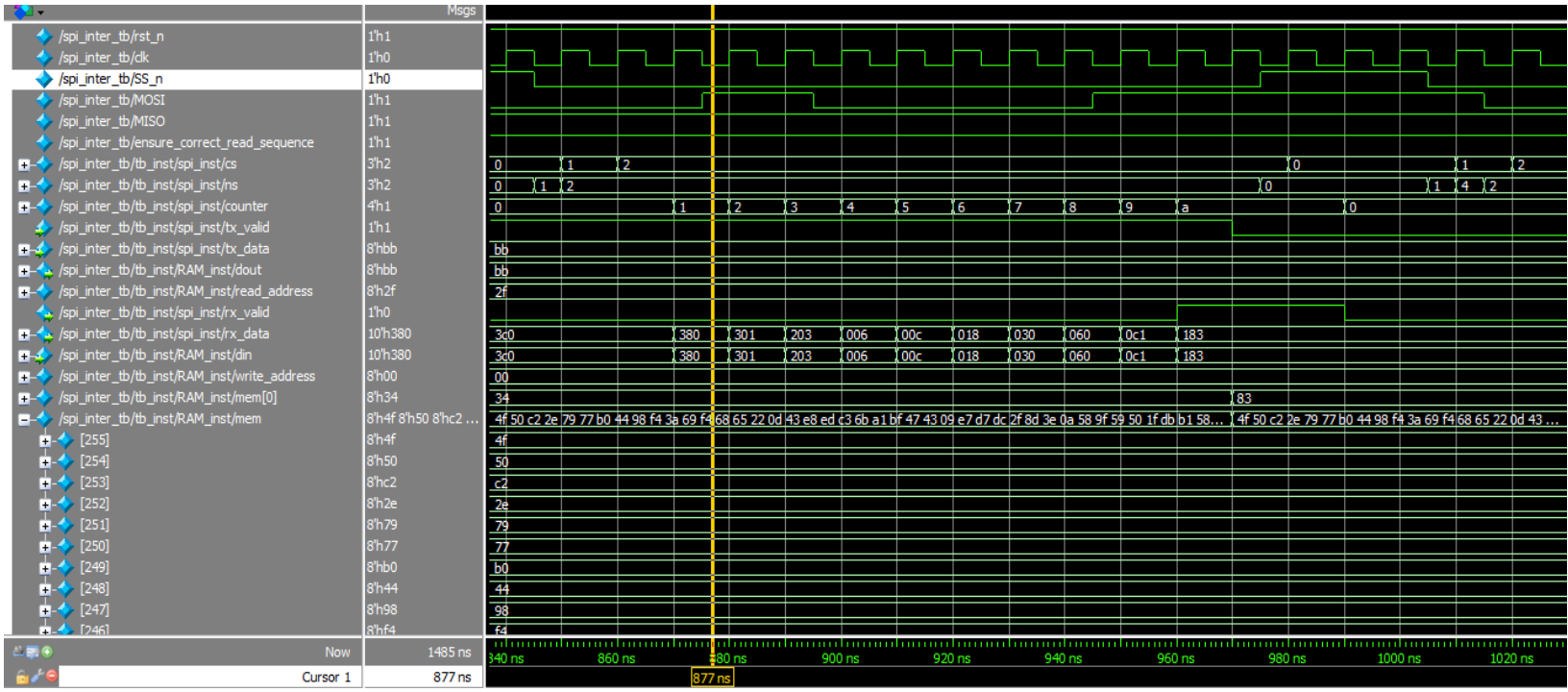


The address 47 in mem.txt file does indeed hold the value “BB”.

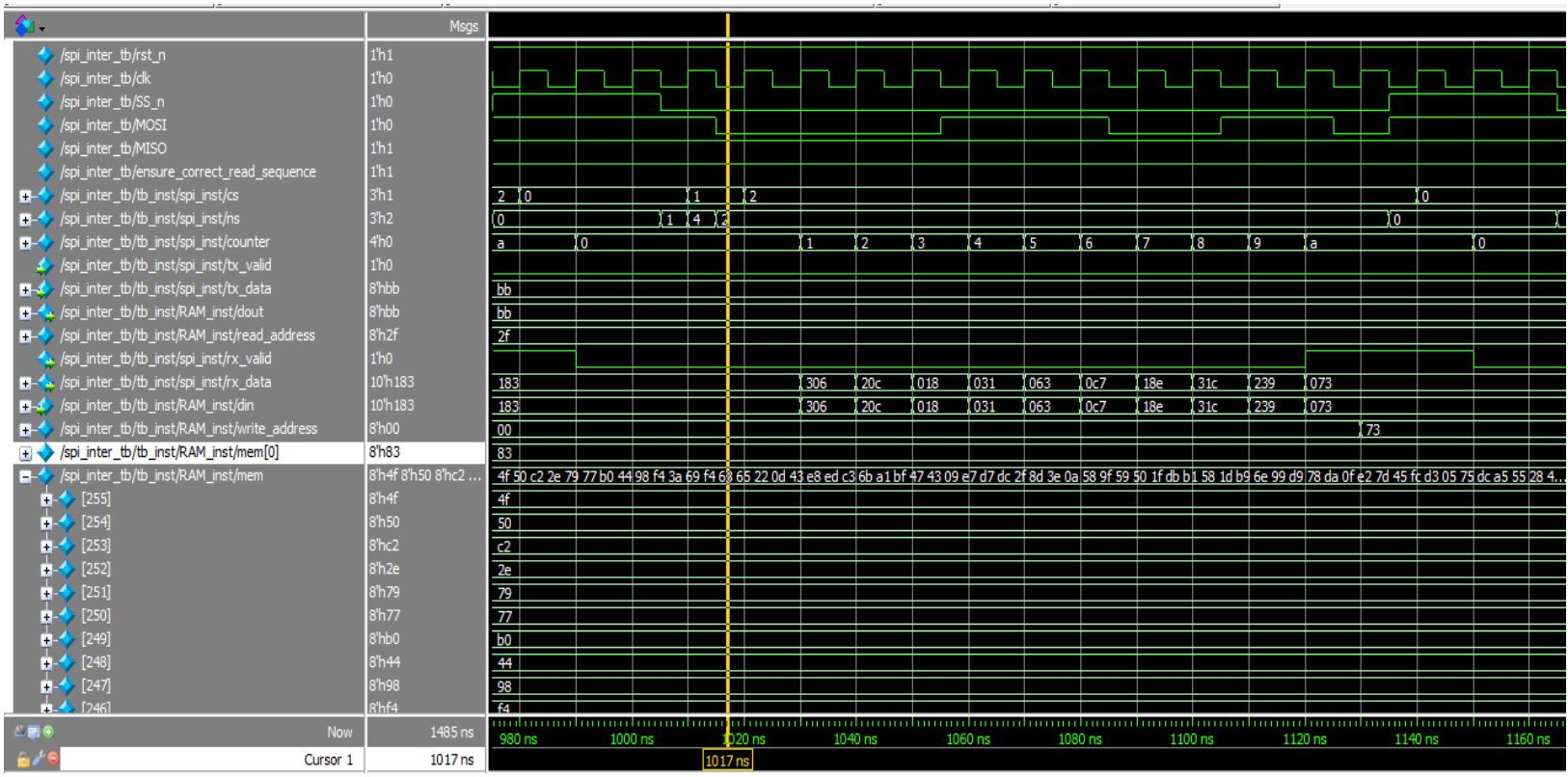


Write Operation testing:

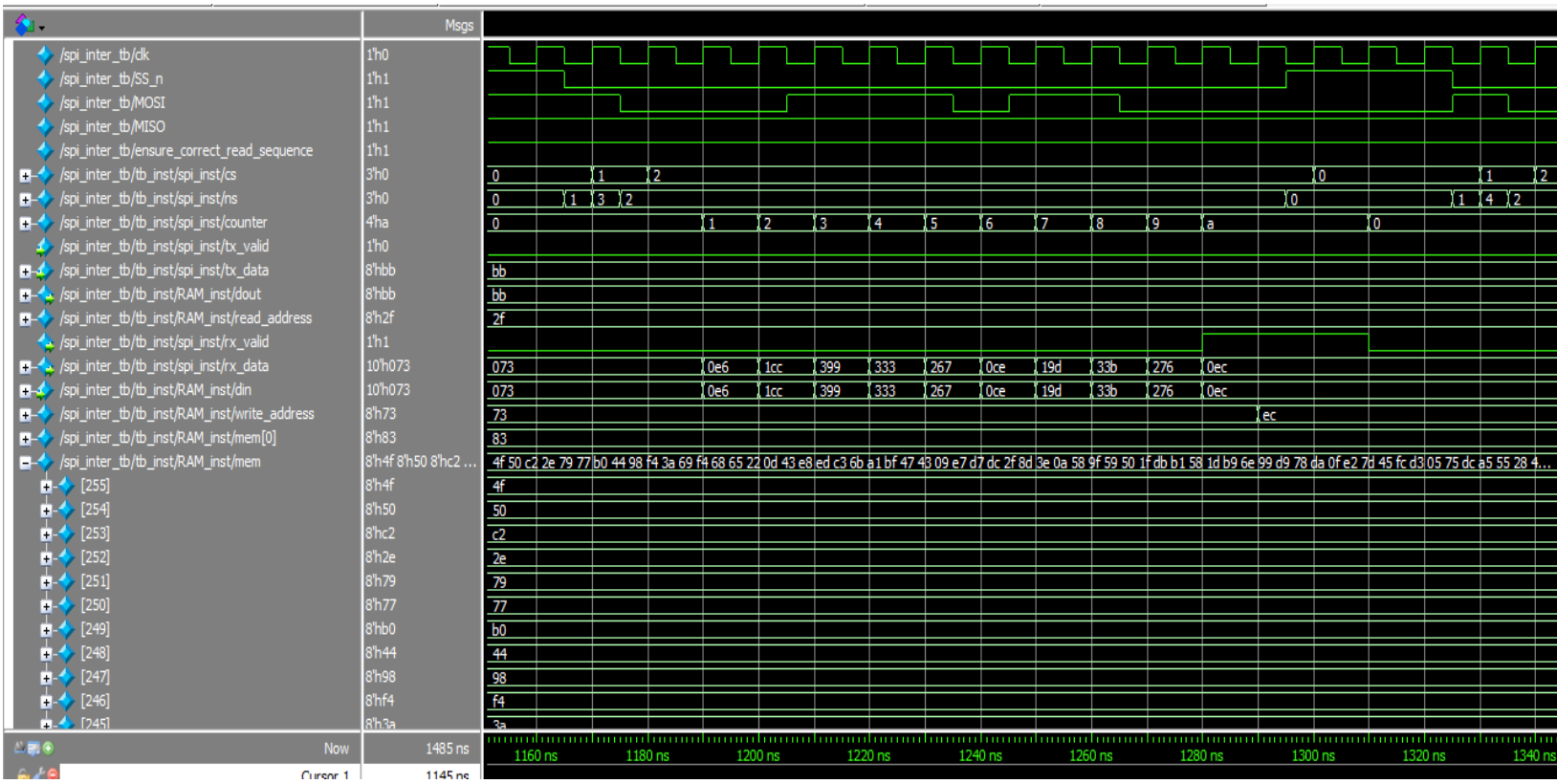
Write Data in the Held Write Address:



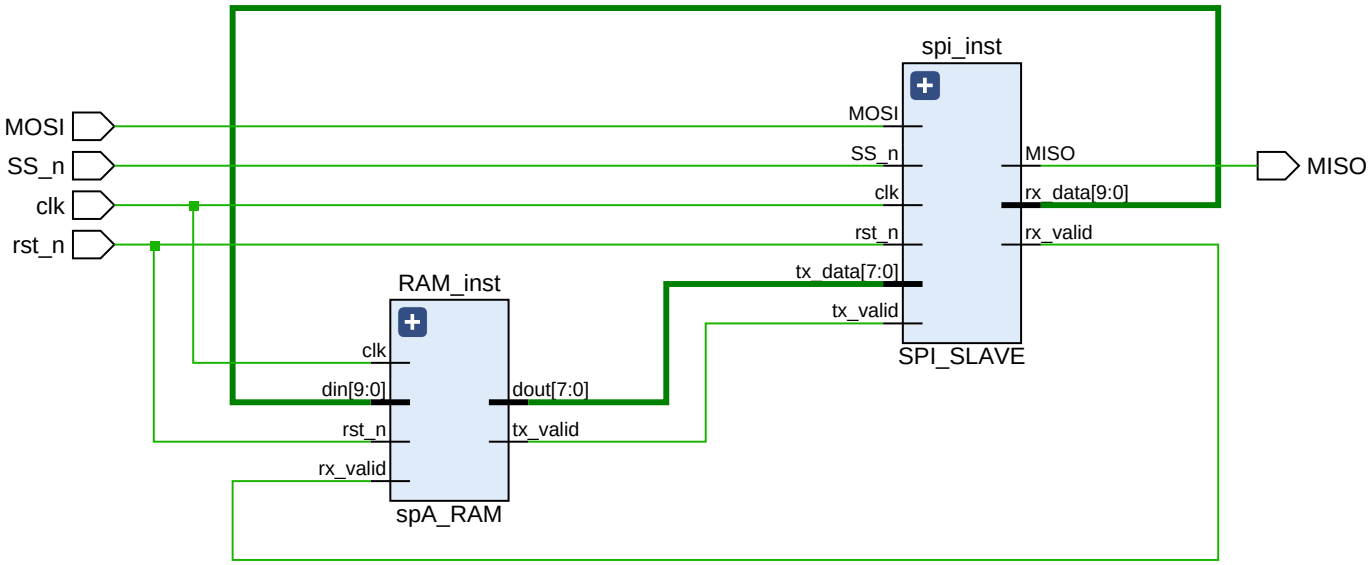
Hold Write Address Operation:



Another Write Data in Held Write Address Test:



Xilinx Vivado Elaborated and Synthesized Designs schematics:


MOSI
SS_n
clk
rst_n
spi_inst
MOSI
SS_n
clk
rst_n
tx_data[7:0]
tx_valid
MISO
rx_data[9:0]
rx_valid
SPI_SLAVE
MISO
RAM_inst
clk
din[9:0]
rst_n
rx_valid
dout[7:0]
tx_valid
spA_RAM