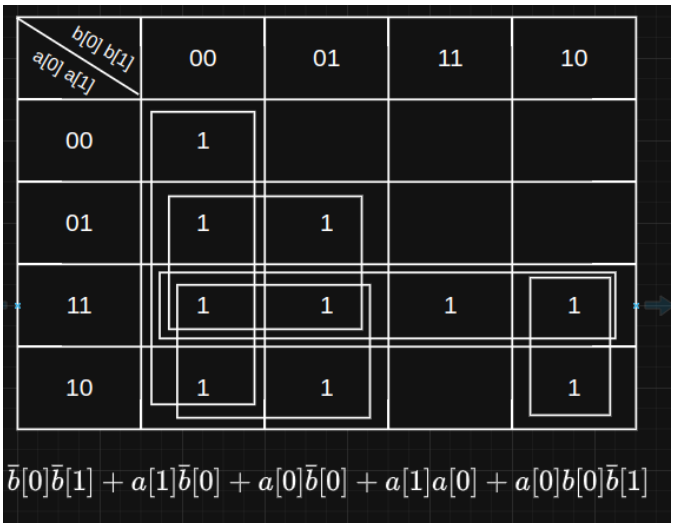
Truth Table

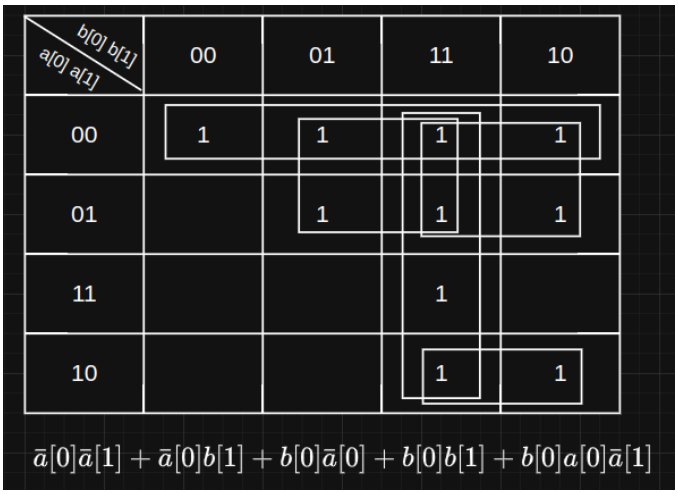
INPUT					OUTPUT			
A[0] (MSB)	A[1] (LSB)	B[0] (MSB)	B[1] (LSB)	Comparison	Color	Red	Green	Blue
0	0	0	0	A=B	Yellow	1	1	0
0	0	0	1	A<B	Cyan	0	1	1
0	0	1	0	A<B	Cyan	0	1	1
0	0	1	1	A<B	Cyan	0	1	1
0	1	0	0	A>B	Purple	1	0	1
0	1	0	1	A=B	Yellow	1	1	0
0	1	1	0	A<B	Cyan	0	1	1
0	1	1	1	A<B	Cyan	0	1	1
1	0	0	0	A>B	Purple	1	0	1
1	0	0	1	A>B	Purple	1	0	1
1	0	1	0	A=B	Yellow	1	1	0
1	0	1	1	A<B	Cyan	0	1	1
1	1	0	0	A>B	Purple	1	0	1
1	1	0	1	A>B	Purple	1	0	1
1	1	1	0	A>B	Purple	1	0	1
1	1	1	1	A=B	Yellow	1	1	0

K-MAPS and Inferred Circuit:

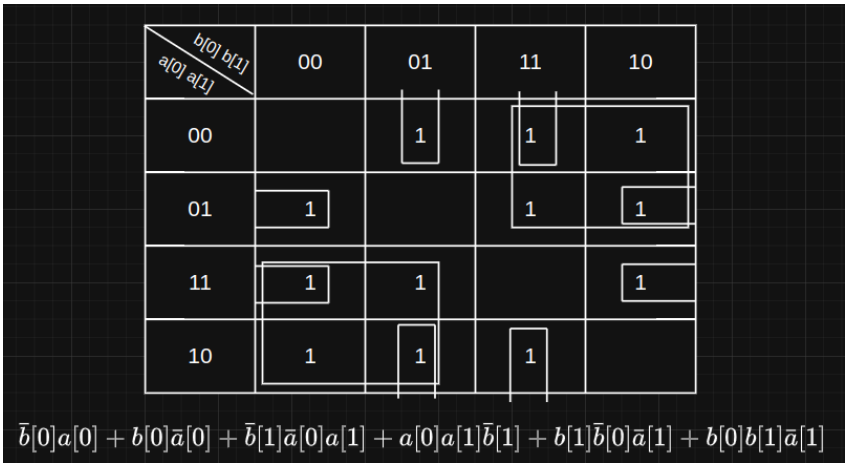
For RED color:



For GREEN color:



For BLUE color:



Circuit diagram from K-Maps:

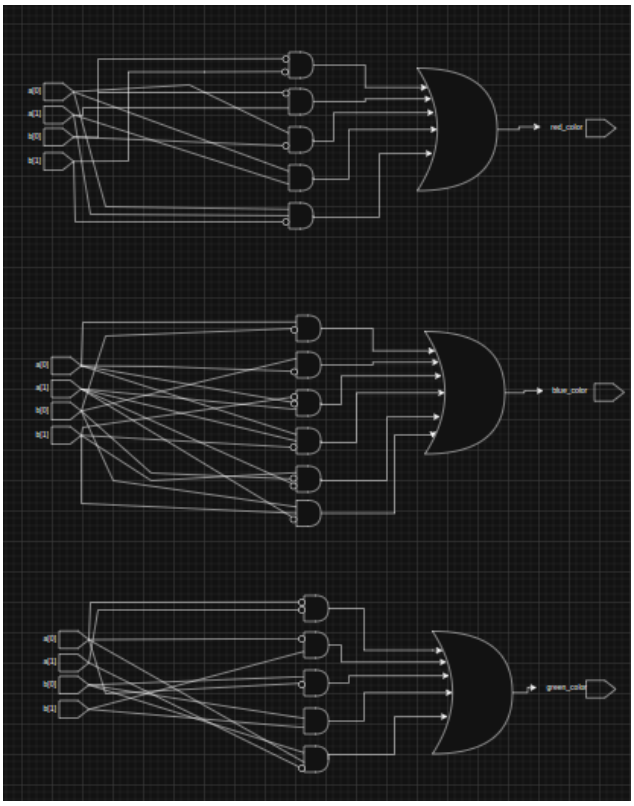
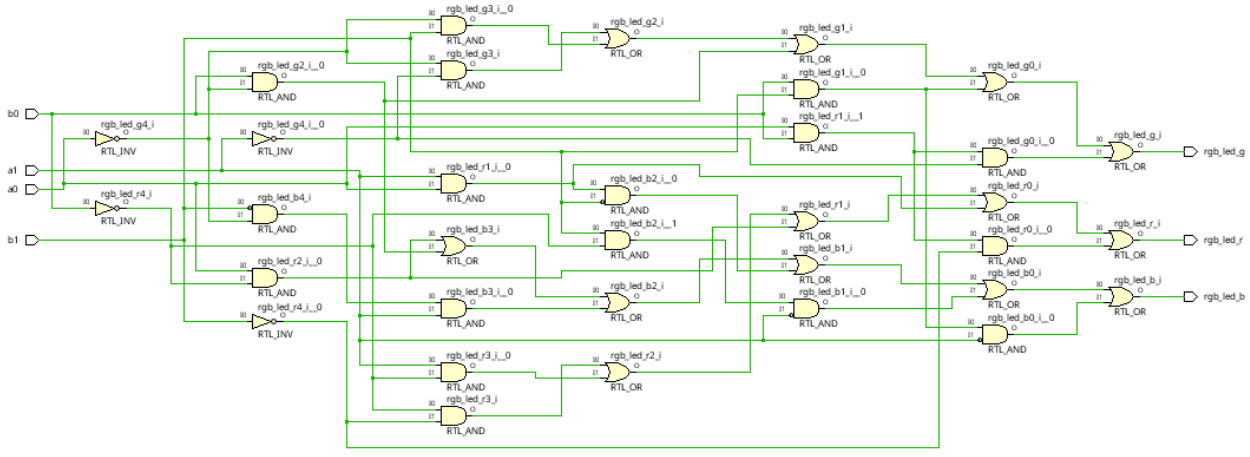


Diagram inferred by Xilinx Vivado:



After testing of the SystemVerilog code in QuestaSim, and comparing it with the truth table above, the inferred circuit diagram is similar to the circuit diagrams from K-Maps.

Combinational Delay:

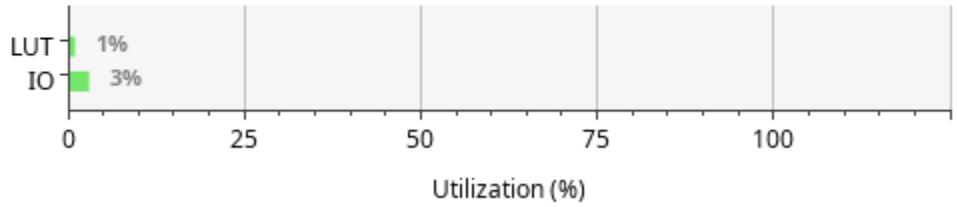
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	3	a1	rgb_led_b	9.842	5.140	4.701	∞	input port clo
Path 2	∞	3	2	3	a1	rgb_led_g	9.464	5.377	4.087	∞	input port clo
Path 3	∞	3	2	3	a1	rgb_led_r	8.665	5.130	3.535	∞	input port clo

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 4	∞	3	2	3	b1	rgb_led_r	2.203	1.504	0.699	-∞	input port clo
Path 5	∞	3	2	3	b1	rgb_led_g	2.529	1.586	0.943	-∞	input port clo
Path 6	∞	3	2	3	b1	rgb_led_b	2.770	1.514	1.256	-∞	input port clo

Maximum Combinational Delay is from a1 to rgb_led_b with 9.842s.

Resource Utilization:

Resource	Utilization	Available	Utilization %
LUT	2	63400	0.00
IO	7	210	3.33



2 out of 63400 LUTs and 7 out of 210 I/O were utilized.

SystemVerilog code of the circuit:

```
`timescale 1ns / 1ps

module rgb_module_code( input a0, input a1, input b0, input b1, output rgb_led_r, output rgb_led_g, output rgb_led_b );

assign rgb_led_r = (b0 & ~b1) | (a1 & ~b0) | (a0 & ~b0) | (a1 & a0) | (a0 & b0 & ~b1);

assign rgb_led_g = (a0 & a1) | (a0 & b1) | (b0 & a0) | (b0 & b1) | (b0 & a0 & ~a1);

assign rgb_led_b = (b0 & a0) | (b0 & a0) | (b1 & ~a0 & a1) | (a0 & a1 & ~b1) | (b1 & ~b0 & ~a1) | (b0 & b1 & ~a1);

endmodule
```