| Ali Tahir | 2023-EE-062 | Section B |

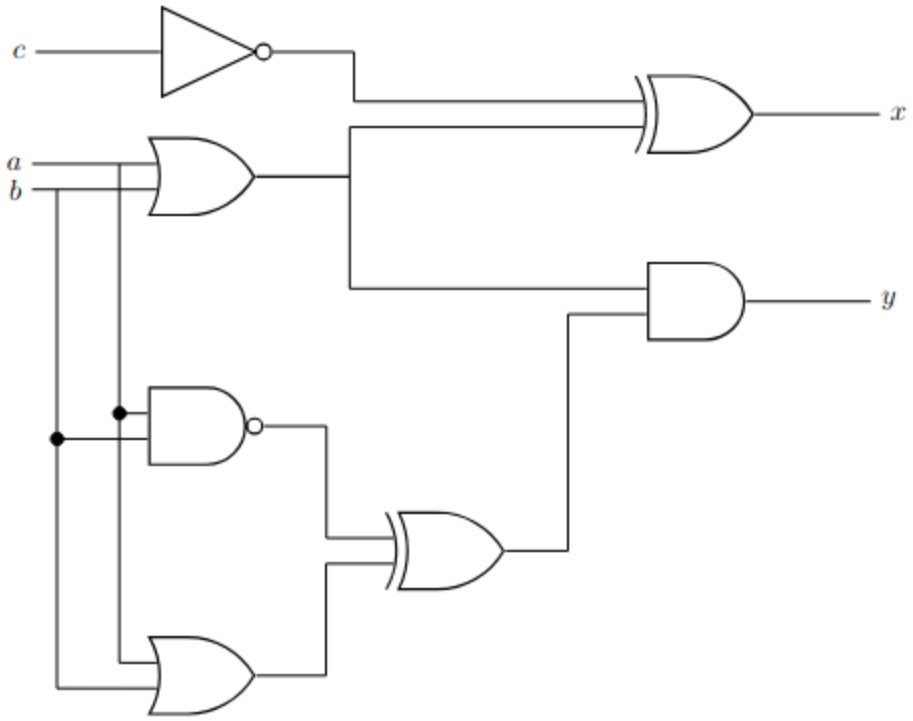

Fig. 2.14: Circuit to be implemented.

Truth Table:

Input			Output	
A	b	c	X	Y
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

Maximum Combinational Delay

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	D
Path 1	∞	3	2	1	c	x	9.268	5.363	3.905	∞	input port clock	
Path 2	∞	3	2	2	b	y	8.370	5.124	3.247	∞	input port clock	

Path 1 has the most delay from c to x having 9.268s delay

Resource Utilization:

```
7. Primitives
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+----------+------+----------------------+
| Ref Name | Used | Functional Category |
+----------+------+----------------------+
| IBUF     |    3 |                   IO |
| OBUF     |    1 |                   IO |
| LUT3     |    1 |                  LUT |
+----------+------+----------------------+
```

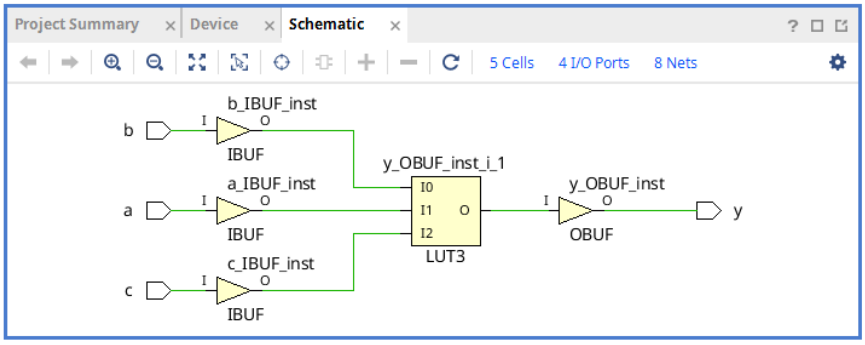
4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	4	0	210	1.90
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

- **Logic Usage**: Only 1 LUT is used, with no registers, muxes, or memory elements.
- **IO Usage**: 4 I/O blocks are used out of 210 (1.9% utilization).

Schematic Comparison:

Implemented Design:



Synthesized Design: