In Test Bench

1. Incorrect syntax, missing semicolon in tb
2. Incorrect instantiation, missing name and missing required parameter
3. Missing code for printing wave to wave generator

In Instantiated module,

1. Incorrect operator for and, added &
2. Incorrect type of variable ‘sum’

Corrected code

For test bench:

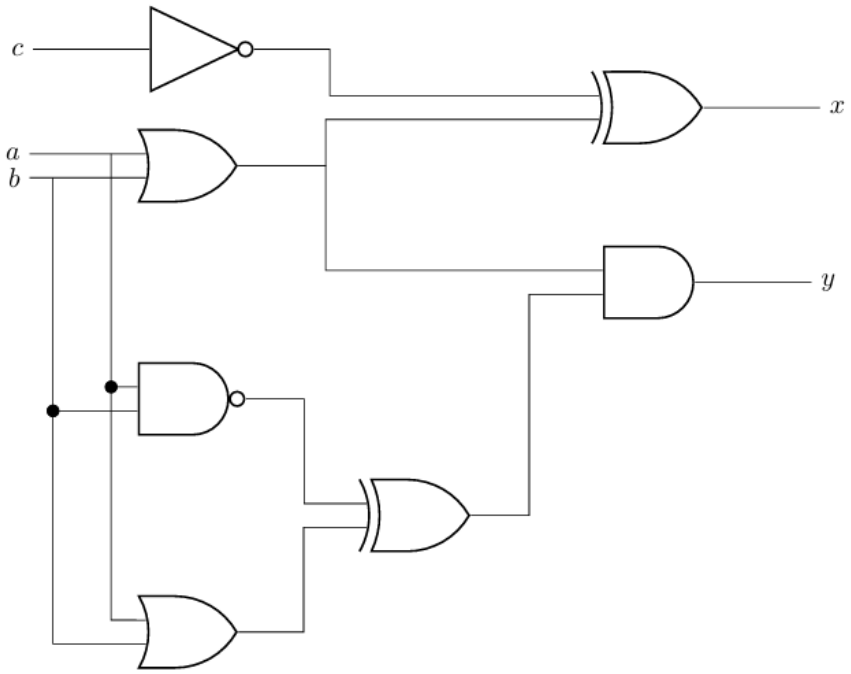
```
module full_adder_tb();
 logic a1;
 logic b1;
 logic c1;
 logic sum1;
 logic carry1

 full_adder UUT (
 .a(a1),
 .b(b1),
 .c(c1),
 .sum(sum1),
 .carry(carry1)
 );
 initial
 begin
 a = 0; b = 0; c = 0;
 #10;
 a1 = 0; b1 = 0; c = 1;
 #10;
 a1 = 0; b1 = 1; c1 = 0;
 #10;
 a1 = 0; b = 1; c1 = 1;
 #10;
 a1 = 1; b1 = 0; c1 = 0;
 #10;
 a1 = 1; b1 = 0; c1 = 1;
 #10;
 a = 1; b1 = 1; c1 = 0;
 #10;
 a1 = 1; b1 = 1; c1 = 1;
 #10;
 $stop;
 end


 initial
 begin
 $monitor("y=%b, a=%b, b=%b, c=%b", y1,a1,b1,c1);
 end
```

```
endmodule
```

For full adder module:

```
module full_adder(
 input logic a,
 input logic b,
 input logic c,
 output logic sum,
 output logic carry,
 );
 assign sum = (a ^ b) ^ c;
 assign carry = (a & b) | (c ^ (a ^ b));
 endmodule
```

Truth table of the circuit



Input			Output	
a	b	c	x	y
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

SystemVerilog of the given circuit:

```
module Lab03 (input logic a, b, c, output logic x, y);
  logic not_c, or_ab, and_ab, not_and_ab, or_ab_2, xor_out;

  not u1(not_c, c);
  or u2(or_ab, a, b);
  nand u3(not_and_ab, a, b);
  xor u4(xor_out, not_and_ab, or_ab);
  and u5(y, or_ab, xor_out);
  xor u6(x, not_c, or_ab);
endmodule
```

Testbench code of the above code:

```
module Lab03_tb();
  logic a, b, c;
  logic x, y;
  Lab03 UUT (
    .a(a),
    .b(b),
    .c(c),
    .x(x),
    .y(y)
  );
  initial begin
    a = 0; b = 0; c = 0;
    #10;
    a = 1; b = 0; c = 0;
    #10;
    a = 0; b = 1; c = 0;
    #10;
    a = 1; b = 1; c = 0;
    #10;
    a = 0; b = 0; c = 1;
    #10;
    a = 1; b = 0; c = 1;
    #10;
    a = 0; b = 1; c = 1;
    #10;
    a = 1; b = 1; c = 1;
    #10;
    $finish;
  end
  initial begin
    $monitor("Time=%0t, a=%0b, b=%0b, c=%0b, x=%0b, y=%0b", $time, a, b, c, x, y);
  end
endmodule
```