Determining the saturated current of 32nm MOSFETs

Ali Abyaneh – abyaneh.ali@gmail.com, abyaneh@outlook.com

Abstract—This article describes a simulation project in which the saturation current of a short-channel NMOS and PMOS MOSFET is calculated with the help of extrapolation. Afterward, the I-V characteristic of transistors is compared with the estimation of such short-channel transistor models as Ning and Taur model.

 NMOS, PMOS, MOSFET, I-V characteristic. Keywords-

I. INTRODUCTION

In the past decades, the galloping rate at which technology is progressing has changed everything, one of which is the size of transistors. In other words, the world's smallest transistor is 1nm long, whereas, in the 1990s, the smallest transistor was about 0.25µm long. Therefore, it stands to reason that longchannel models are not useful anymore in that in 1nm quite a few factors affect the behavior of transistors.

II. CALCULATING THE THRESHOLD VOLTAGE

In general, for long channel transistors, the drain current is:

$$\begin{cases} I_{ds} = \frac{K'_n w}{l} \left[V_{GS} - V_{th} - \frac{V_{DS}}{2} \right] V_{DS} & Linear \\ I_{ds} = \frac{K'_n w}{2l} \left[V_{GS} - V_{th} \right]^2 [1 + V_{DS}. \lambda] & Saturation \end{cases}$$

In the Linear region, if V_{DS} is small, we can assume that:

$$I_{ds} = \frac{K'_{n}w}{l}[V_{GS} - V_{th}]V_{DS}$$

Therefore, we can assume that in the point where the current is zero, $V_{th} = V_{GS}$. In other words, with extrapolation, we can estimate V_{th} in the linear region of long channel transistors. Nonetheless, in the saturated region, this method is not practical because there is no linear relation between Ids and Vth. However, in short channel transistors, due to mobility degradation and velocity saturation, to name but two, Ids has linear relation with voltage,

$$I_{ds} = k[V_{GS} - V_{th}^*]$$

 $I_{ds} = k[V_{GS} - V_{th}^*]$ where V_{th} is calculated from V_{gs} - I_{ds} characteristic of the transistor. Figure 1 shows this method precisely.

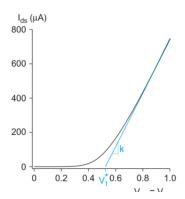


Figure 3 - I-V characteristc of NMOS MOSFET, V_{Gs}=V_{Ds}

Hence, in the first place, we have to determine the I_{ds} by sweeping the drain-source voltage in a hspice code. Afterward, we can draw the characteristic and estimate V_{th} .

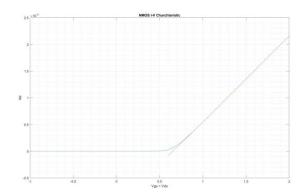
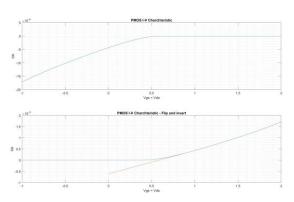


Figure 1, I-V characteristc of a 32nm NMOS MOSFET in 32nm_LP library, V_{Gs}=V_{Ds}.



Figu2, I-V characteristc of a 32nm PMOS MOSFET in 32nm_LP library,

Also,

Transistor	Threshold Voltage
NMOS	0.65113 v
PMOS	-0.5847 v

III. USING A MODEL FROM NING AND TAUR BOOK

Moreover, we can use the Ning and Taur simplified model,

$$I_{Dsat} = \frac{W}{L} \mu_{eff} C_{ox} V_{Dsat} (V_{GS} - V_{TH})$$

$$V_{DS} = \frac{(V_{GS} - V_{Th}) E_c L}{(V_{GS} - V_{TH}) + E_c L}$$
According to the BSIM480_Manual and the 32nm_LP

library,

$$t_{ox} = t_{oxe} = 1.65e - 9 = 1.65 nm$$

$$C_{ox} = EPSROX. \frac{\varepsilon_0}{t_{ox}} = 3.9 * \frac{8.854187817 \times 10^{-12}}{1.65 \times 10^{-9}} = 0.0209$$

Therefore,

$$I_{dsat} = \frac{W}{L} C_{ox} \frac{540}{1 + \left(\frac{V_{gs} + V_t}{0.54 * t_{ox}}\right)^{1.85} \frac{\left(V_{gs} - V_{th}\right)^2 E_c L}{\left(V_{gs} - V_{th}\right) + E_c L}$$

Hence, if we sweep V_{gs} in the spice model and calculate I_{dsat} , we can readily use a non-linear curve fit and estimate the best value for E_CL . Note that Ning and Taur model can be used only in the saturation region. Accordingly, I biased the simulated transistor in the saturation region, that is, $V_{ds} = V_{DD}$ and V_{gs} are swept from 0.8v to $V_{DD} = 1.1v$. The result of this part is depicted in figure 4.

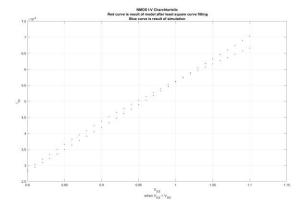


Figure 4 - I-V characteristic of model

Also, I used this model to calculate V_{dsat} :

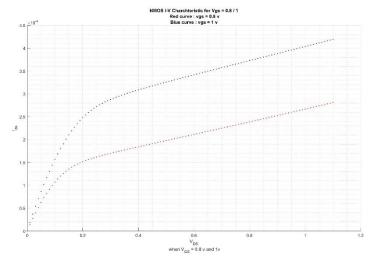


Figure 5- I-V characteristic

	${f V_{gs}}$	V_{ds} (V)
	simulation	model
0.8	0.18	0.14654
1	0.29	0.29448

IV. CONCLUSION

According to the result, the simplified Ning and Taur model is a good model for estimating V_{dsat} in short-channel transistors.

V. REFERENCES

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