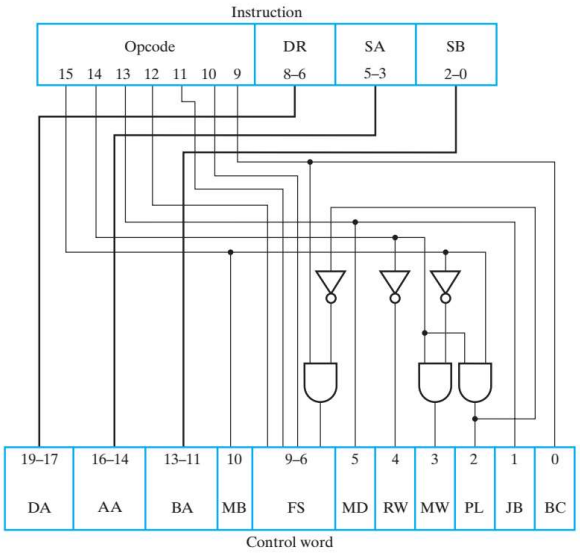
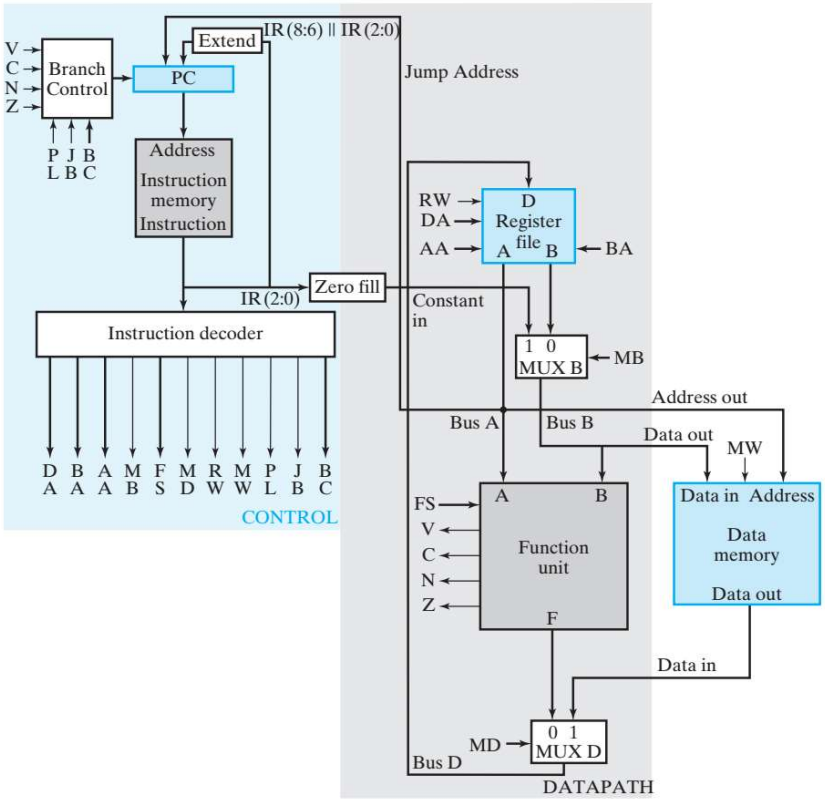
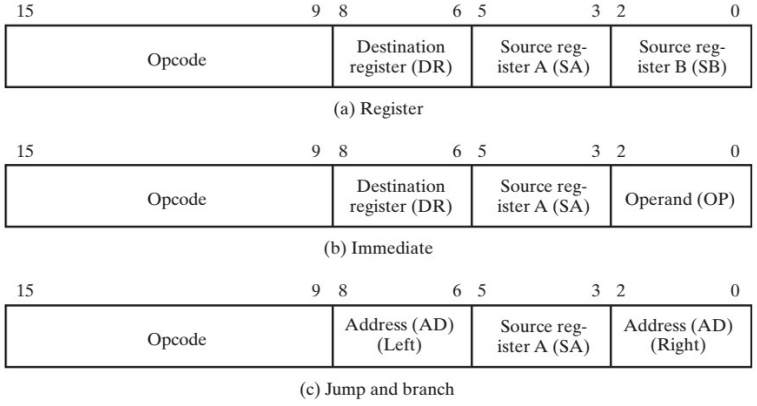
Instruction Specifications for the Simple Computer

Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move A	0000000	MOVA	RD, RA	R[DR] ← R[SA]*	N, Z
Increment	0000001	INC	RD, RA	R[DR] ← R[SA] + 1*	N, Z
Add	0000010	ADD	RD, RA, RB	R[DR] ← R[SA] + R[SB]*	N, Z
Subtract	0000101	SUB	RD, RA, RB	R[DR] ← R[SA] − R[SB]*	N, Z
Decrement	0000110	DEC	RD, RA	R[DR] ← R[SA] − 1*	N, Z
AND	0001000	AND	RD, RA, RB	R[DR] ← R[SA] ∧ R[SB]*	N, Z
OR	0001001	OR	RD, RA, RB	R[DR] ← R[SA] ∨ R[SB]*	N, Z
Exclusive OR	0001010	XOR	RD, RA, RB	R[DR] ← R[SA] ⊕ R[SB]*	N, Z
NOT	0001011	NOT	RD, RA	R[DR] ← $\overline{R[SA]}$*	N, Z
Move B	0001100	MOVB	RD, RB	R[DR] ← R[SB]*	
Shift Right	0001101	SHR	RD, RB	R[DR] ← sr R[SB]*	
Shift Left	0001110	SHL	RD, RB	R[DR] ← sl R[SB]*	
Load Immediate	1001100	LDI	RD, OP	R[DR] ← zf OP*	
Add Immediate	1000010	ADI	RD, RA, OP	R[DR] ← R[SA] + zf OP*	N, Z
Load	0010000	LD	RD, RA	R[DR] ← M[SA]*	
Store	0100000	ST	RA, RB	M[SA] ← R[SB]*	
Branch on Zero	1100000	BRZ	RA, AD	if (R[SA] = 0) PC ← PC + se AD, if (R[SA] ≠ 0) PC ← PC + 1	N, Z
Branch on Negative	1100001	BRN	RA, AD	if (R[SA] < 0) PC ← PC + se AD, if (R[SA] ≥ 0) PC ← PC + 1	N, Z
Jump	1110000	JMP	RA	PC ← R[SA]*	

* For all of these instructions, PC ← PC + 1 is also executed to prepare for the next cycle.







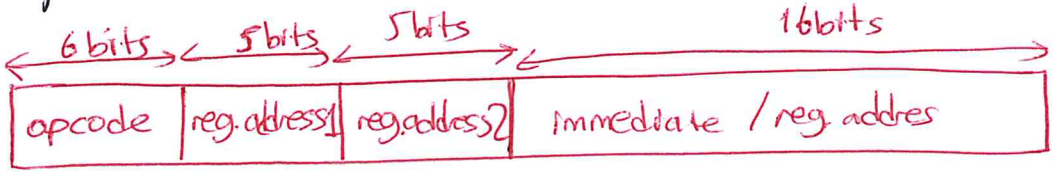
Ex: A computer has a 32-bit instruction word broken into fields as follows: opcode (6-bits), two register file address fields (5-bits each), and one immediate operand / register file address field (16-bits).

(a) What is the maximum number of operations that can be specified?

(b) How many registers can be addressed?

(c) What is the range of unsigned immediate operands that can be provided?

(d) What is the range of signed immediate operands that can be provided, assuming that the operands are in 2's complement representation and that bit 15 is the sign bit?



a) Number of operations: $2^{\#\text{ of opcode bits}}$

$= 2^6 = 64$

b) Number of registers: $2^{\#\text{ of reg. address bits}}$

$= 2^5 = 32$

c) unsigned immediate range $\Rightarrow$ $0 \leftrightarrow (2^{16}-1)$

$0 \leftrightarrow 65535$

d) signed immediate range $\Rightarrow$ $-(2^{15}+1) \leftrightarrow 2^{15}$

$-32768 \leftrightarrow 32767$

C#: The single-cycle computer in figure executes the following instructions described by the register transfers:

(a) Complete the following table, giving the binary instruction decoder outputs during execution of each of the instructions

Instruction	Instruction Register Transfer	DA	AA	BA	MB	FS	MD	RW	MW	PL	JB BC
exclusive or	R[0] ← R[7] ⊕ R[5]	000	111	011	0	1010	0	1	0	0	%
load	R[1] ← M[R[4]]	001	100	xxx	0	0000	1	1	0	0	%
add immediate	R[2] ← R[5] + 2	010	101	xxx	1	0010	0	1	0	0	%
shift left	R[3] ← sl R[6]	011	xxx	110	0	1110	0	1	0	0	%
branch on zero	if (R[4]=0) PC ← PC+seAD else PC ← PC+1	xxx	100	xxx	1	0000	0	0	0	1	%

(b) Complete the following table, giving the instruction in binary for the single-cycle computer that executes the register transfer (if any field is not used, give it the value 0)

Instruction	Instruction Register-Transfer	Opcode	DR	SA	SB or Operand
add	R[0] ← R[7] + R[6]	0000010	000	111	110
decrement	R[1] ← R[5] − 1	0000110	001	101	000
shift left	R[2] ← sl R[4]	0001110	010	000	100
not	R[3] ← $\overline{R[3]}$	0001011	011	011	000
or	R[4] ← R[2] ∨ R[1]	0001001	100	010	001