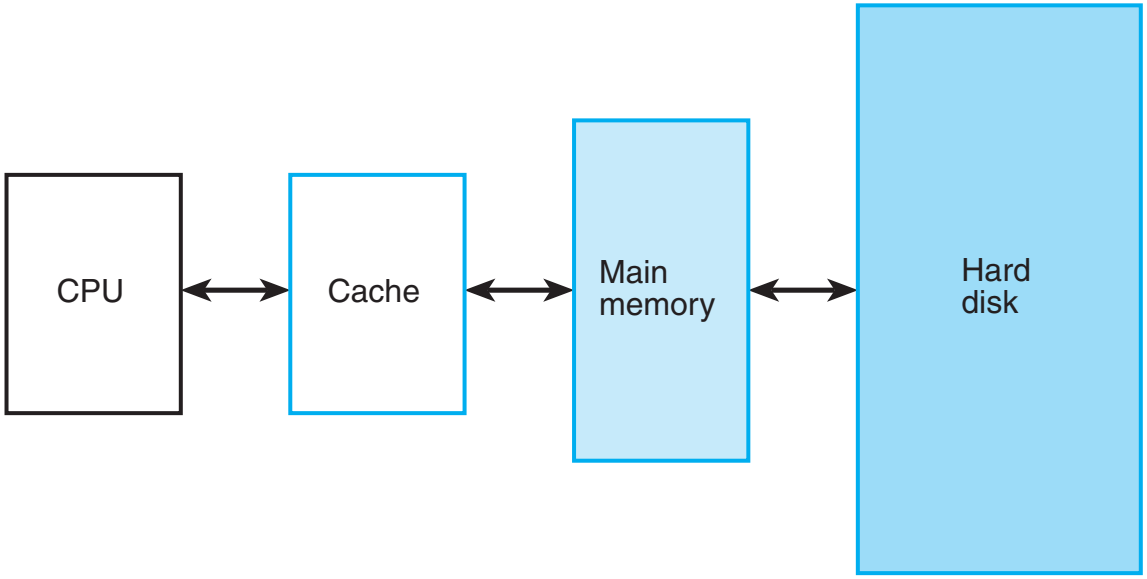

Fig. 12-1 Memory Hierarchy

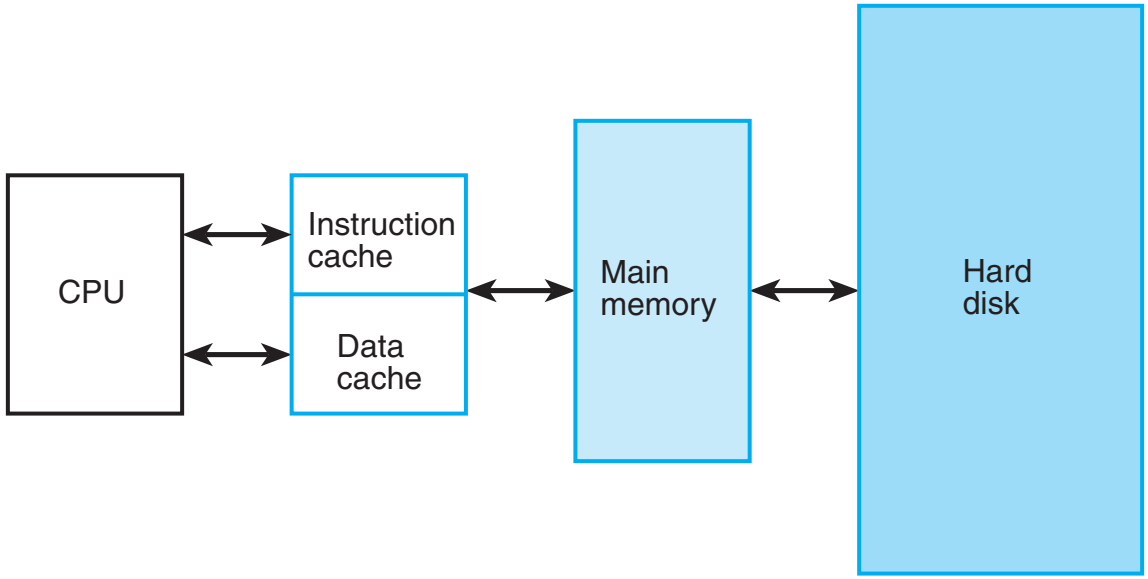

Fig. 12-2 Example of Memory Hierarchy

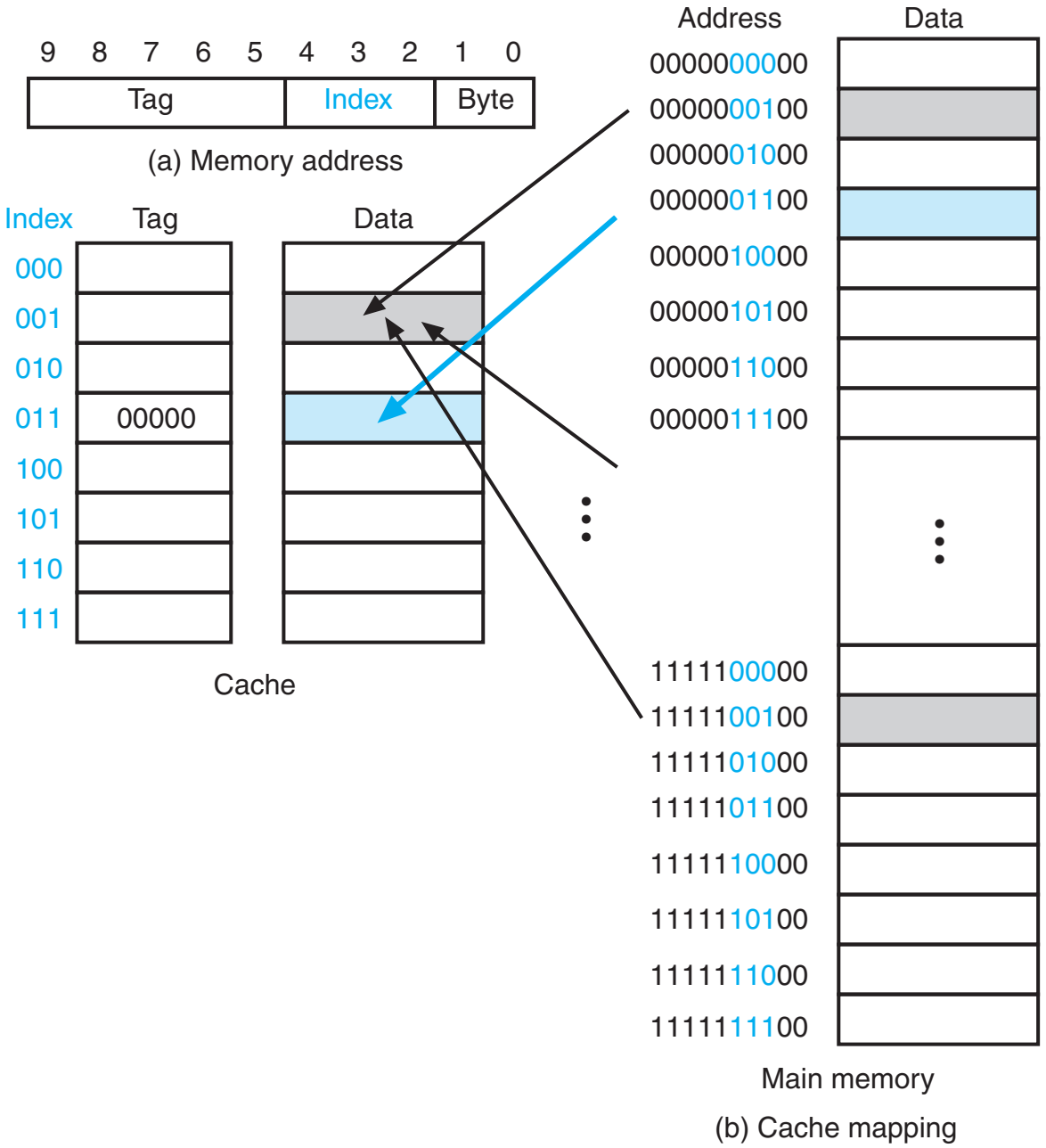

Fig. 12-3 Direct Mapped Cache

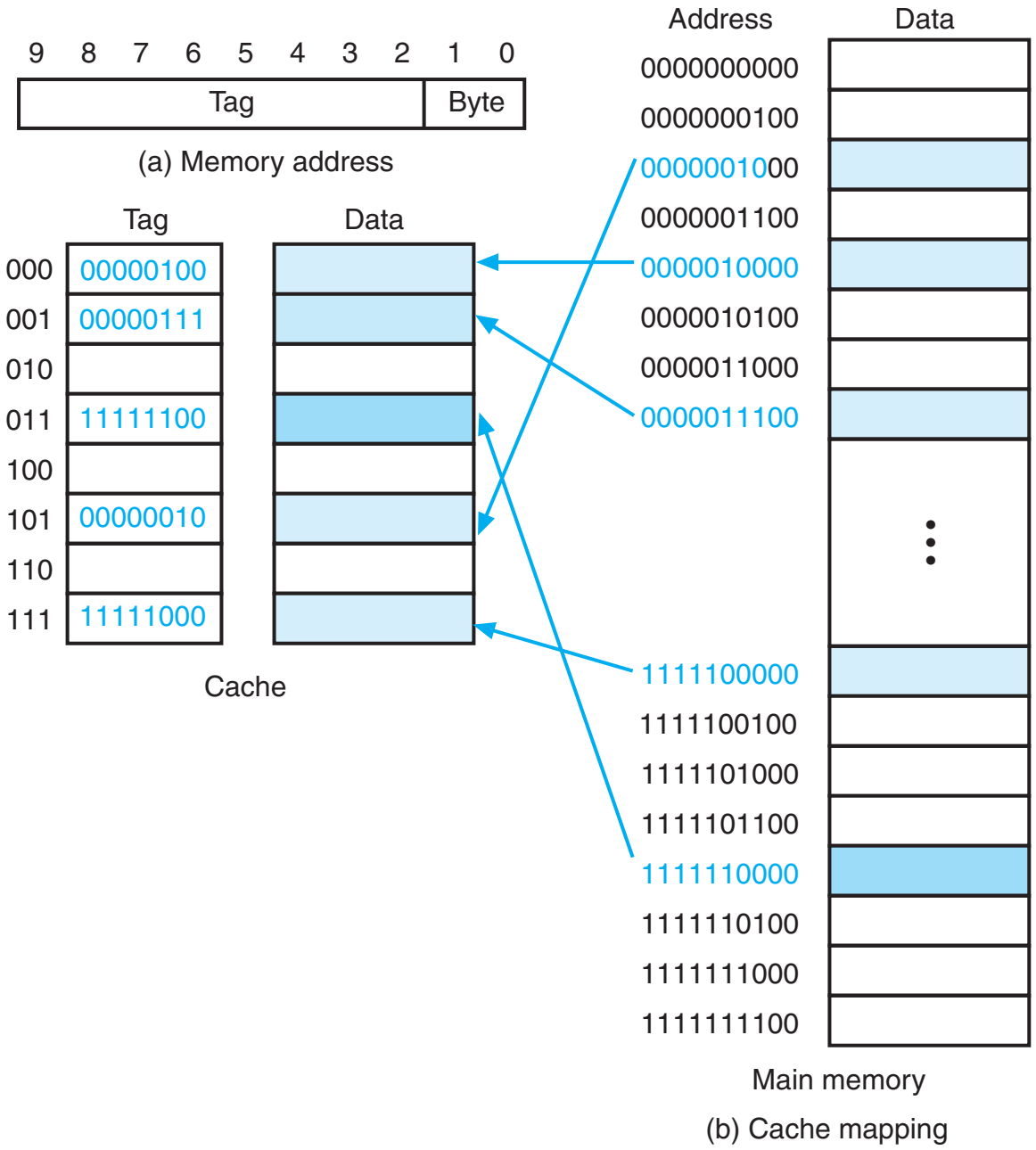

Fig. 12-4 Fully Associative Cache

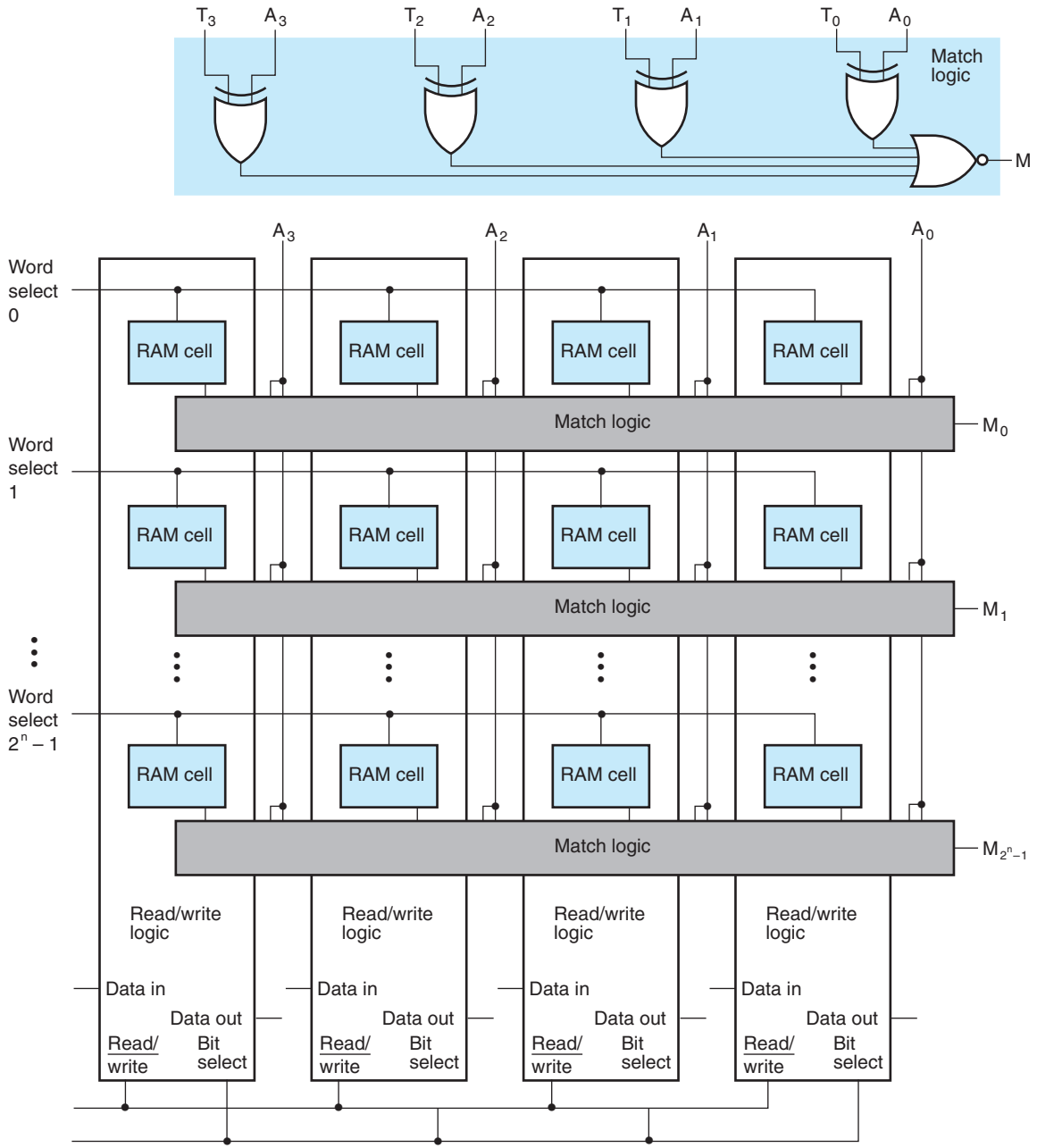

Fig. 12-5 Associative Memory for 4-bit Tags

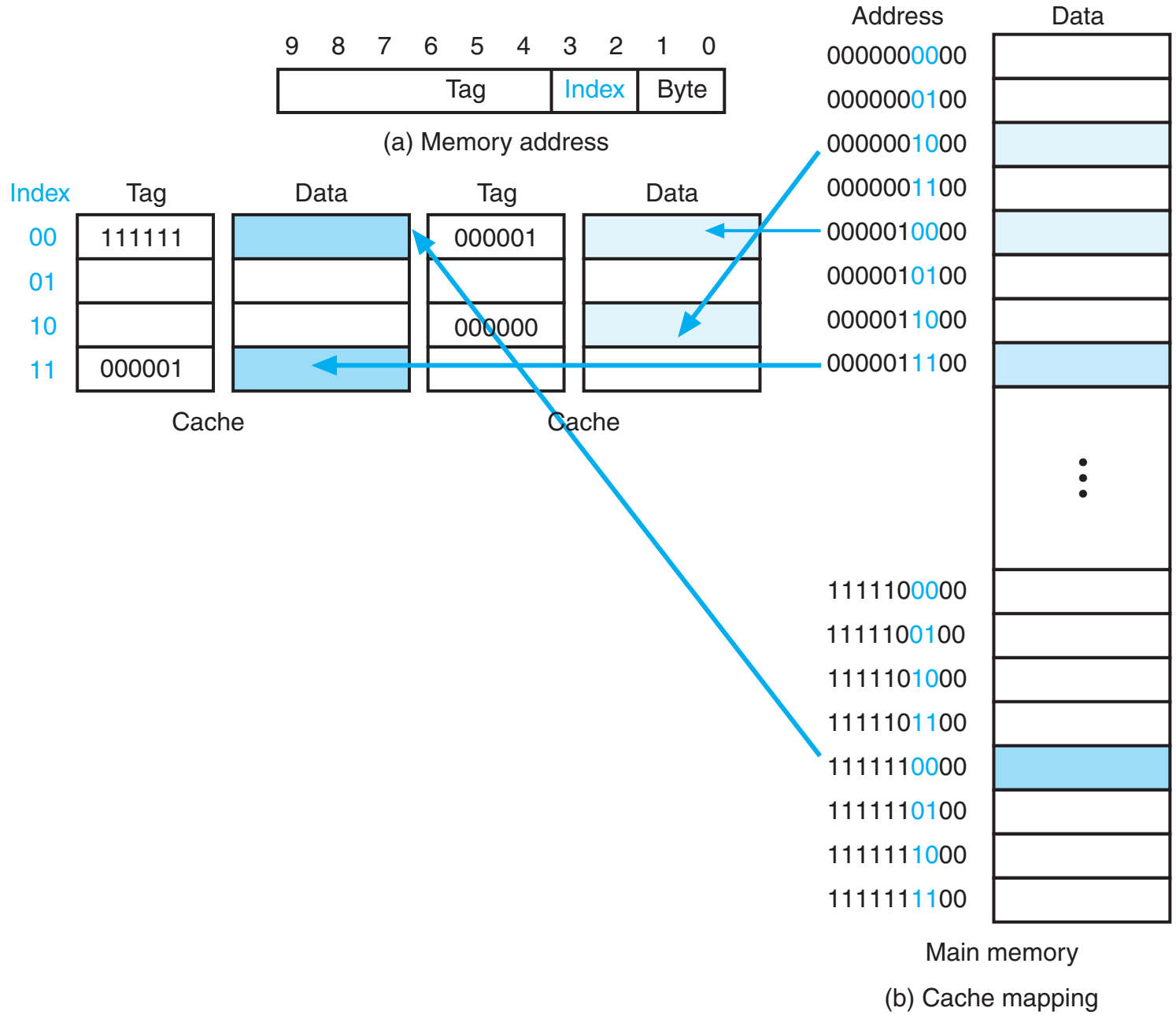

Fig. 12-6 Two-way Set-associative Cache

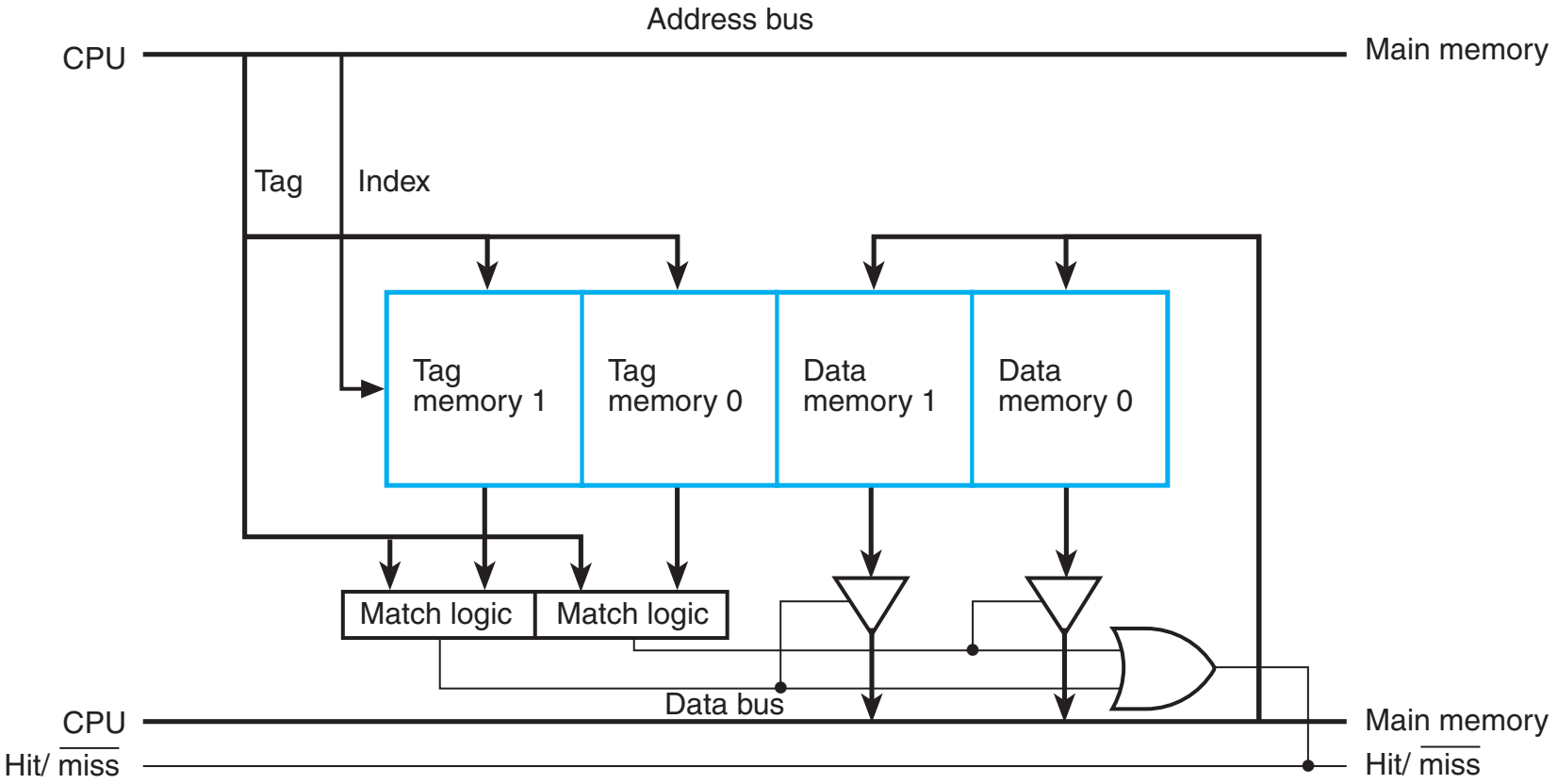

Fig. 12-7 Partial Hardware Block Diagram for Set-associative Cache

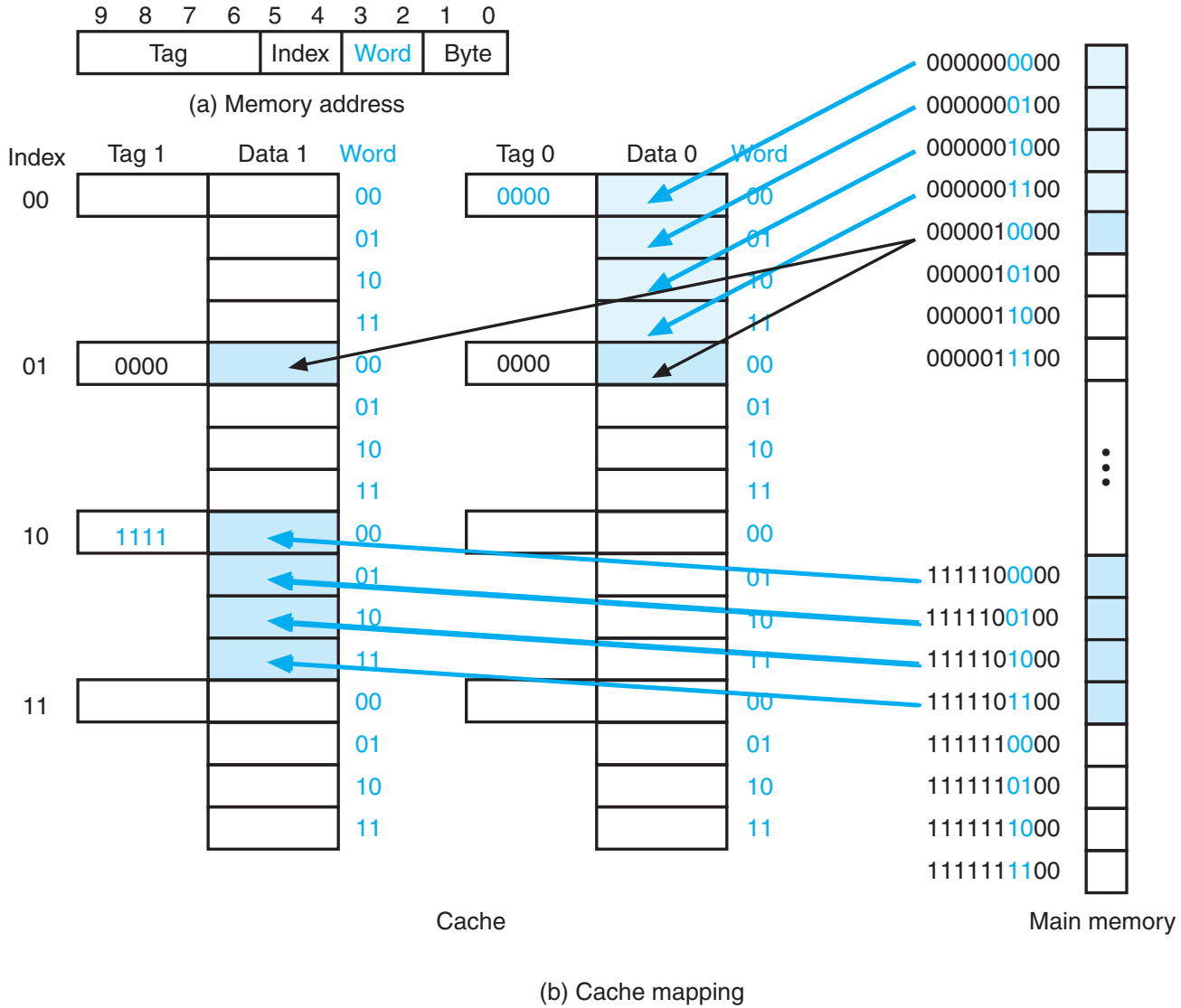

Fig. 12-8 Set-associative Cache with 4-word Lines

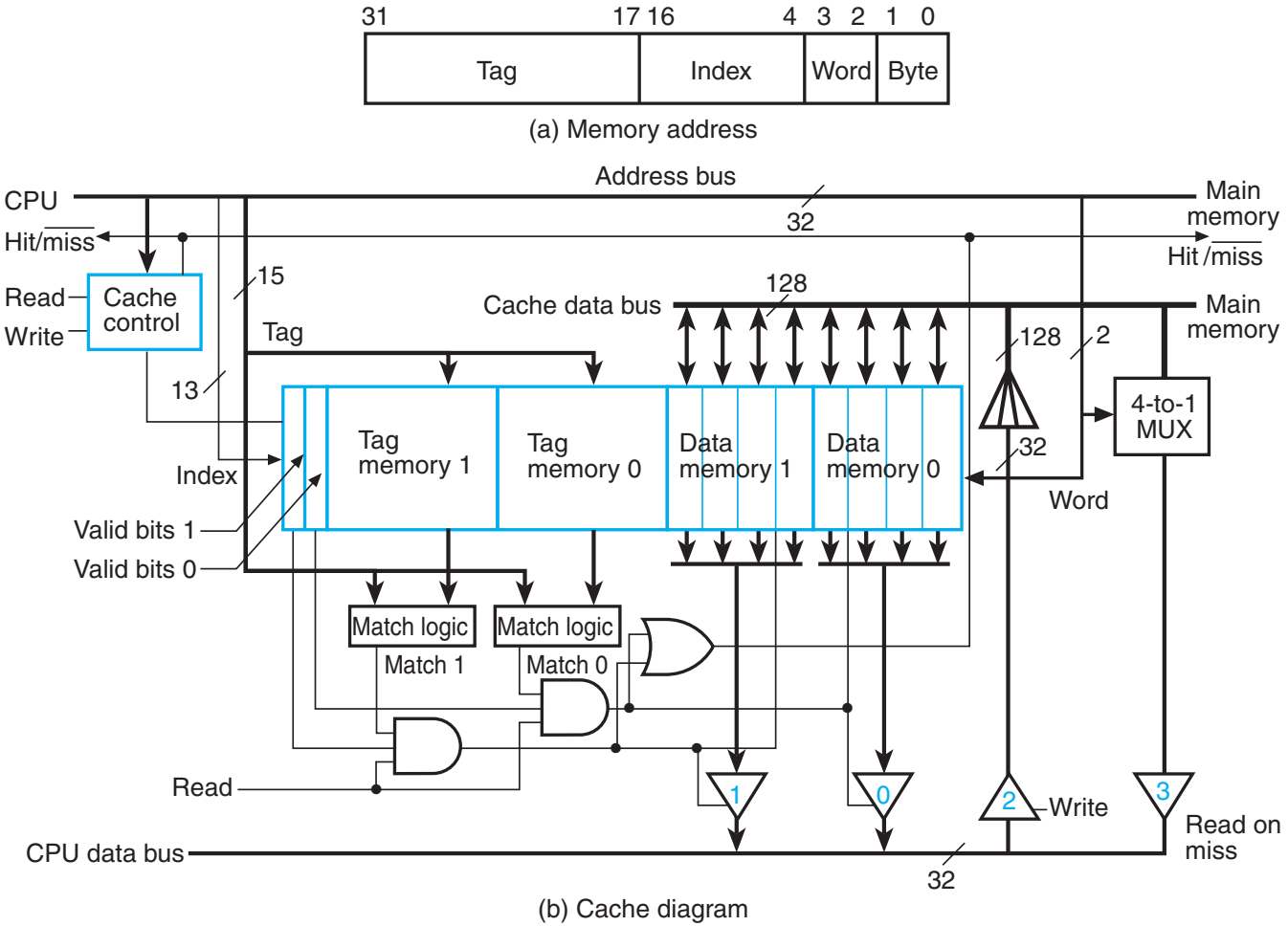

Fig. 12-9 Detailed Block Diagram for 256K Cache

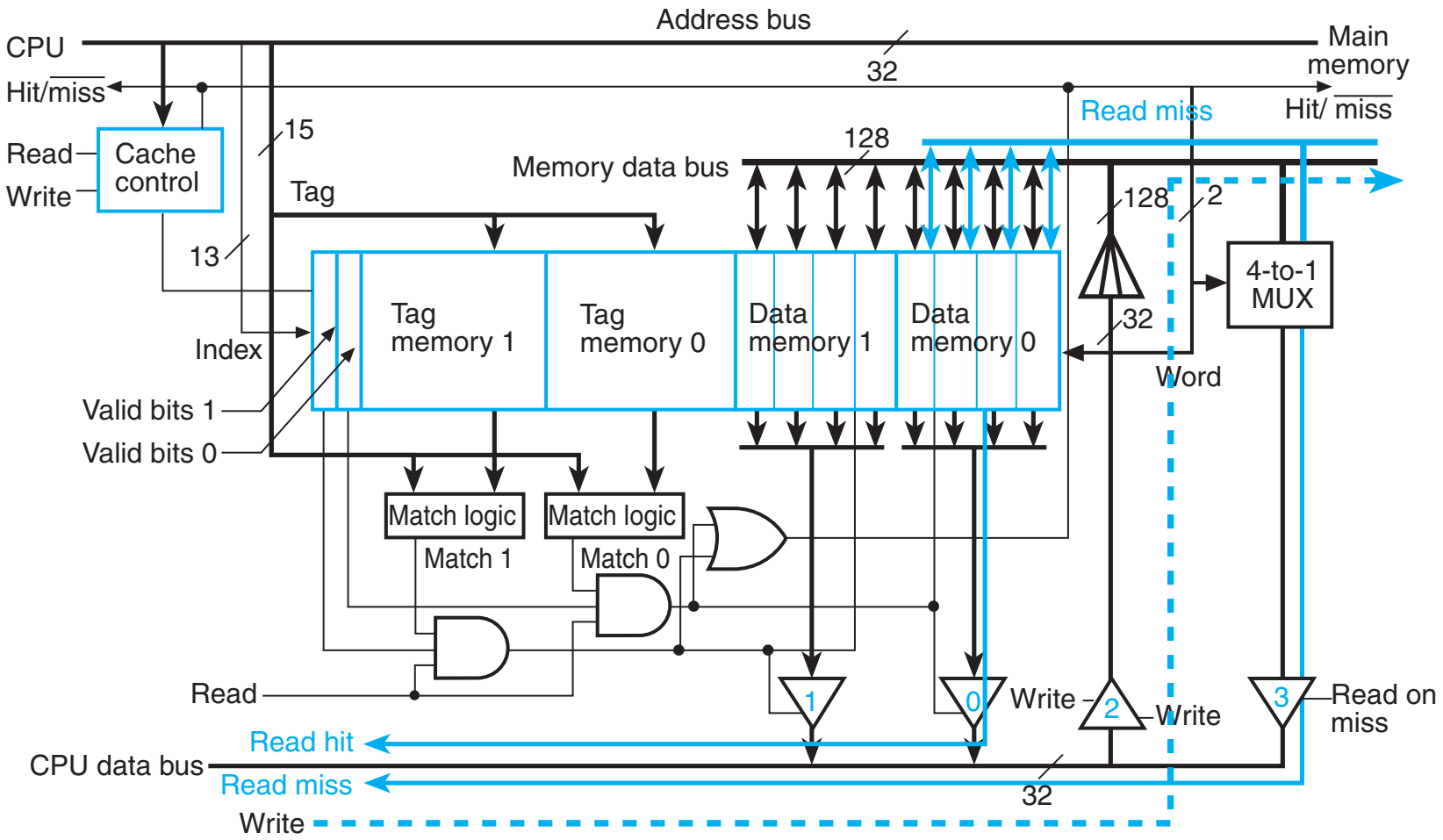

Fig. 12-10 256K Cache: Read and Write Operations

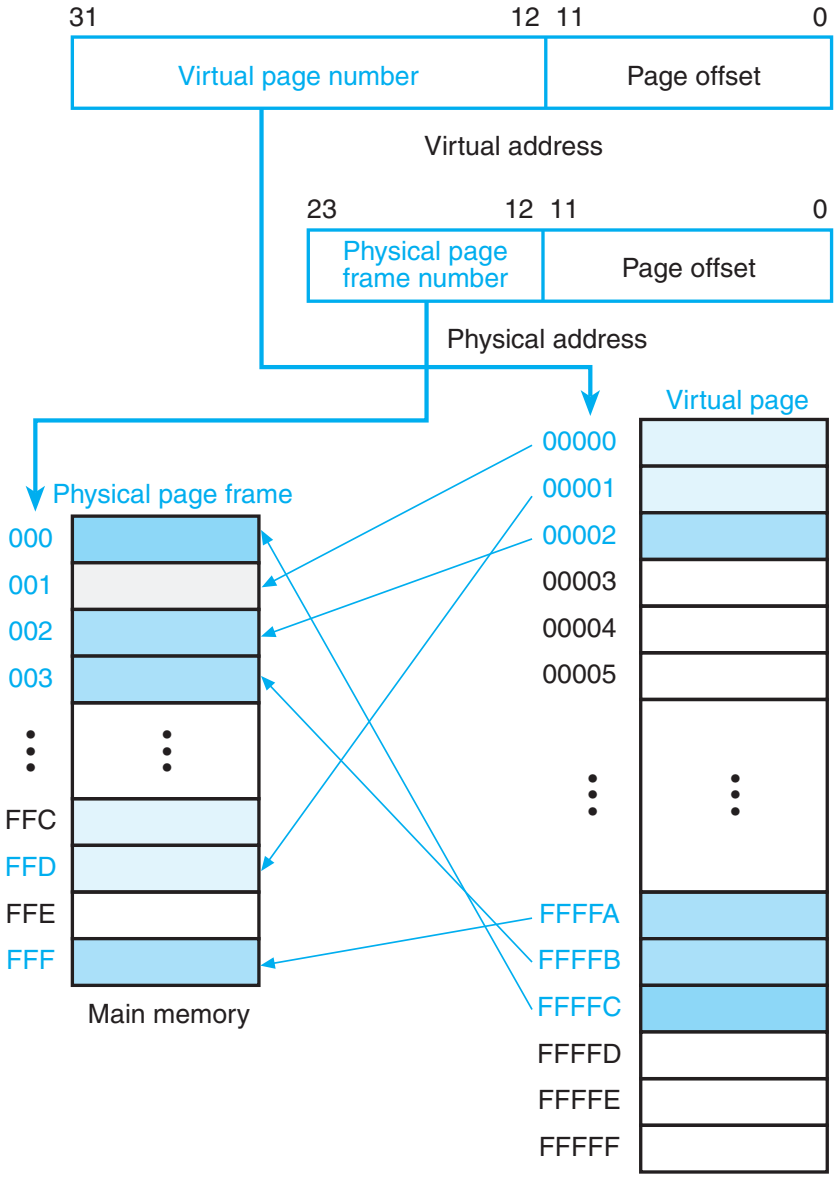

Fig. 12-11 Virtual and Physical Address Fields and Mapping

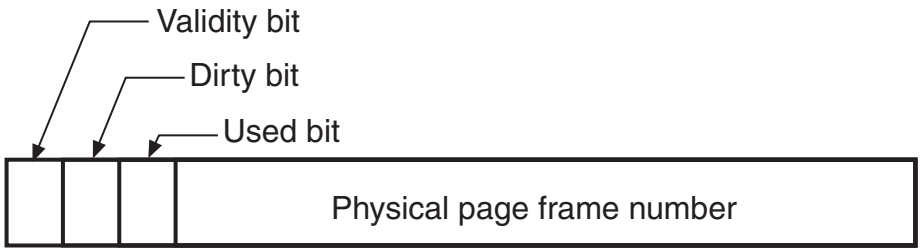

Fig. 12-12 Format for Page Table Entries

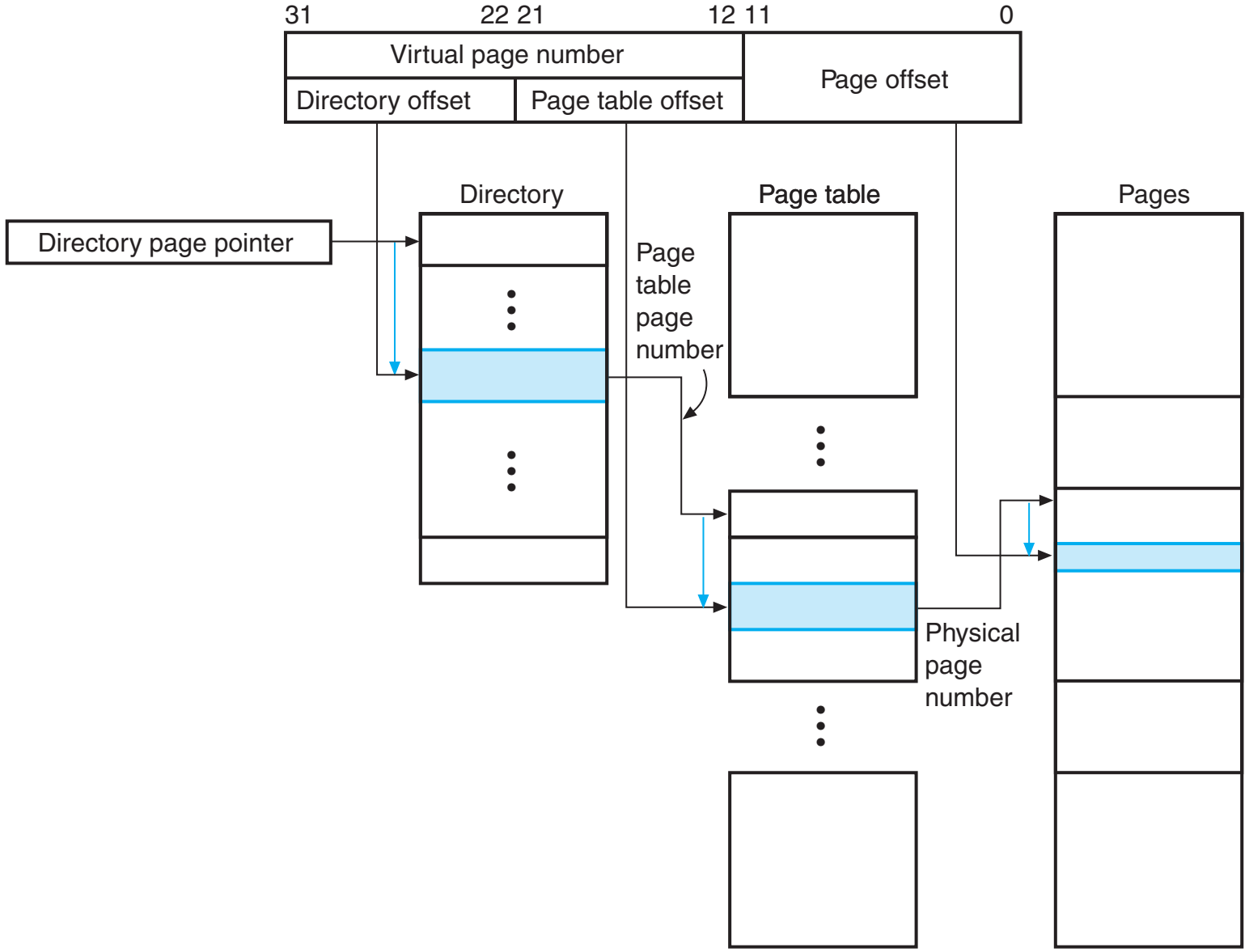

Fig. 12-13 Example of Page Table Structure

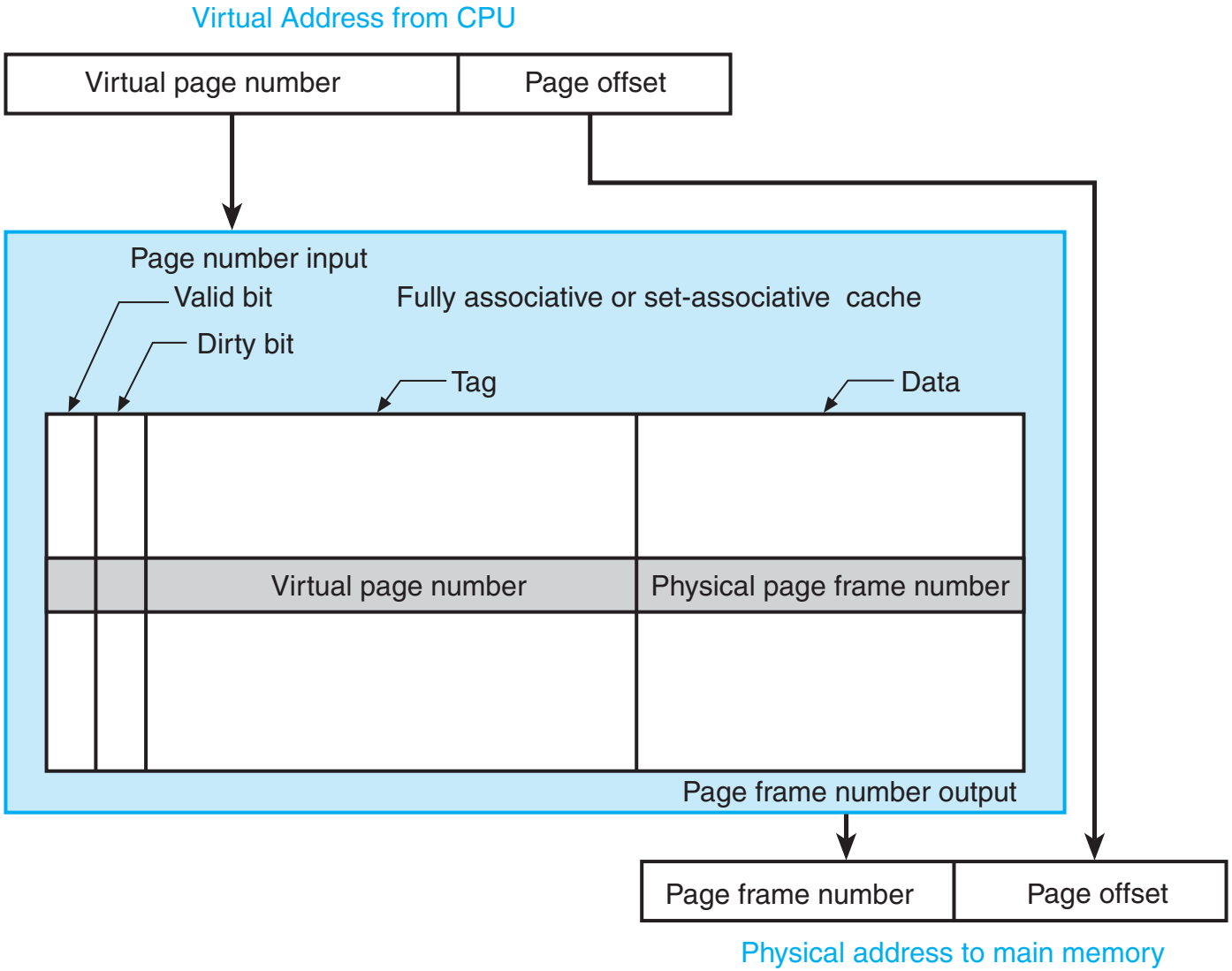

Fig. 12-14 Example of Translation Lookaside Buffer