

Fig. 12-1 Memory Hierarchy

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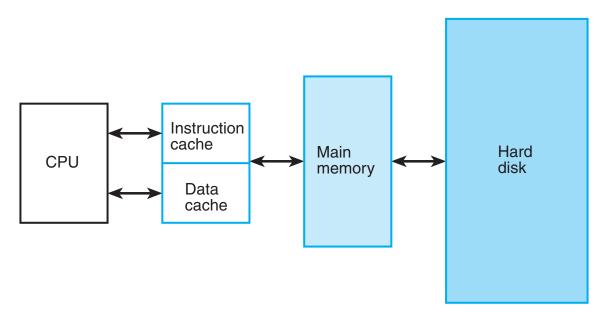
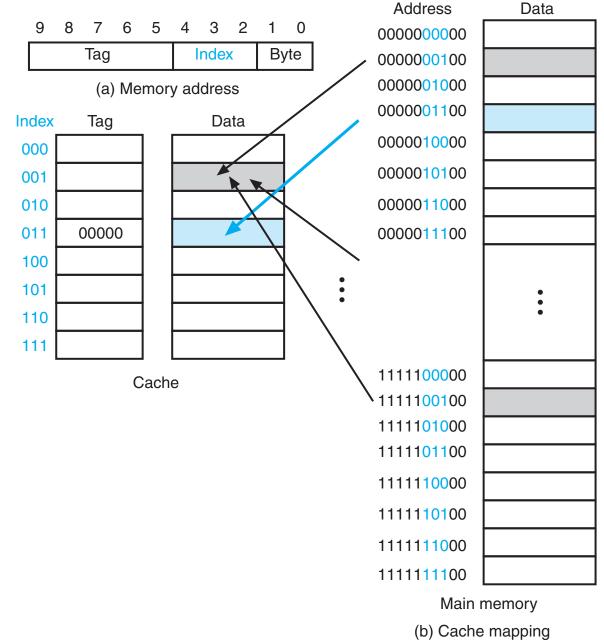


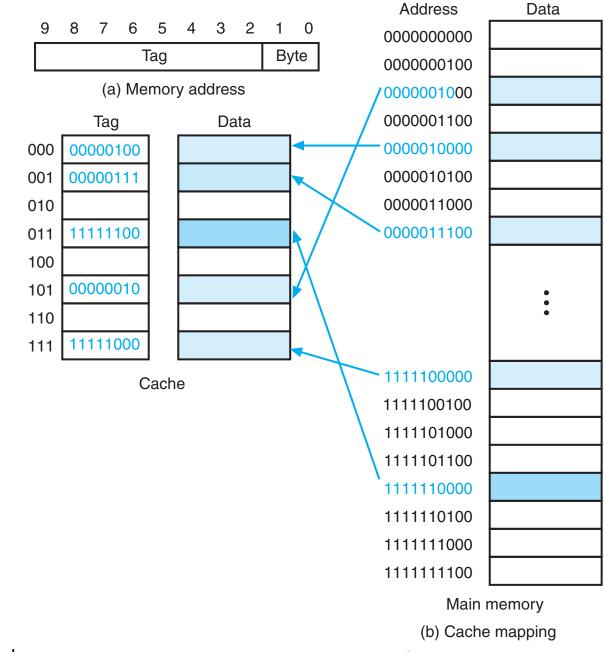
Fig. 12-2 Example of Memory Hierarchy

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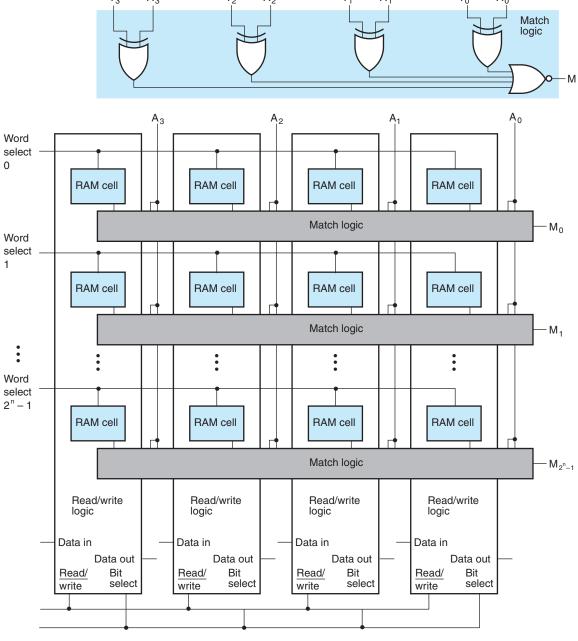
Fig. 12-3 Direct Mapped Cache



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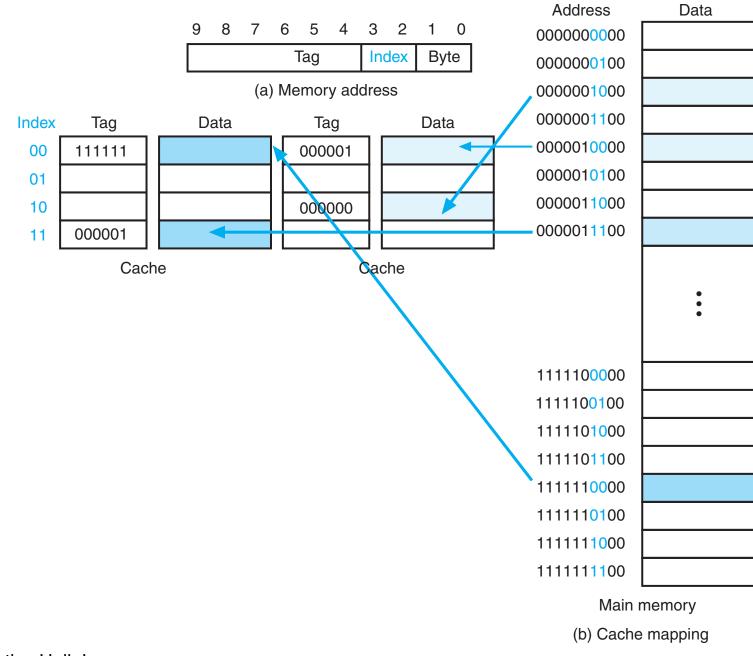
Fig. 12-4 Fully Associative Cache



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Fig. 12-5 Associative Memory for 4-bit Tags

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© 2001 Prentice Hall, Inc. Fig. 12-6 Two-way Set-associative Cache

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LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 2e, Updated.

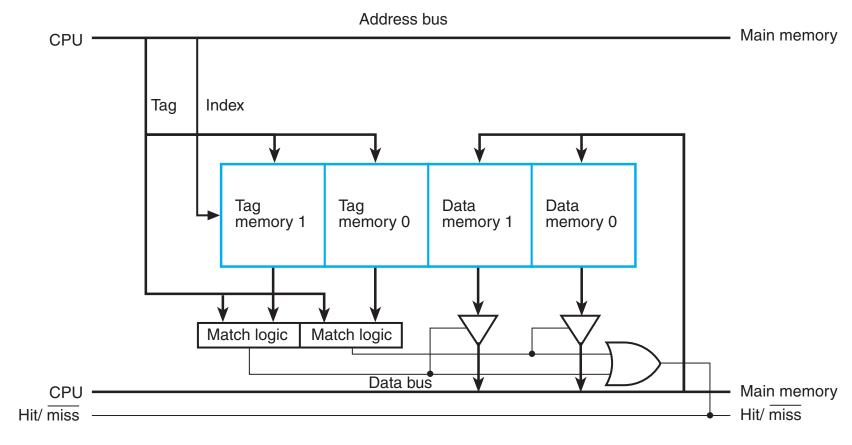


Fig. 12-7 Partial Hardware Block Diagram for Set-associative Cache

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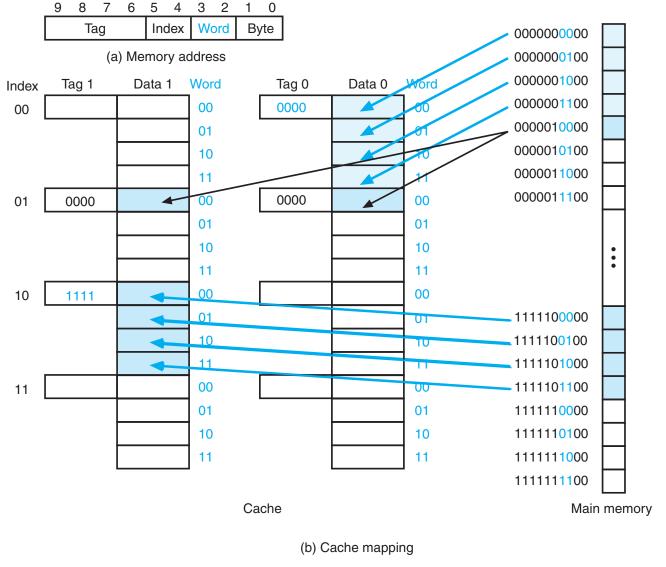


Fig. 12-8 Set-associative Cache with 4-word Lines

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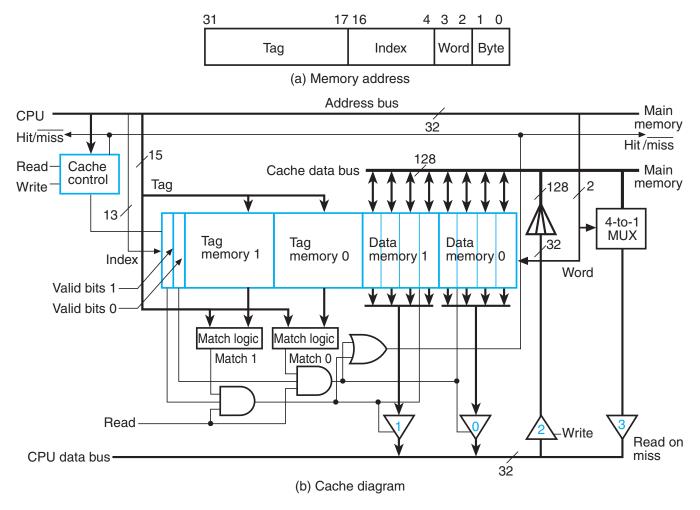


Fig. 12-9 Detailed Block Diagram for 256K Cache

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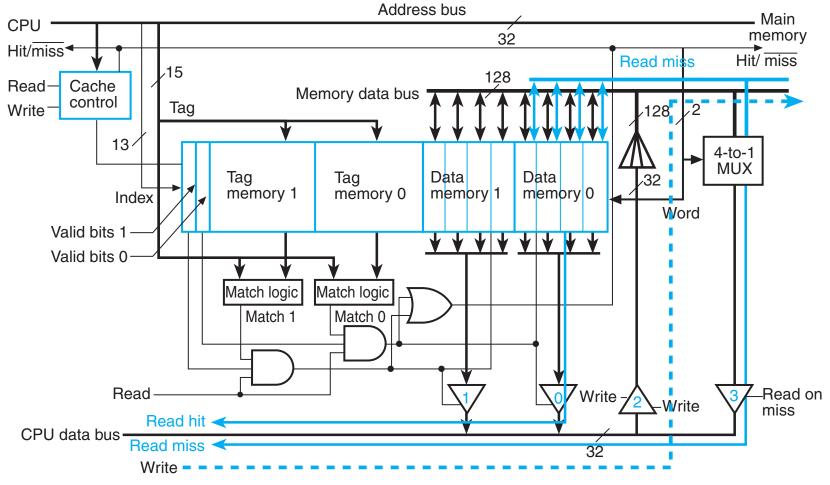


Fig. 12-10 256K Cache: Read and Write Operations

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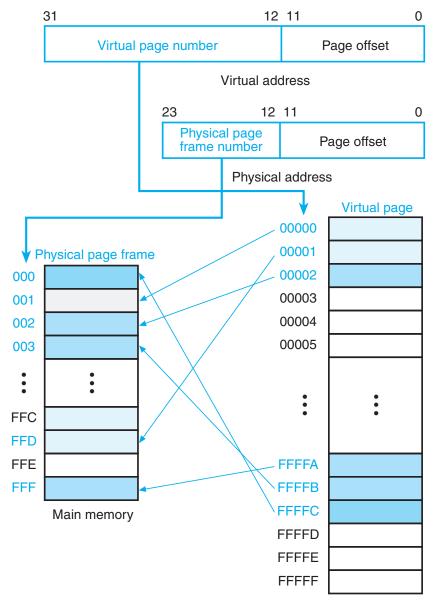


Fig. 12-11 Virtual and Physical Address Fields and Mapping

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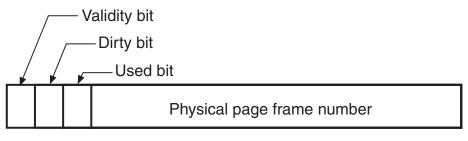


Fig. 12-12 Format for Page Table Entries

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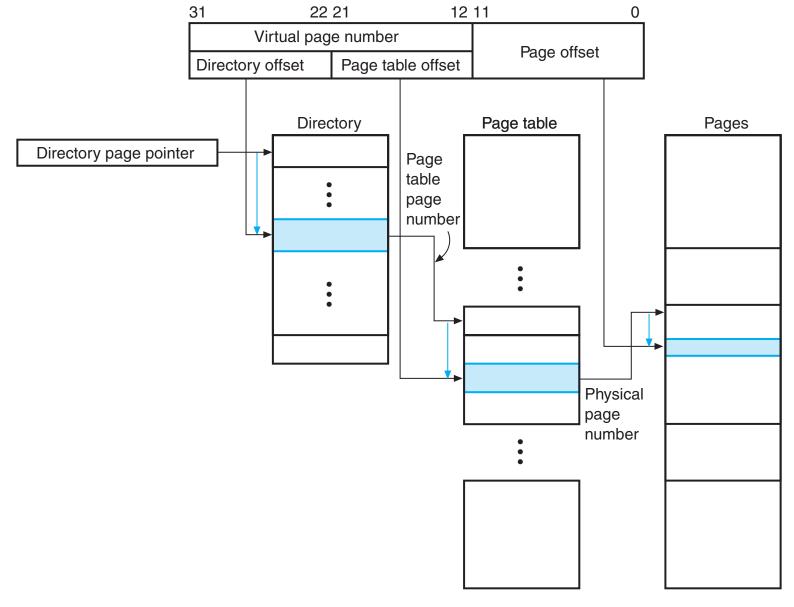
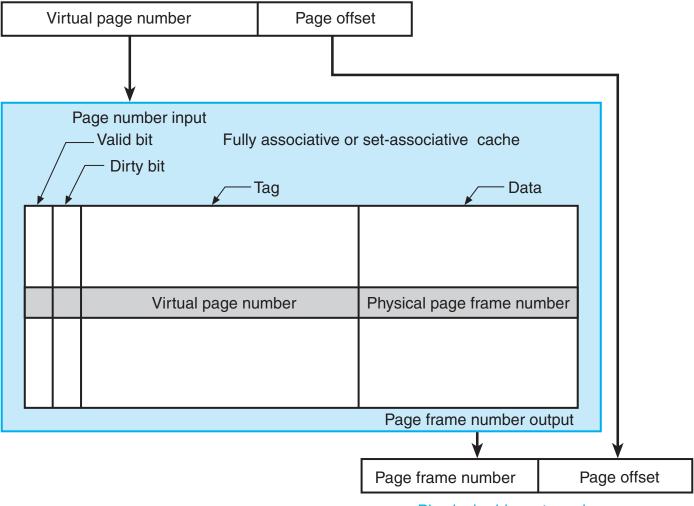


Fig. 12-13 Example of Page Table Structure

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## Virtual Address from CPU



Physical address to main memory

Fig. 12-14 Example of Translation Lookaside Buffer

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