به نام خدا

علی عطاءاللهی ۸۱۰۱۹۹۴۶۱

علی هدائی ۸۱۰۱۹۹۵۱۳

تمرین کامپیوتری 3 معماری کامپیوتر

قالب دستورات:

R-type:

opcode	Rs	Rt	Rd	Sh	func
[31:26]	[25:21]	[20:16]	[15:11]	[10:6]	[5:0]

addi:

opcode	Rs	Rt	data
[31:26]	[25:21]	[20:16]	[15:0]

slti:

opcode	Rs	Rt	data
[31:26]	[25:21]	[20:16]	[15:0]

Memory_refrence (lw , sw) :

opcode	Rs	Rt	adr
[31:26]	[25:21]	[20:16]	[15:0]

j:

opcode	adr
[31:26]	[25:0]

jal:

opcode	adr
[31:26]	[25:0]

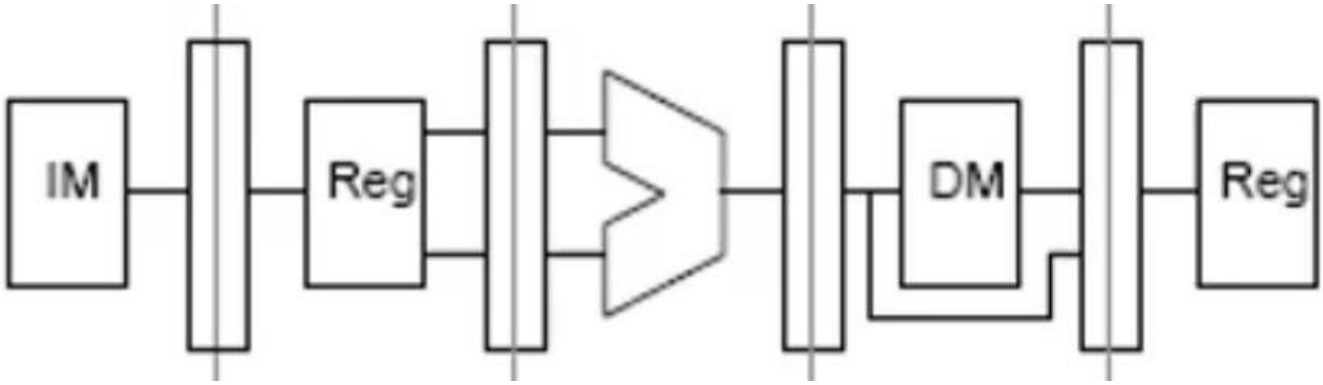
jr:

opcode	Rs	X
[31:26]	[25:21]	[20:0]

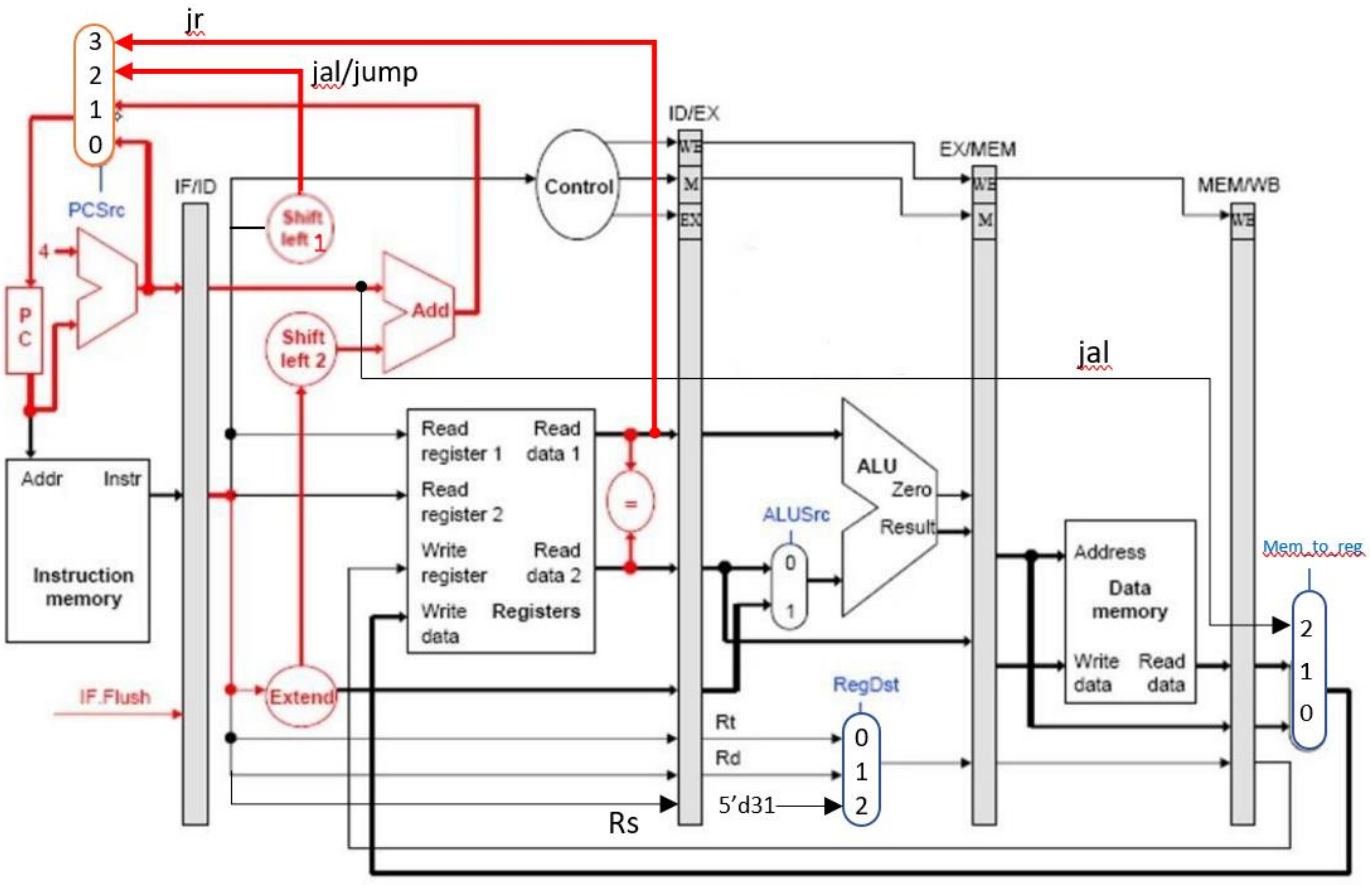
beq:

opcode	Rs	Rt	L
[31:26]	[25:21]	[20:16]	[15:0]

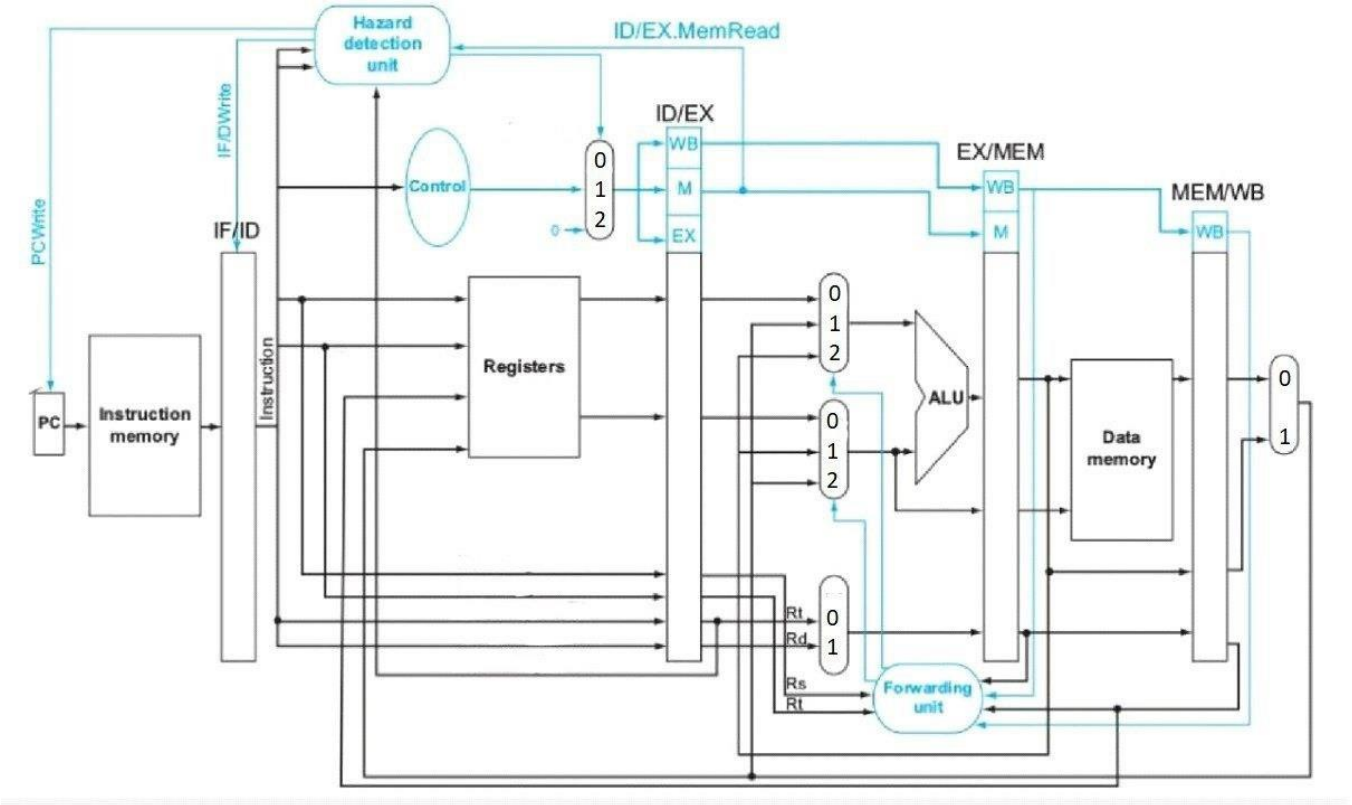
scheme:



Datapath without controller path :



datapath with controller:



controller signals:

```
    always @(opcode)
    begin
        {reg_dst, mem_to_reg, reg_write, alu_src, mem_read, mem_write, pc_src, alu_op,
IFflush} = 13'd0;
        case (opcode)
            `R_type : {reg_dst, reg_write, alu_op} = {2'b01, 1'b1, 2'b10};
            `Lw : {alu_src, mem_to_reg, reg_write, mem_read} = {1'b1, 2'b01, 1'b1, 1'b1};
            `Sw : {alu_src, mem_write} = 2'b11;
            `Beq : {pc_src, IFflush} = {1'b0, operands_equal, operands_equal};
            `Addi : {reg_write, alu_src} = 2'b11;
            `J : {pc_src, IFflush} = {2'b10, 1'b1};
            `Jal : {reg_dst, mem_to_reg, pc_src} = {2'b10, 2'b10, 2'b10};
            `Jr: {pc_src} = {2'b11};
            `Slti: {alu_src, reg_dst, reg_write, alu_op, mem_to_reg} = {1'b1, 2'b00, 1'b1,
2'b11, 2'b00};
        endcase
    end
```

alu controller :

```
    always @(ALUop,func) begin
        op=3'b000;
        case (ALUop)
            2'b00: op=3'b010;//add
            2'b01: op=3'b110;//sub
            2'b10: begin
                op=3'b000;
                case (func)
                    `Add: op=3'b010;
                    `Sub: op=3'b110;
                    `And: op=3'b000;
                    `Or:  op=3'b001;
                    `Slt: op=3'b111;
                    default: op=3'b110;
                endcase
            end
            2'b11: op=3'b111;//Slt
            default: op=3'b110;
        endcase

    end
```

Pseudocode:

```
max = a[0]
maxIndex = 0
for (int i = 1 ; i < 20 ; i++)
{
    if (a[i] > max)
    {
        max = a[i]
        maxIndex = i
    }
}
```

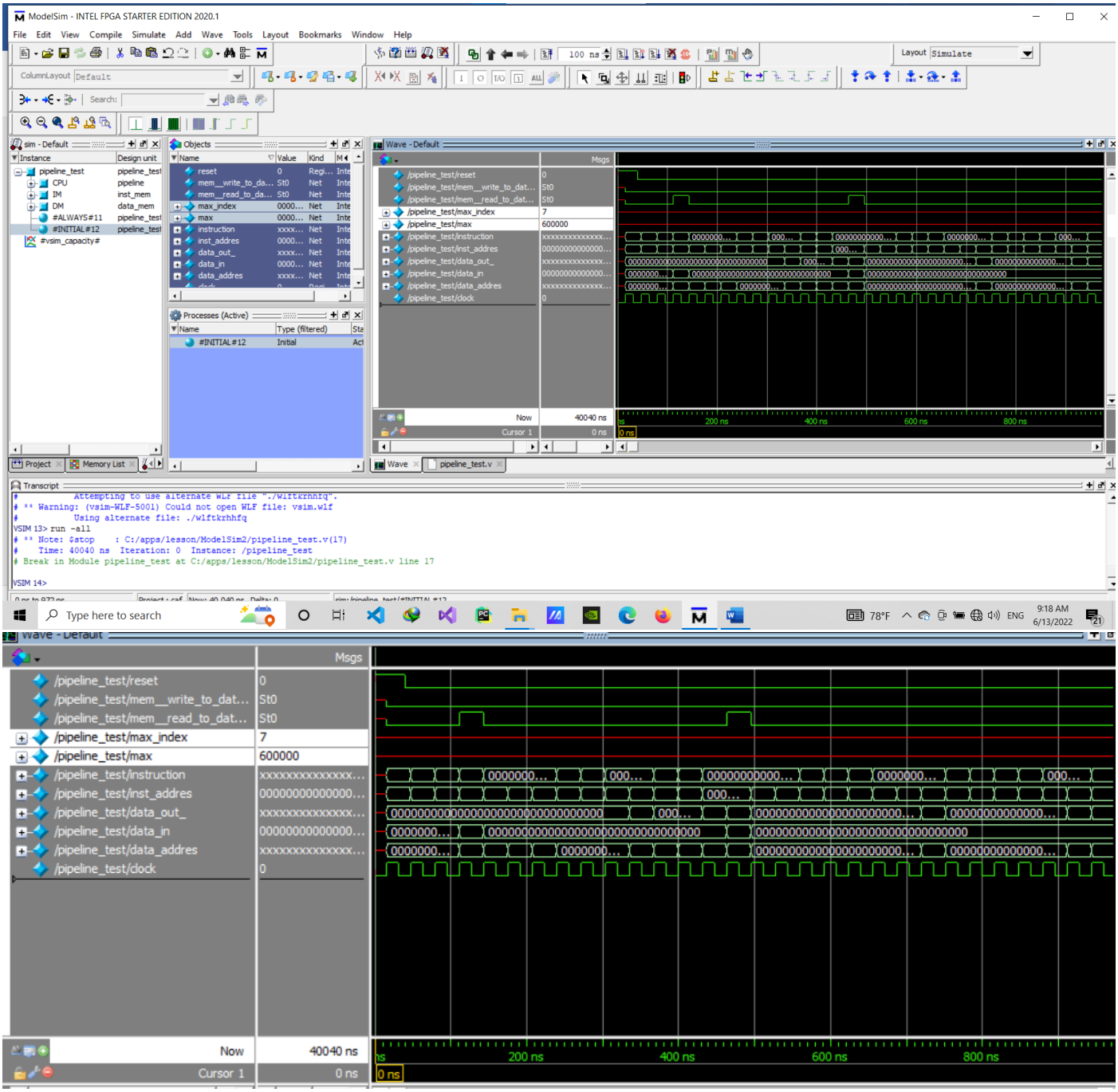
assembly code:

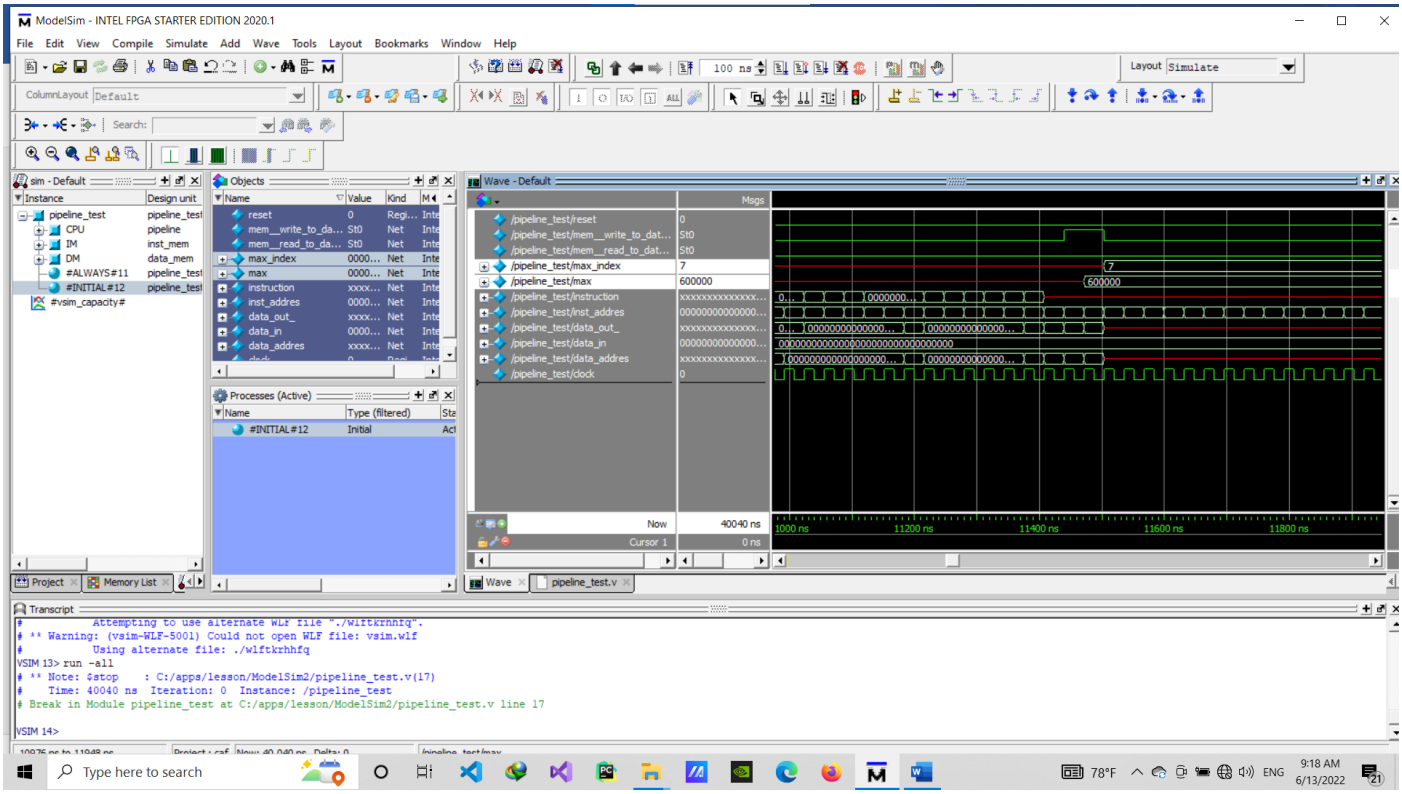
```
        LW R4 , 1000 ( R0 )
        ADDi R5 , R0 , 0
        ADDi R1 , R0 , 1
        ADDi R2 , R0 , 20
        NOP
        NOP
        NOP
iLoop:  Beq R1 , R2 , A_LOOP
        ADD R3 , R0 , R1
        ADD R3 , R3 , R3
        ADD R3 , R3 , R3
        LW R6 , 1000 ( R3 )
        SLT R10 , R4 , R6
        NOP
        NOP
        NOP
        Beq R10 , R0 , E_Loop
        ADD R4 , R0 , R6
        ADD R5 , R0 , R1
E_Loop: ADDi R1 , R1 , 1
        NOP
        NOP
        NOP
        J iLoop
A_Loop: SW R4 , 2000 ( R0 )
        SW R5 , 2004 ( R0 )
```

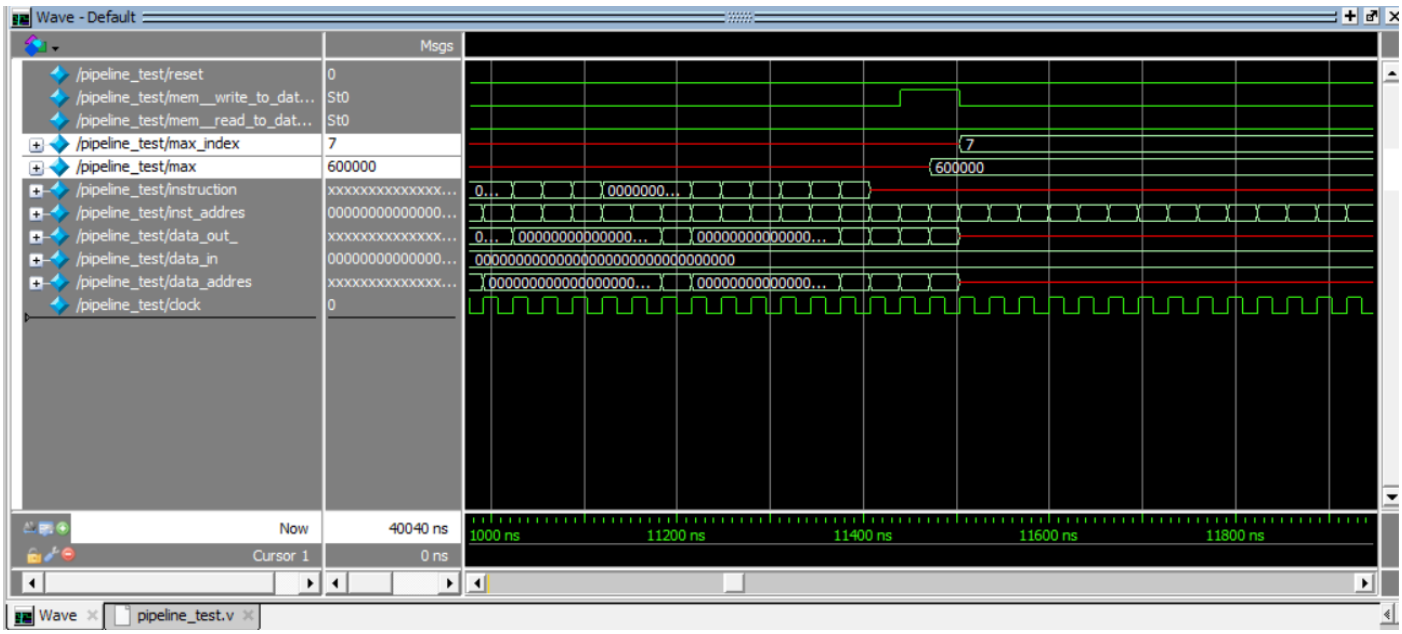
array of random numbers table:

index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
value	10	3000	12	15	31	29	50	600000	3500	90	120	5	400	35	16	17	670	97	330	11

screenshots:


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
Using alternate file: ./wlftkrhhfq
VSIM 13> run -all
** Note: $stop : C:/apps/lesson/ModelSim2/pipeline_test.v(17)
Time: 40040 ns Iteration: 0 Instance: /pipeline_test
Break in Module pipeline_test at C:/apps/lesson/ModelSim2/pipeline_test.v line 17
VSIM 14>
Type here to search
78°F
ENG
9:18 AM
6/13/2022
Wave - Default
Msgs
/pipeline_test/reset
/pipeline_test/mem__write_to_dat...
/pipeline_test/mem__read_to_dat...
/pipeline_test/max_index
/pipeline_test/max
/pipeline_test/instruction
/pipeline_test/inst_addres
/pipeline_test/data_out_
/pipeline_test/data_in
/pipeline_test/data_addres
/pipeline_test/clock
Now
40040 ns
Cursor 1
0 ns
200 ns
400 ns
600 ns
800 ns


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/pipeline_test/reset
/pipeline_test/mem__write_to_dat...
/pipeline_test/mem__read_to_dat...
/pipeline_test/max_index
/pipeline_test/max
/pipeline_test/instruction
/pipeline_test/inst_addres
/pipeline_test/data_out_
/pipeline_test/data_in
/pipeline_test/data_addres
/pipeline_test/clock
Now
Cursor 1
1000 ns
11200 ns
11400 ns
11600 ns
11800 ns
Transcript
** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
Using alternate file: ./wlftkrhhfq
VSIM 13> run -all
** Note: $stop : C:/apps/lesson/ModelSim2/pipeline_test.v(17)
Time: 40040 ns Iteration: 0 Instance: /pipeline_test
Break in Module pipeline_test at C:/apps/lesson/ModelSim2/pipeline_test.v line 17
VSIM 14>
Type here to search
78°F
ENG
9:18 AM
6/13/2022


Wave - Default
/pipeline_test/reset
/pipeline_test/mem__write_to_dat...
/pipeline_test/mem__read_to_dat...
/pipeline_test/max_index
/pipeline_test/max
/pipeline_test/instruction
/pipeline_test/inst_addres
/pipeline_test/data_out_
/pipeline_test/data_in
/pipeline_test/data_addres
/pipeline_test/clock
Now
Cursor 1
1000 ns
11200 ns
11400 ns
11600 ns
11800 ns
Wave
pipeline_test.v