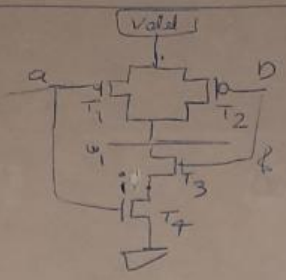
Ali Ataollahi 810199461 CA1

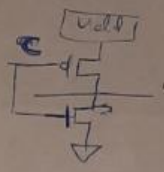
In the name of God

1) switch level show

NAND



NOT



nmos#(3,5,7) pmos#(4,7,9)

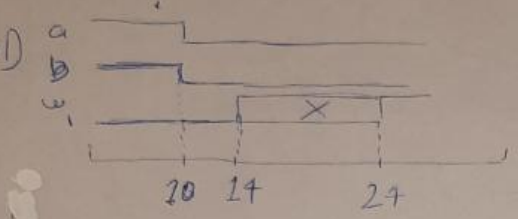
a) NAND: —D○— NOT —▷○— / b) NAND* To1 → max(4, 2×7) = 14 ab: 11 → 01

To 0 → max(2×5, 9) = 10 ab: 00 → 11

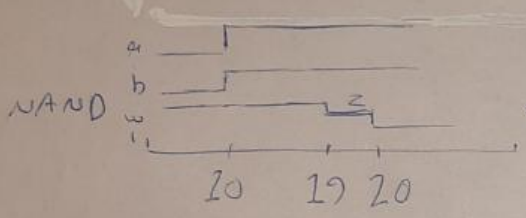
NOT To1 → max(4, 4) = 7 a: 1 → 0

To 0 → max(3, 9) = 9 a: 0 → 1

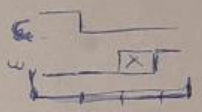
NAND



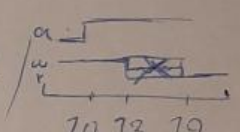
← To 1



← To 0 / NOT



To 1 /



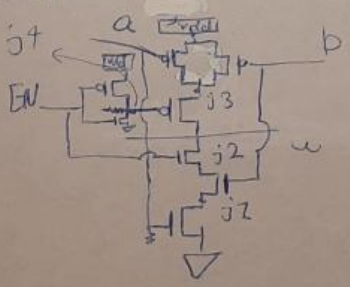
NOT To 0

c) ...

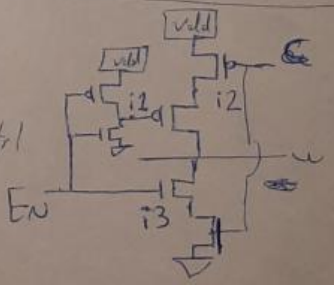
e) there's no diffrece (in first of time period output is z (in Systemrerilog) because nmos and pmos still doesn't Conduct but that's not necessary

2) switch level:

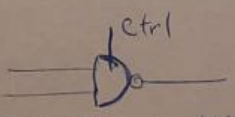
NAND gate with ctrl



NOT gate with ctrl

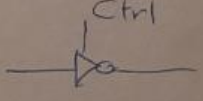


a) NAND



nmos#(3,5,7) pmos#(4,7,7)

NOT



NAND if1

b) To1: max(3×7, 2×4) = 21

abEN: 111 → 011

To 0: max(2×9, 3×5) = 18

abEN: 001 → 111

To Z: max(7, 7+9) = 16

abEN: 011 → 000

NOT if1 2×7

To1: max(9, 9+4) = 14

CEN: 11 → 01

To 0: max(2×3, 2×9) = 18

CEN: 01 → 11

To Z: max(3+7, 7+9) = 16

CEN: 01 → 00

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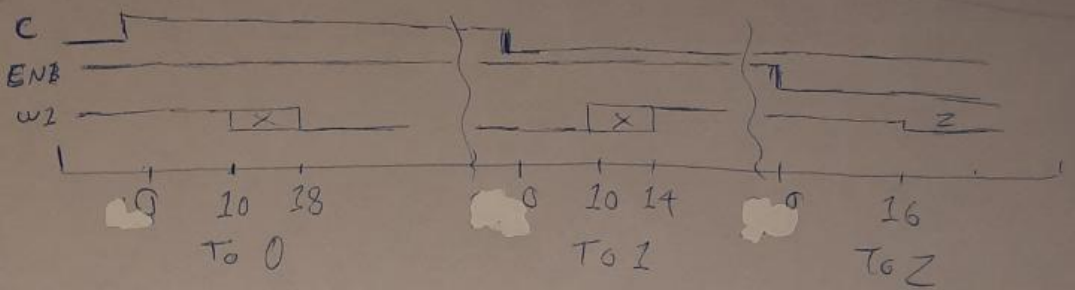
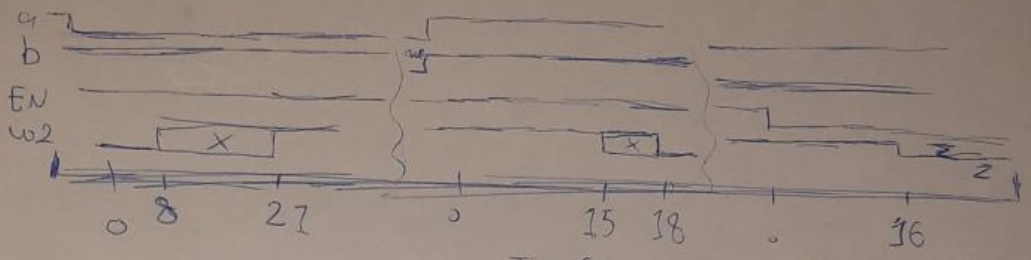
NOT_ctrl



NAND_ctrl



C...

e) there is no diffrence (like question 1)

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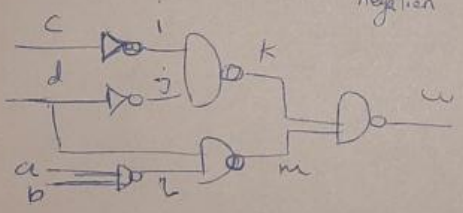
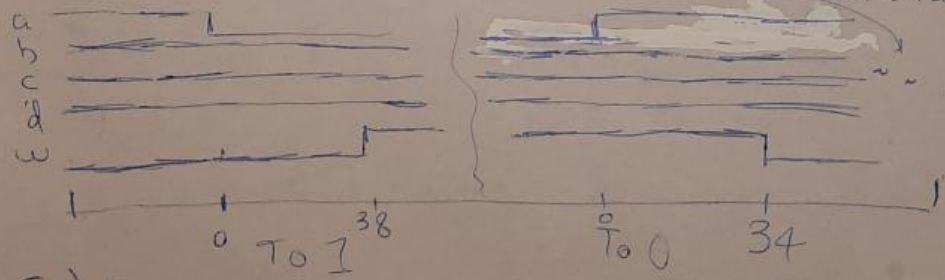
3) $w = \bar{d} \cdot \bar{c} + d \cdot (\overline{a \cdot b})$ $\xrightarrow[\text{negation}]{\text{double}}$ $\overline{\bar{d} \cdot \bar{c}} \cdot \overline{d \cdot (\overline{a \cdot b})}$

a) use NOT and NAND



~~NAND~~ nand #(14, 10) ~~NOT~~ not #(7,9)

a) To 1 abcd: 1111 → 0111 (38) → 14+14+10 To 0 abcd: 0111 → 1111 (34) → 14+10+10



In system verilog it's 33

c) o e o

~~e) same 1 3~~

d) in initial of ww it's z because it spends time to get 1 or 0 value / In system verilog to 1 is 31' but ther 38 and to 0 is 33 but there 33

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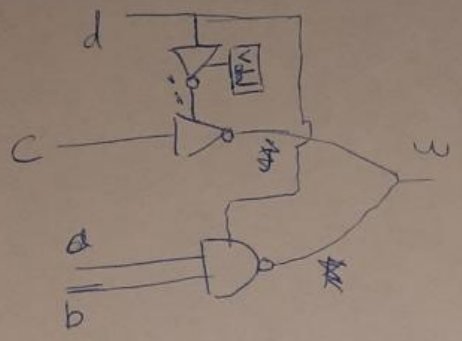
4)

a)



nandif1#(21,18,16) notif1#(21,18,16)

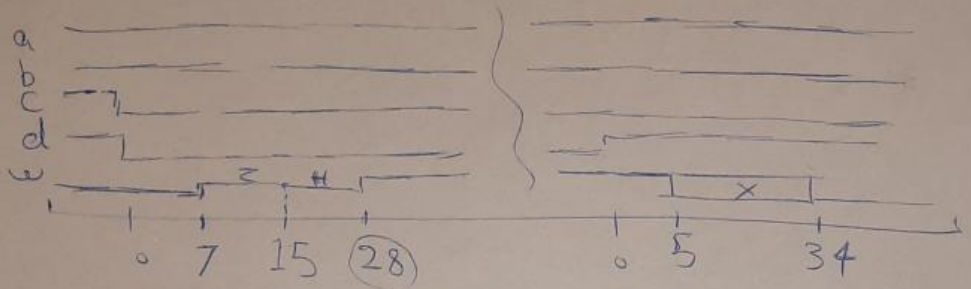
b) To 1 : abcd : 1101 → 1100

14+14 = 28

but in verilog it's 27

To 0 : abcd : 1100 → 1101

16+18 = 34



in system verilog it's 27

c) ...

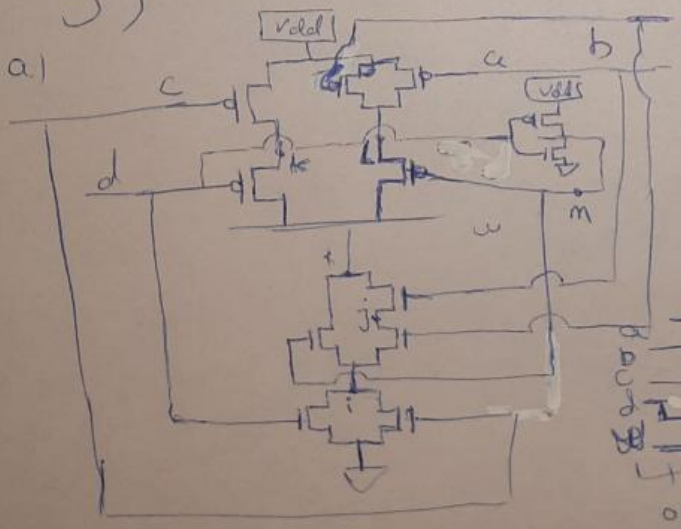
d) To 1 in hand calculate is 28 but in system verilog is 27

5)

$w = \bar{d}\cdot\bar{c} + d\cdot(\bar{a}+\bar{b})$

nmos #(3,5,7) pmos #(4,7,9)

a)



b) To 1 : abcd : 1101 → 1100

max(3×7, 4) = 21

To 0 : abcd : 1100 → 1110

max(2×9, 3×3) = 18

c) ...

d) There is no diffrence

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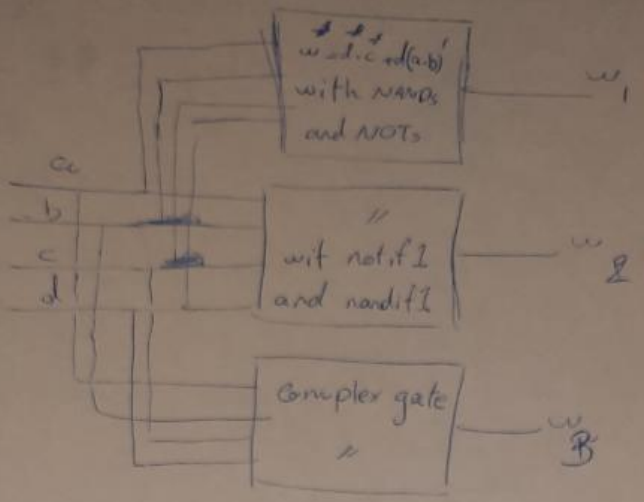
6) a) B



b)

we consider systemverilog delays

c) ~~Timing~~ timing : Circuits part3 #(31,34) part4 #(28,34) part5 #(21,28)

circuits part5 has best (lowest) delays

number of transistors: part 3: 2×2 + 4×4 = 20 (2)
part 4: 2×6 + 8 = 20 (3) → order as lowest power consumption
part 5: 6+6 = 12 (1)

part 5 has lowest power consumption because has less transistors and less direct path between vdd and gnd (supply 1 and 0). after that part 4 is considered. because has less gates and direct path bitween supply 1 and 0

explain: I look to number of gates because is each gate we have one direct conduct path bitween gnd and vdd. and there a momentary power consumption)

part 5 has one direct conduct path between gnd and vdd and because of that has lowest power consumption. but part 4 has more gates and direct path and placed in 2 rank. after that part 3 has most power consumption because when d is 1 and we have static power consumption not momentary like part 3 and 5. because has more gates