به نام خد ا

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1:

Diagram, schematic

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Code:

`timescale 1ns/1ns

module MOORE10110 (input clk,rst,j,output w);

    logic [2:0] ns,ps;

    parameter [2:0] A=3'b000,B=3'b001,C=3'b010,D=3'b011,E=3'b100,F=3'b101;

    always@(ps,j) begin

        ns=3'b000;

        case(ps)

            A: ns= j ? B : A;

            B: ns= j ? B : C;

            C: ns= j ? D : A;

            D: ns= j ? E : C;

            E: ns= j ? B : F;

            F: ns= j ? D : A;

            default: ns=A;

        endcase

    end

    assign w= (ps==F) ? 1'b1 : 1'b0;

    always@(posedge clk,posedge rst)begin

        if(rst)

            ps<=A;

        else

            ps<=ns;

    end

endmodule

Tb:

`timescale 1ns/1ns

module CA5\_E1\_TB\_1 ();

    logic clock=0,jj=0,reset=0;

    wire ww1,ww2;

    MOORE10110 xx(clock,reset,jj,ww1);

    E1\_QQ xxx(clock,reset,jj,ww2);

    always #50 clock=~clock ;

    initial begin

        #90 jj=0;

        #100 jj=0;

        #100 jj=1;

        #100 jj=1;

        #100 jj=0;

        #100 jj=1;

        #100 jj=1;

        #100 jj=0;

        #100 jj=0;

        #100 jj=1;

        #100 jj=1;

        #40 reset=1;

        #40 reset=0;

        #20 jj=0;

        #100 jj=1;

        #100 jj=1;

        #100 jj=0;

        #100 jj=0;

        #100 jj=0;

        #200 $stop;

    end

endmodule

Graphical user interface, application, table

Description automatically generatedGraphical user interface, text, application

Description automatically generatedGraphical user interface, text, application

Description automatically generatedGraphical user interface, application

Description automatically generatedA screenshot of a computer

Description automatically generated with medium confidenceGraphical user interface, application

Description automatically generatedGraphical user interface, application

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2:

Diagram, schematic

Description automatically generated

TB:

`timescale 1ns/1ns

module CA5\_E2\_TB ();

    logic clock=0,cnt=1,en=1,reset=0;

    wire ccoo;

    wire[7:0] ww;

    E2\_QQ xxxx(ccoo,clock,en,cnt,reset,ww);

    always #10 clock=~clock ;

    initial begin

        #5000 cnt=1;

        #5000 cnt=0;

        #5000 cnt=1;

        #5000 reset=1;

        #5000 reset=0;

        #10000 $stop;

    end

endmodule

Graphical user interface, text, application

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Description automatically generatedGraphical user interface, application, Excel

Description automatically generatedGraphical user interface, application, Excel

Description automatically generatedGraphical user interface, application

Description automatically generatedGraphical user interface, treemap chart

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3:

Diagram, schematic

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TB:

`timescale 1ns/1ns

module CA5\_E3\_TB ();

    logic serInn=1,clkk=1,resett=0;

    wire serout;

    wire[7:0] ww;

    E3\_QQ xxxxx(serout,serInn,clkk,resett,ww);

    always #10 clkk=~clkk ;

    initial begin

        #4490 resett=0;

#250 resett=1;

#250 resett=0;

        #20 serInn=1;

        #20 serInn=0;

        #20 serInn=1;

        #20 serInn=1;

        #20 serInn=0;

        #10000 $stop;

    end

endmodule

Graphical user interface

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