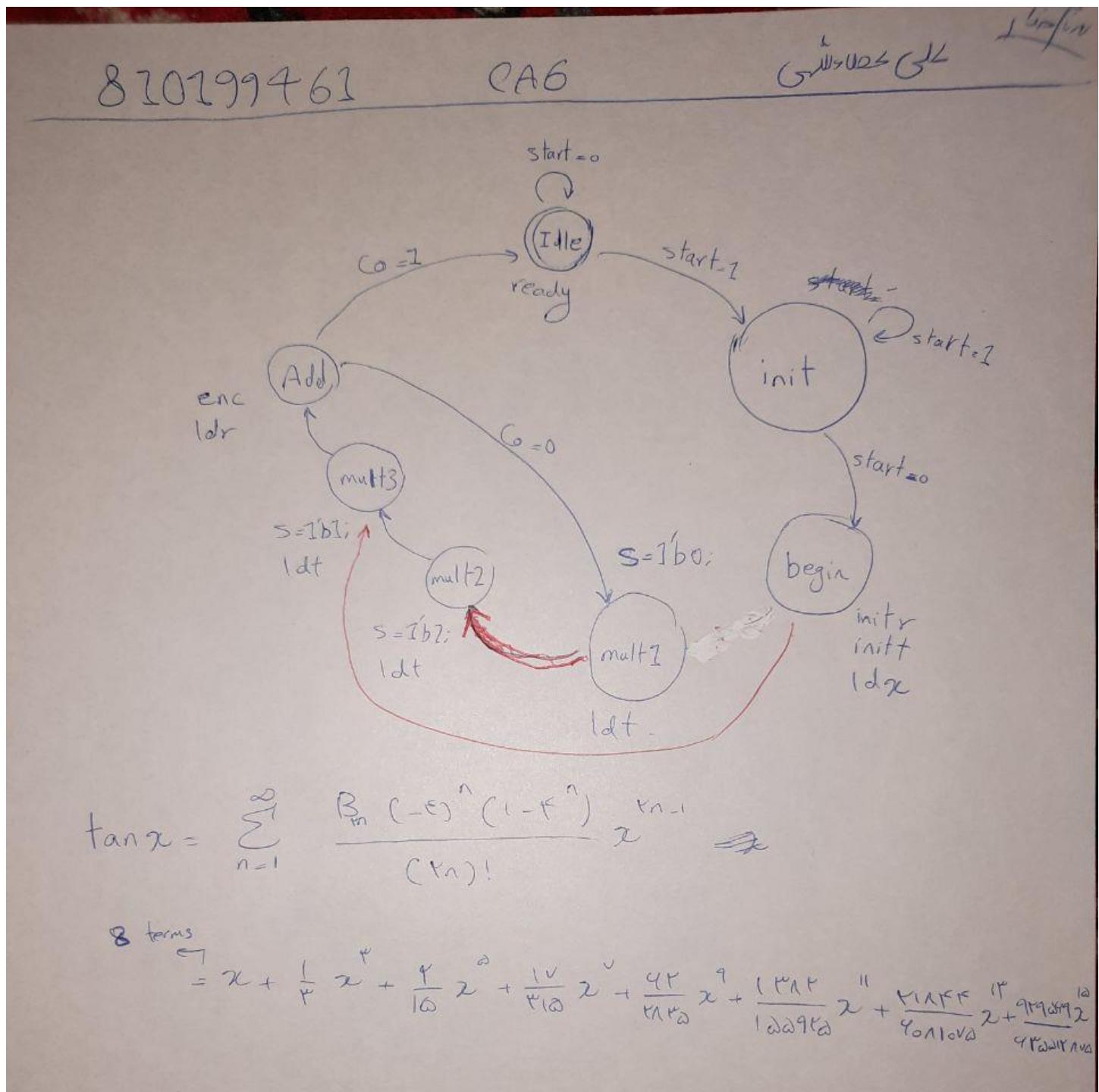
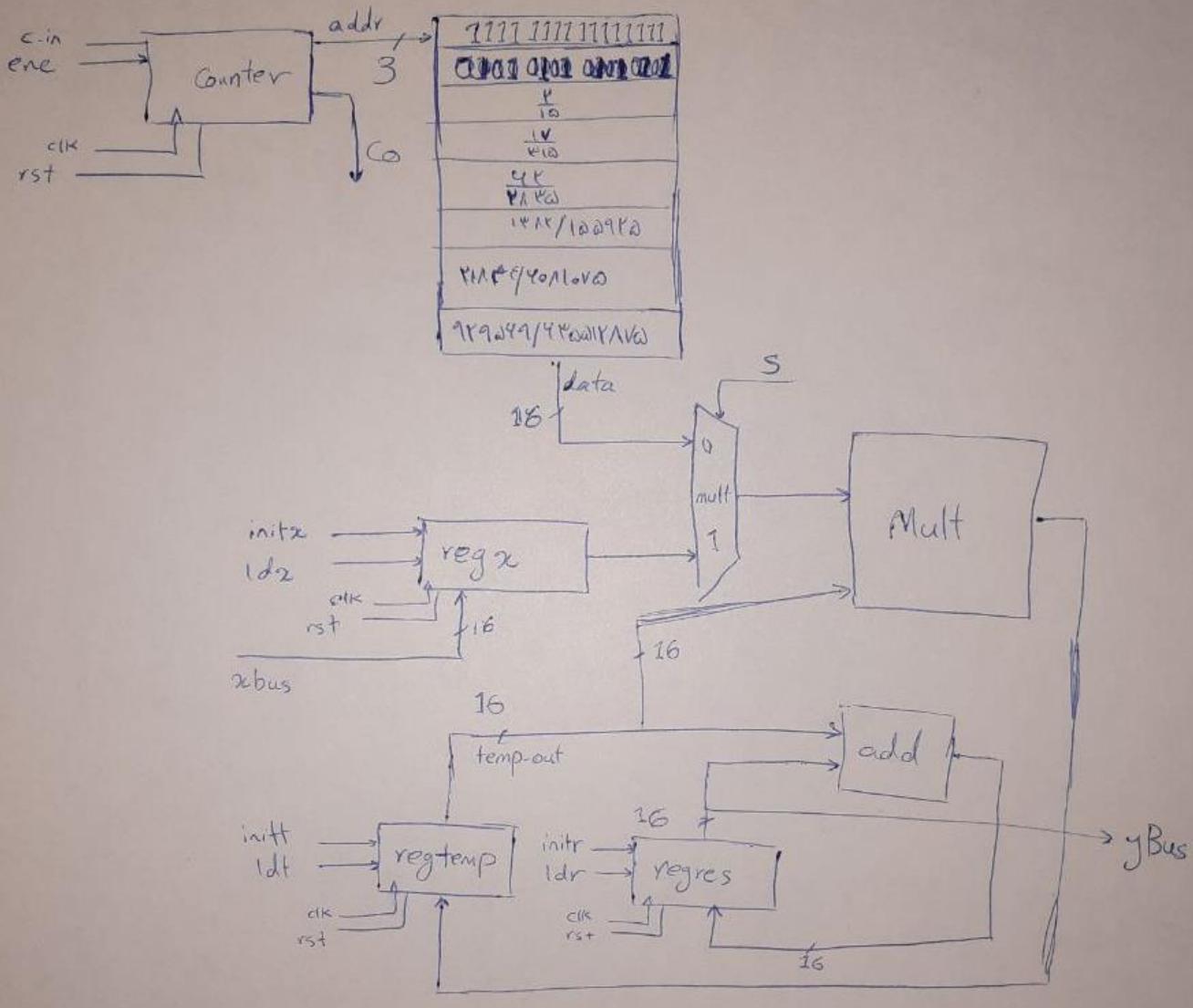


به نام خدا  
علی عطاءالله  
810199461





Controller:

`timescale 1ns/1ns

```
module controller (input clk,rst,start,co,output reg ready,initx,ldx,initt,lrd,enc,s,busy);
```

```
reg[2:0] ps,ns;
```

```
parameter [2:0] Idle=0,init=1,Begin=2,Mult1=3,Mult2=4,Mult3=5,add=6;
```

```
always @(ps,co,start)begin
```

```
    ns=Idle;
```

```
    case(ps)
```

```
        Idle:ns=(start)? init:Idle;
```

```
        init:ns=(start)? init:Begin;
```

```
        Begin:ns=Mult2;
```

```
        Mult1:ns=Mult2;
```

```
        Mult2:ns=Mult3;
```

```
        Mult3:ns=add;
```

```

    add:ns=(co)? Idle:Mult1;

    endcase

end

always@(posedge clk,posedge rst)begin

if(rst==1'b1)

    ps<=Idle;

else

    ps<=ns;

end

always @ (ps,co,start)begin

    ready=1'b0;initx=1'b0;idx=1'b0;initt=1'b0;lbt=1'b0;busy=1'b0;

    initr=1'b0;lbr=1'b0;enc=1'b0;s=1'b0;

    case(ps)

        Idle:begin ready=1'b1; end

        init:begin idx=1'b1; end

        Begin:begin initr=1'b1; initt=1'b1; end

        Mult1:begin s=1'b0; lbt=1'b1;busy=1'b1; end

        Mult2:begin s=1'b1; lbt=1'b1;busy=1'b1; end

        Mult3:begin s=1'b0; lbt=1'b1;busy=1'b1; end

        add:begin enc=1'b1; lbr=1'b1;busy=1'b1; end

    endcase

end

endmodule

```

TB:

```

`timescale 1ns/1ns

module tb ();
    logic ready,initx,Idx,initt,lbt,initr,lbr,lbt,enc,s;

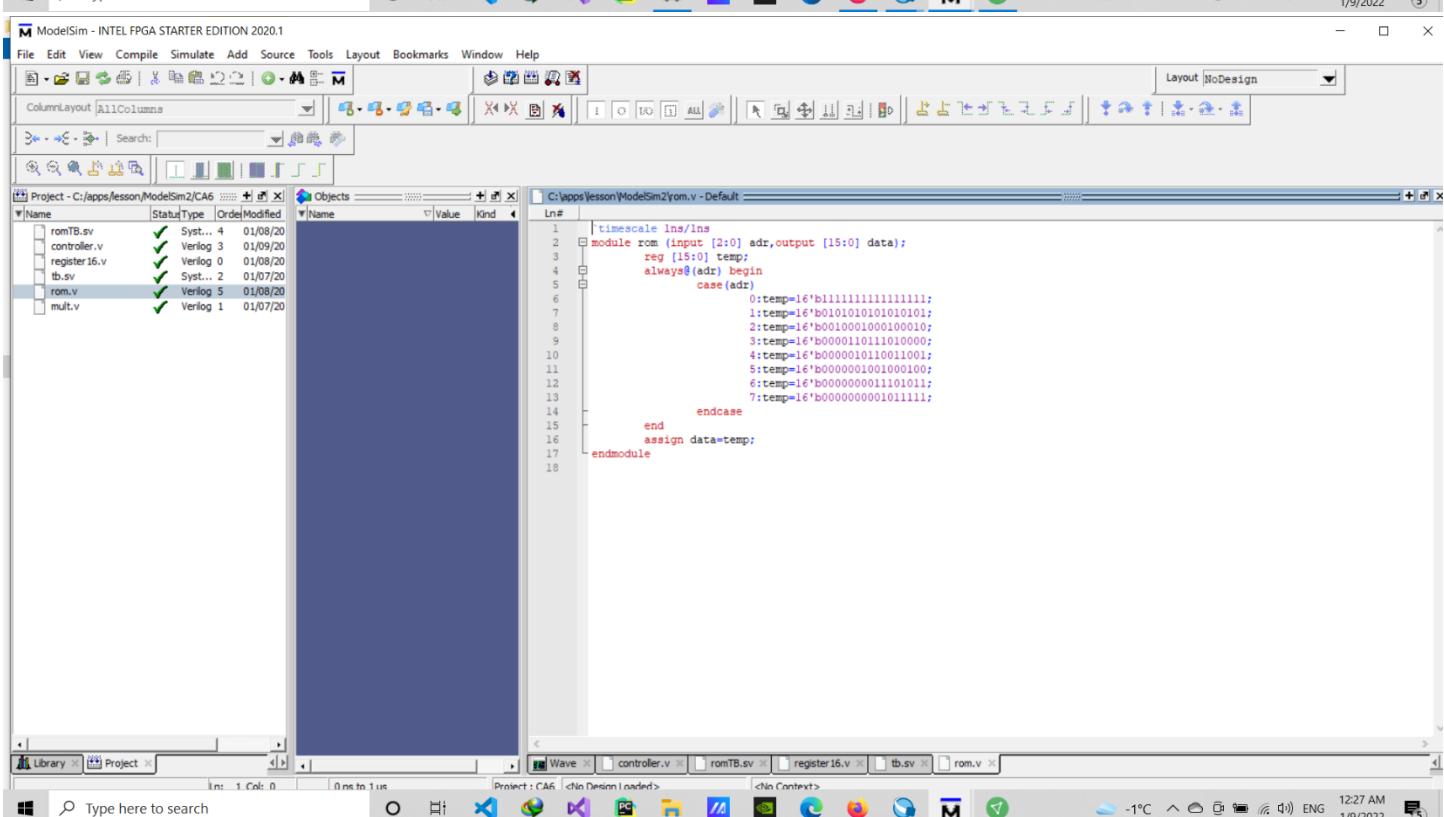
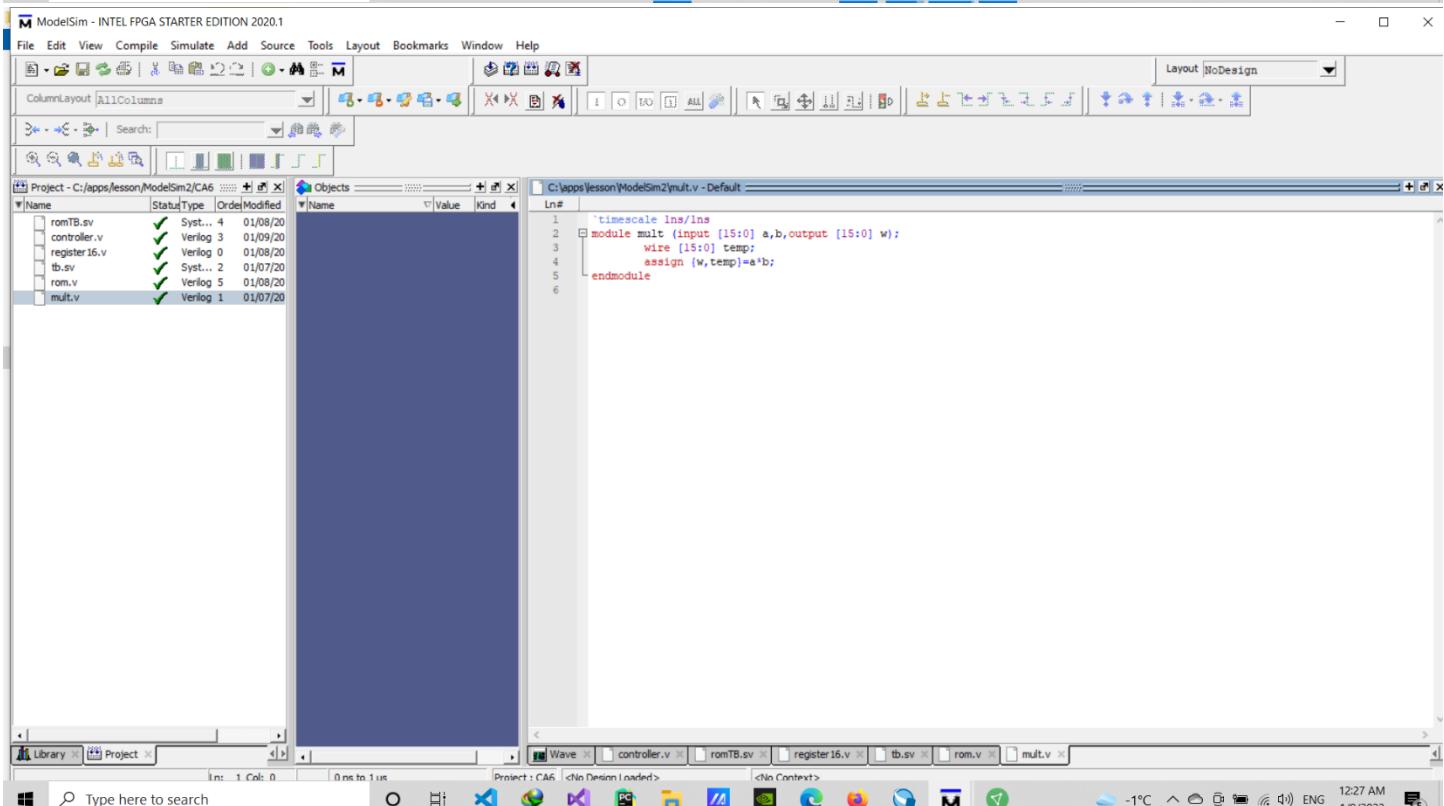
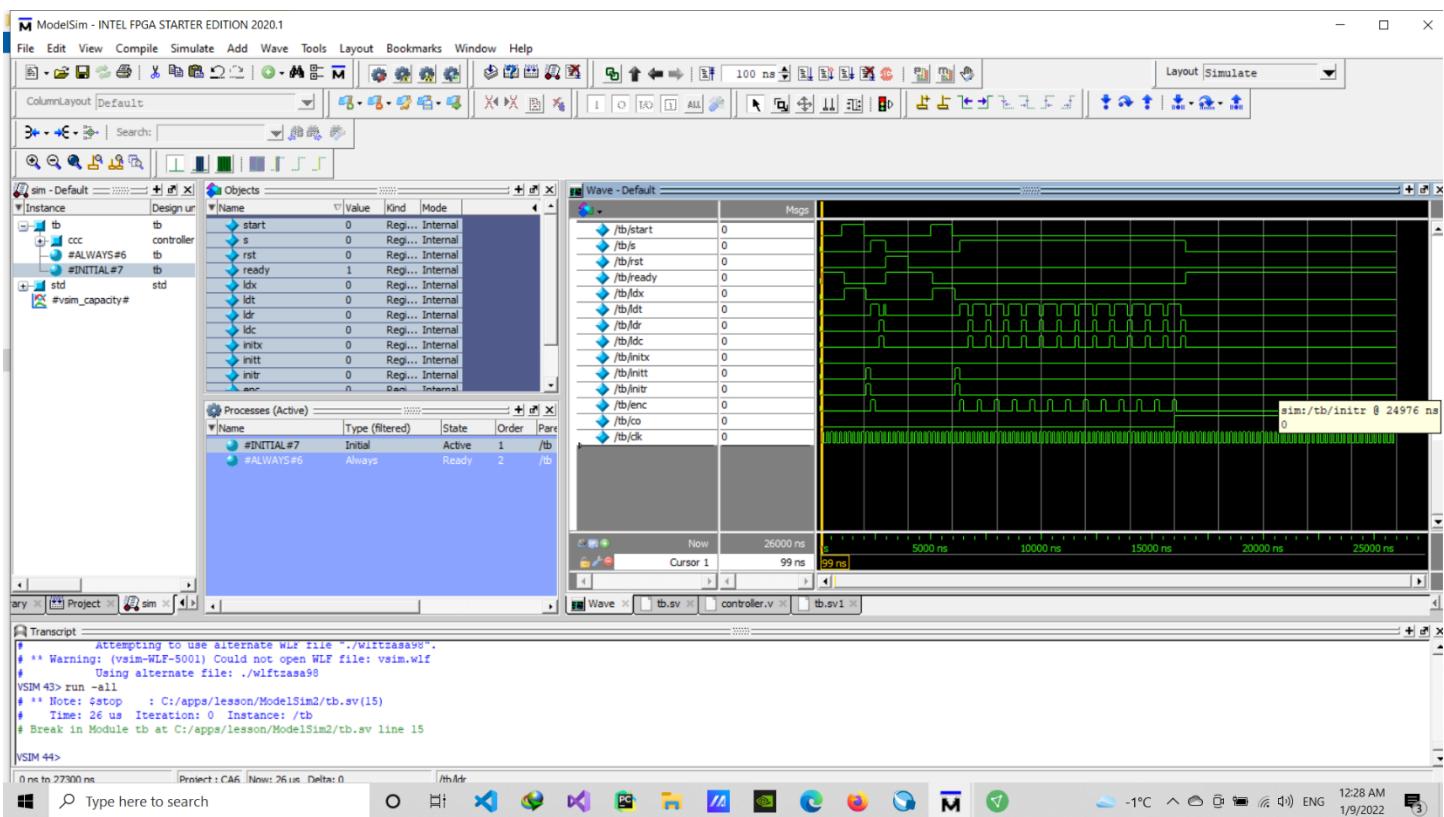
    logic clk=1'b0,rst=1'b0,start=1'b0,co=1'b0;

    controller ccc(clk,rst,start,co,ready,initx,Idx,initt,lbt,initr,lbr,lbt,enc,s);

    always #100 clk=~clk;

```

```
initial begin  
    #1000 start=1'b1;  
  
    #1000 start=1'b0;  
  
    #1000 rst=1'b1;  
  
    #1000 rst=1'b0;  
  
    #1000 start=1'b1;  
  
    #1000 start=1'b0;  
  
    #10000 co=1'b1;  
  
    #10000 $stop;  
  
end  
  
endmodule
```



ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

ColumnLayout [AllColumns] Objects Layout [NoDesign]

Project - C:/apps/lesson/ModelSim/CA6

Name Status Type Order Modified Name Value Kind

- romTB.v ✓ System 4 01/08/20
- controller.v ✓ Verilog 3 01/09/20
- register16.v ✓ Verilog 0 01/08/20
- tb.v ✓ System 2 01/07/20
- rom.v ✓ Verilog 5 01/08/20
- mult.v ✓ Verilog 1 01/07/20

C:\apps\lesson\ModelSim\tb.sv - Default

```
1 timescale 1ns/1ns
2 module tb ();
3   logic ready, initx, ldx, initr, ldr, ldc, enc, s;
4   logic clk=1'b0, rst=1'b0, start=1'b0, co=1'b0;
5   controller coc(clk, rst, start, co, ready, initx, ldx, initr, ldr, ldc, enc, s);
6   always #100 clk=~clk;
7   initial begin
8     $1000 start=1'b1;
9     $1000 start=1'b0;
10    $1000 rst=1'b1;
11    $1000 rst=1'b0;
12    $1000 start=1'b1;
13    $1000 start=1'b0;
14    $1000 co=1'b1;
15    $10000 $stop;
16  end
17 endmodule
18
```

Device is ready  
'USB Keyboard' is set up and ready to go.

Library Project Wave controller.v romTB.sv register16.v tb.sv

Type here to search

12:27 AM 1/9/2022

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

ColumnLayout [AllColumns] Objects Layout [NoDesign]

Project - C:/apps/lesson/ModelSim2/CA6

Name Status Type Order Modified Name Value Kind

- romTB.v ✓ System 4 01/08/20
- controller.v ✓ Verilog 3 01/09/20
- register16.v ✓ Verilog 0 01/08/20
- tb.sv ✓ System 2 01/07/20
- rom.v ✓ Verilog 5 01/08/20
- mult.v ✓ Verilog 1 01/07/20

C:\apps\lesson\ModelSim2\register16.v - Default

```
1 timescale 1ns/1ns
2 module register16 (input clk,rst,init,ld,input[15:0] ParIn,io,output reg[15:0] ParOut);
3   always @(posedge clk,posedge rst,posedge init)begin
4     if(rst)
5       ParOut<=16'b0;
6     else
7       if(init)
8         ParOut<= io;
9     else
10       ParOut<= (ld) ? ParIn : ParOut;
11   end
12 endmodule
13
```

Device is ready  
'USB Keyboard' is set up and ready to go.

Library Project Wave controller.v romTB.sv register16.v tb.sv

Type here to search

12:27 AM 1/9/2022

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

ColumnLayout [AllColumns] Search: Layout NoDesign

Project - C:/apps/lesson/ModelSim2/CA6 Objects

Name	Status	Type	Order	Modified
romTB.sv	✓	Syst...	4	01/08/20
controller.v	✓	Verilog	3	01/09/20
register16.v	✓	Verilog	0	01/08/20
tb.sv	✓	Syst...	2	01/07/20
rom.v	✓	Verilog	5	01/08/20
mult.v	✓	Verilog	1	01/07/20

C:/apps/lesson/ModelSim2/controller.v - Default

```

1 timescale 1ns/1ns
2 module controller (input clk,rst,start,co,output reg ready,initx,ldx,initt,ldt,initr,ldr,enc,s,busy);
3   reg[2:0] ps,ns;
4   parameter [2:0] Idle=0,init=1,Begin=2,Mult1=3,Mult2=4,Mult3=5,add=6;
5   always @(ps,co,start)begin
6     ns<idle;
7     case(ps)
8       Idle:ns=(start)? init:Idle;
9       init:ns=(start)? init:Begin;
10      Begin:ns=Mult2;
11      Mult1:ns=Mult3;
12      Mult2:ns=Mult3;
13      Mult3:ns=add;
14      add:ns=(co)? Idle:Mult1;
15    endcase
16  end
17  always@(posedge clk,posedge rst)begin
18    if(rst==1'b1)
19      ps<idle;
20    else
21      ps<ns;
22  end
23  always @(ps,co,start)begin
24    ready=1'b0;initx=1'b0;ldx=1'b0;initt=1'b0;ldt=1'b0;busy=1'b0;
25    initr=1'b0;ldr=1'b0;enc=1'b0;s=1'b0;
26    case(ps)
27      Idle:begin ready=1'b1; end
28      init:begin ldx=1'b1; end
29      Begin:begin initr=1'b1; initt=1'b1; end
30      Mult1:begin s=1'b0; ldt=1'b1;busy=1'b1; end
31      Mult2:begin s=1'b1; ldt=1'b1;busy=1'b1; end
32      Mult3:begin s=1'b0; ldt=1'b1;busy=1'b1; end
33      add:begin enc=1'b1; ldr=1'b1;busy=1'b1; end
34    endcase
35  end
36 endmodule

```

Wave controller.v romTB.sv

Library Project

1 Col: 0 0 ms to 1 us Project : CAR <In Design | loaded> <In Context>

-1°C ENG 12:27 AM 1/9/2022

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

ColumnLayout [AllColumns] Search: Layout NoDesign

Project - C:/apps/lesson/ModelSim2/CA6 Objects

Name	Status	Type	Order	Modified
romTB.sv	✓	Syst...	4	01/08/20
controller.v	✓	Verilog	3	01/09/20
register16.v	✓	Verilog	0	01/08/20
tb.sv	✓	Syst...	2	01/07/20
rom.v	✓	Verilog	5	01/08/20
mult.v	✓	Verilog	1	01/07/20

C:/apps/lesson/ModelSim2/romTB.sv - Default

```

1 timescale 1ns/1ns
2 module romTB ();
3   logic add=3'b001;
4   wire[15:0] q;
5   logic clk=1'b0;
6   myRom mr (add,clk,q);
7   initial begin
8     $1000 add=3'b011;
9     $10000 $stop;
10  end
11 endmodule

```

Wave controller.v romTB.sv

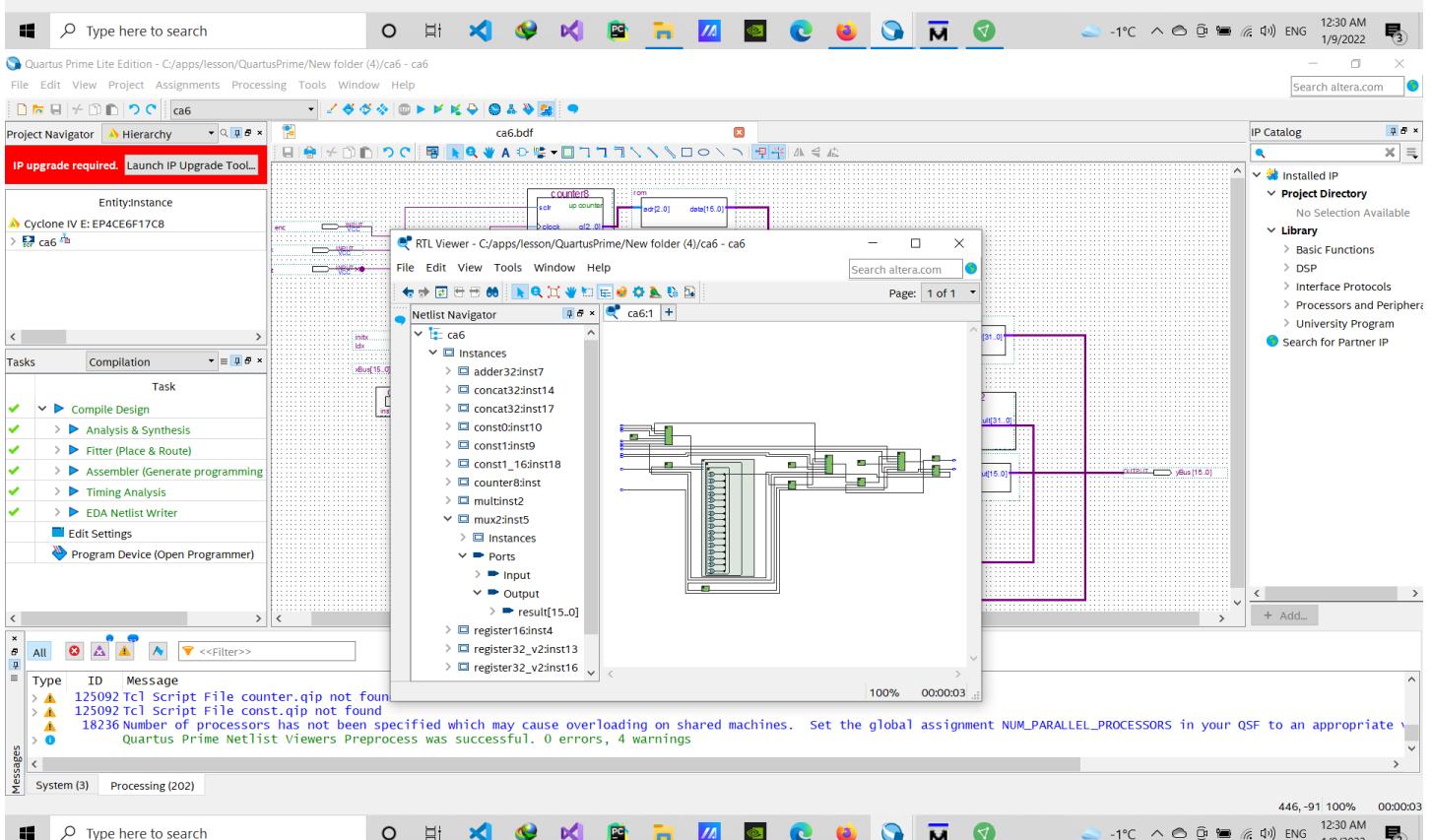
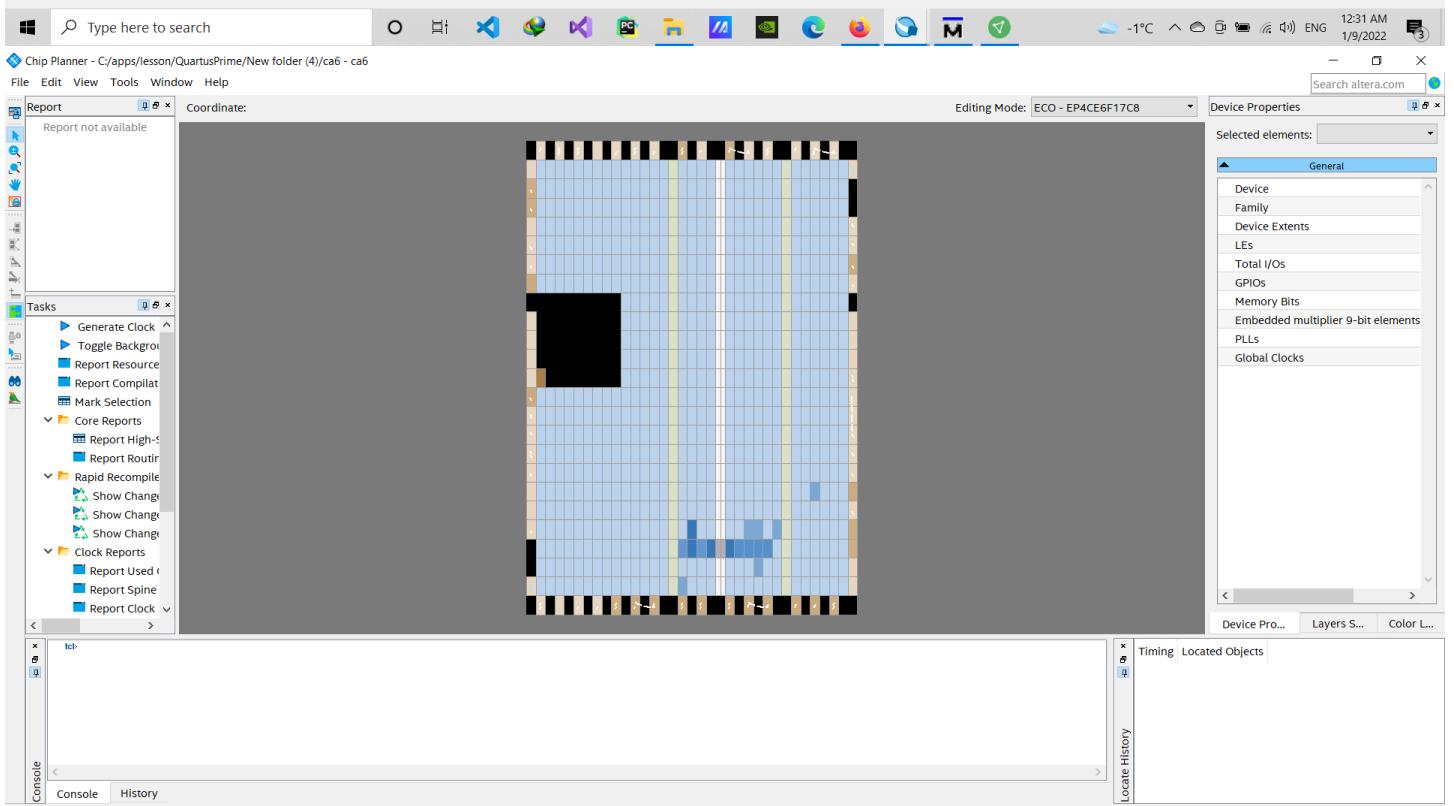
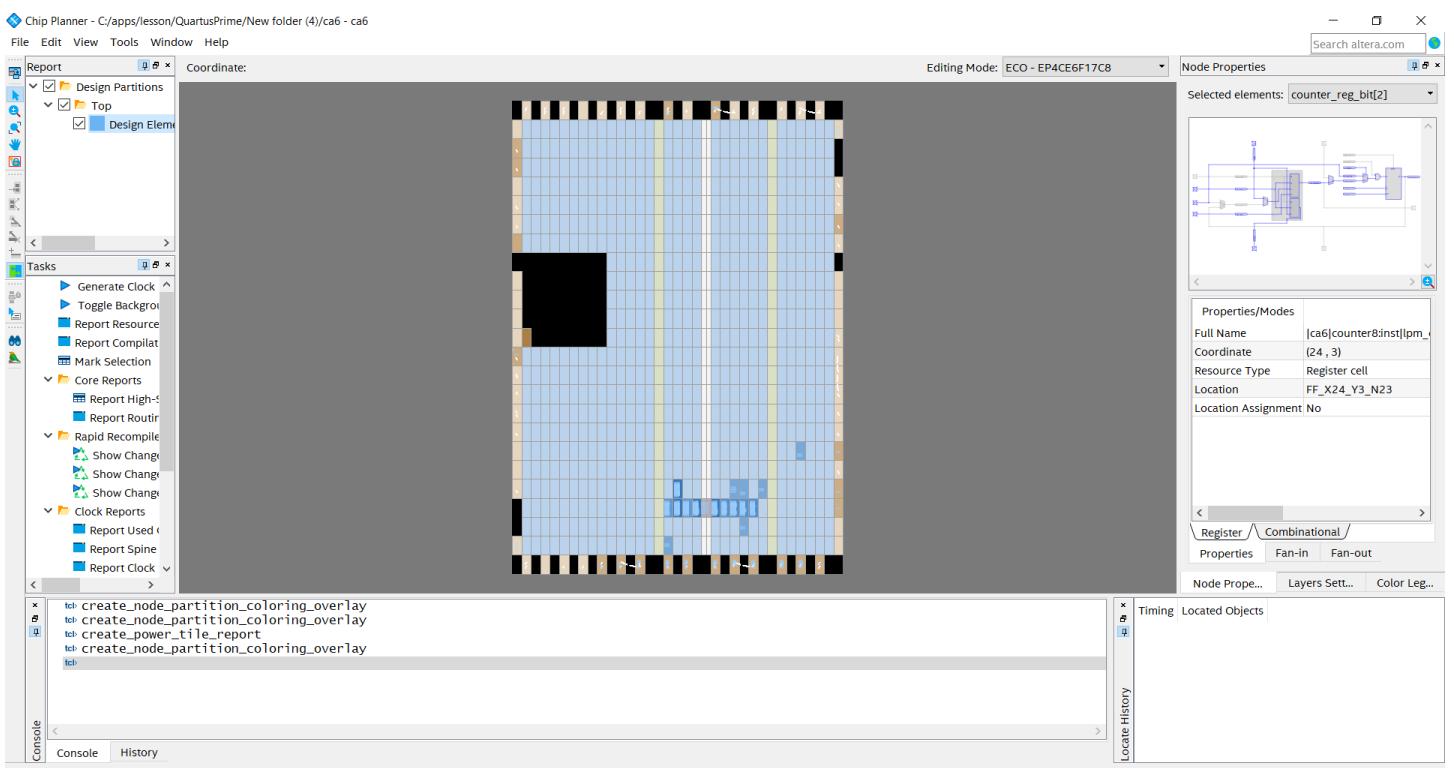
Library Project

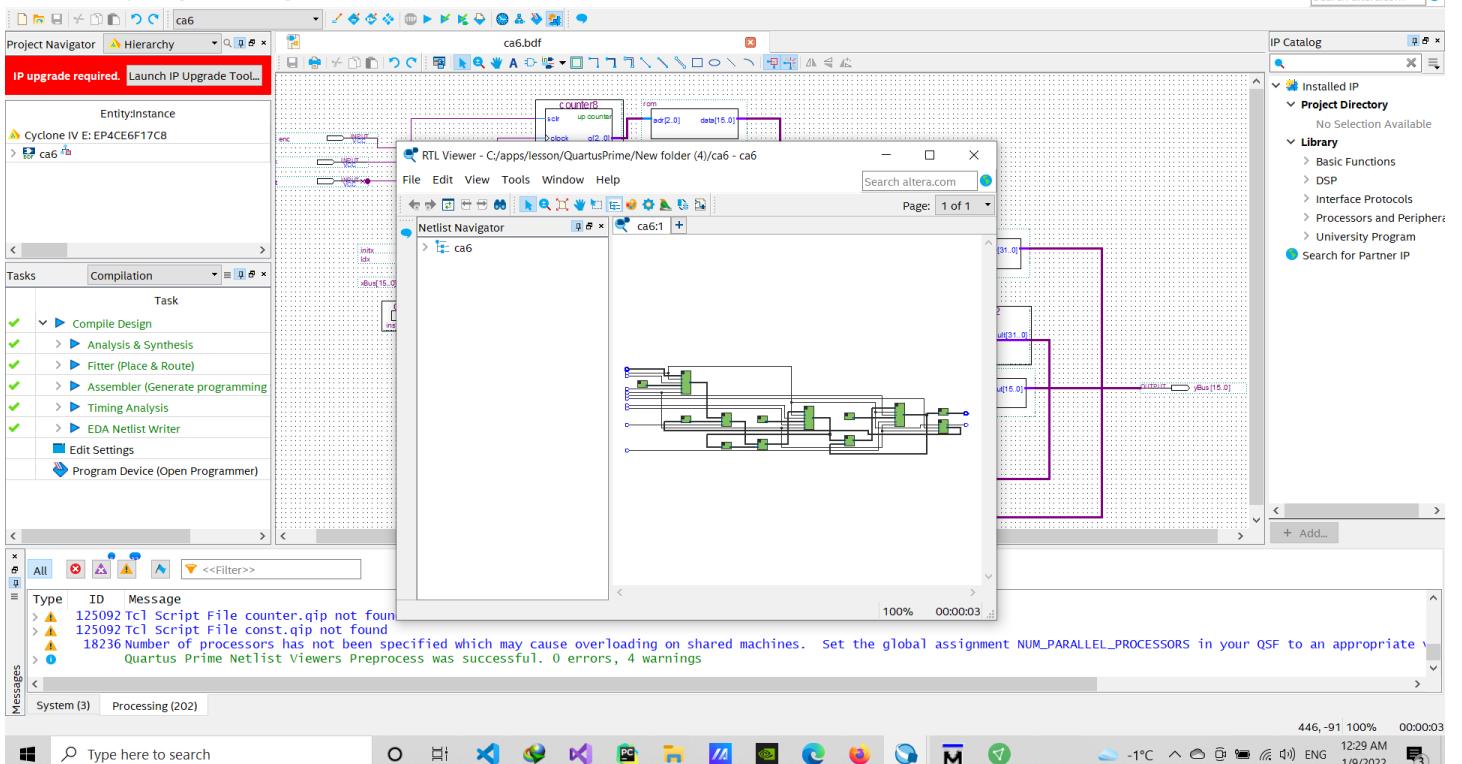
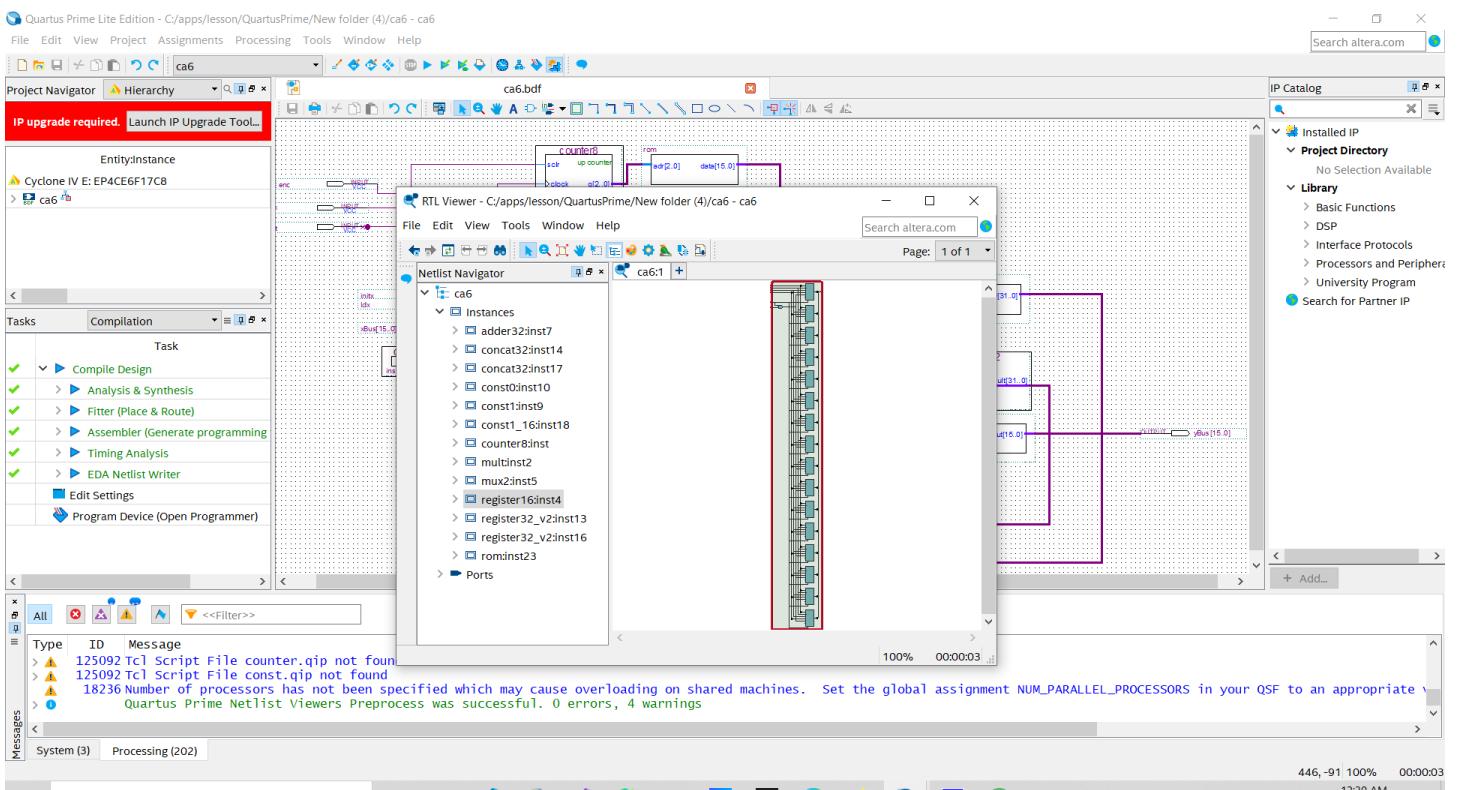
1 Col: 0 0 ms to 1 us Project : CAR <In Design | loaded> <In Context>

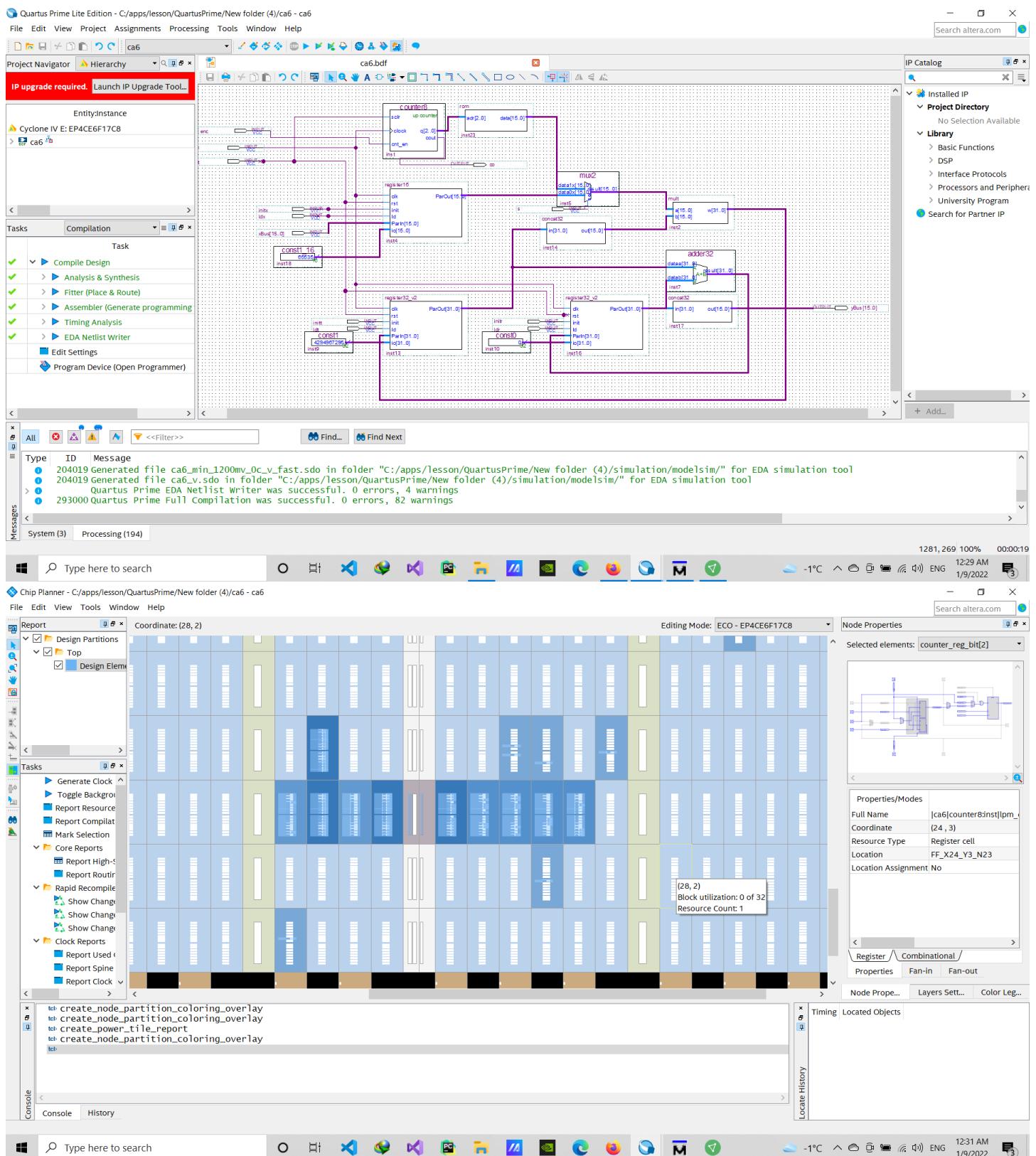
Setting up a device  
We're setting up 'USB Keyboard'.

-1°C ENG 12:27 AM 1/9/2022

Datapath:







Full:

Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (5)/ca6\_final - ca6\_final

File Edit View Project Assignments Processing Tools Window Help

ca6\_final

Project Navigator Hierarchy

EntityInstance Cyclone IV E:EP4CE6E22C8 > ca6\_final

Tasks Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

ca6\_final.bdf

```

1 timescale 1ns/1ns
2 module controller (input clk,rst,start,co, output reg ready,initx,ldx,initt,lrd,initr,ldr,enc,s,busy);
3 parameter [2:0] Idle=0,init=1,Begin=2,Mult1=3,Mult2=4,Mult3=5,add=6;
4
5 always @(ps,co,start)begin
6   ps=Idle;
7   case(ps)
8     Idle:ns=(start)? init:Idle;
9     init:ns=(start)? init:Begin;
10    Begin:ns=Mult2;
11    Mult1:ns=Mult2;
12    Mult2:ns=Mult3;
13    Mult3:ns=add;
14    add:ns=(co)? Idle:Mult1;
15   endcase
16 end
17 always@(posedge clk,posedge rst)begin
18   if(rst==1'b1)
19     ps<=Idle;
20   else
21     ps<=ns;
22 end
23 always @(ps,co,start)begin
24   ready=1'b0;initx=1'b0;ldx=1'b0;initt=1'b0;busy=1'b0;
25   initr=1'b0;lrd=1'b0;enc=1'b0;s=1'b0;
26   case(ps)
27     Idle:begin ready=1'b1; end
28     init:begin initr=1'b1; initt=1'b1; end
29     Begin:begin initx=1'b1; ldx=1'b1; busy=1'b1; end
30     Mult1:begin s=1'b0; ldt=1'b1; busy=1'b1; end
31     Mult2:begin s=1'b1; ldt=1'b1; busy=1'b1; end
32     Mult3:begin s=1'b0; ldt=1'b1; busy=1'b1; end
33     add:begin enc=1'b1; ldr=1'b1; busy=1'b1; end
34   endcase
35 end
36 endmodule

```

IP Catalog

- Installed IP
- Project Directory
- No Selection Available
- Library

  - Basic Functions
  - DSP
  - Interface Protocols
  - Processors and Peripherals
  - University Program

Search for Partner IP

All Find... Find Next

Type ID Message

- 204019 Generated file ca6\_final\_min\_1200mv\_0c\_v.fast.sdo in folder "C:/apps/lesson/QuartusPrime/New folder (5)/simulation/modelsim/" for EDA simulation tool
- 204019 Generated file ca6\_final\_v.sdo in folder "C:/apps/lesson/QuartusPrime/New folder (5)/simulation/modelsim/" for EDA simulation tool
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 61 warnings

Messages System Processing (177)

