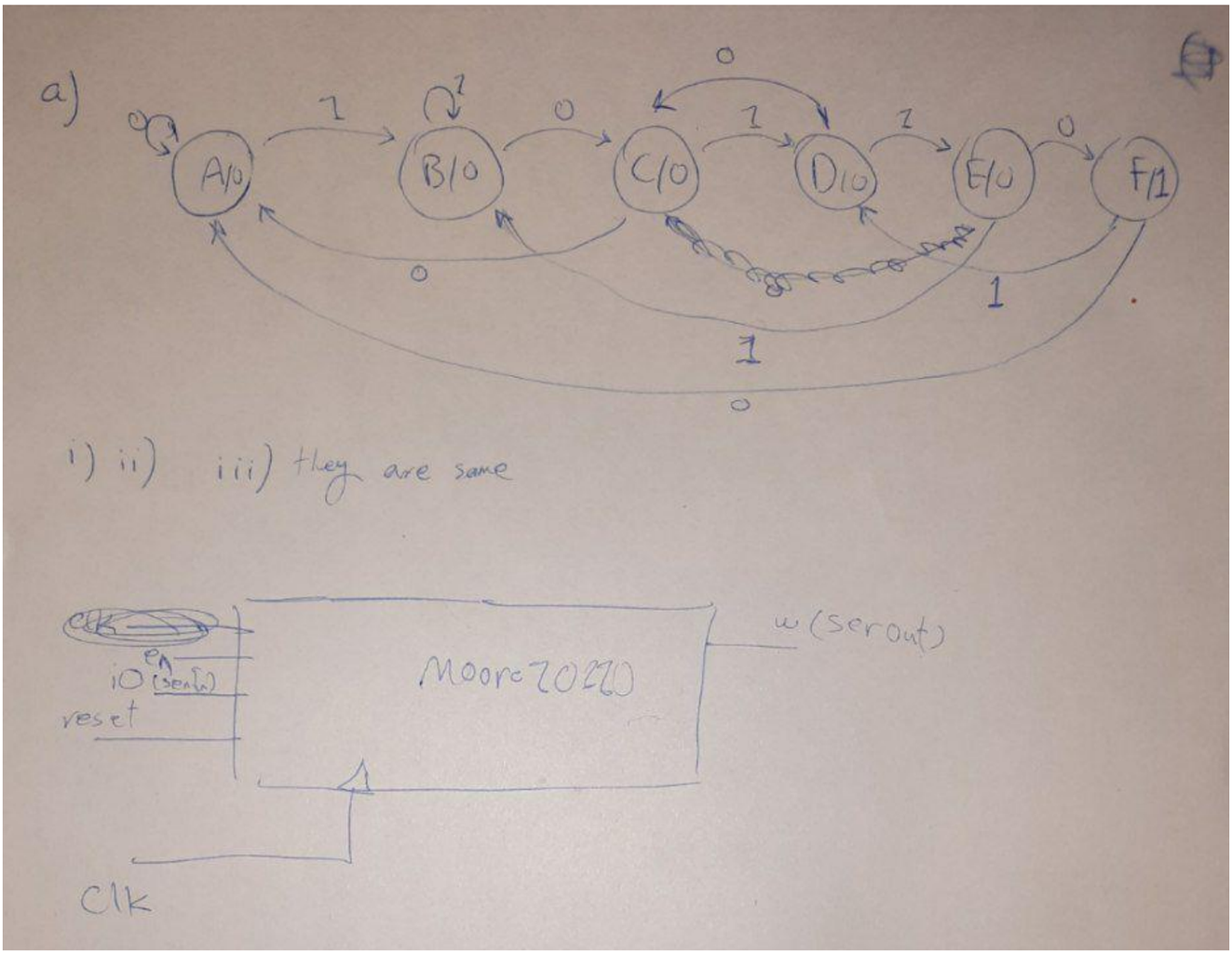
به نام خد ا

علی عطاللهی

810199461

1:

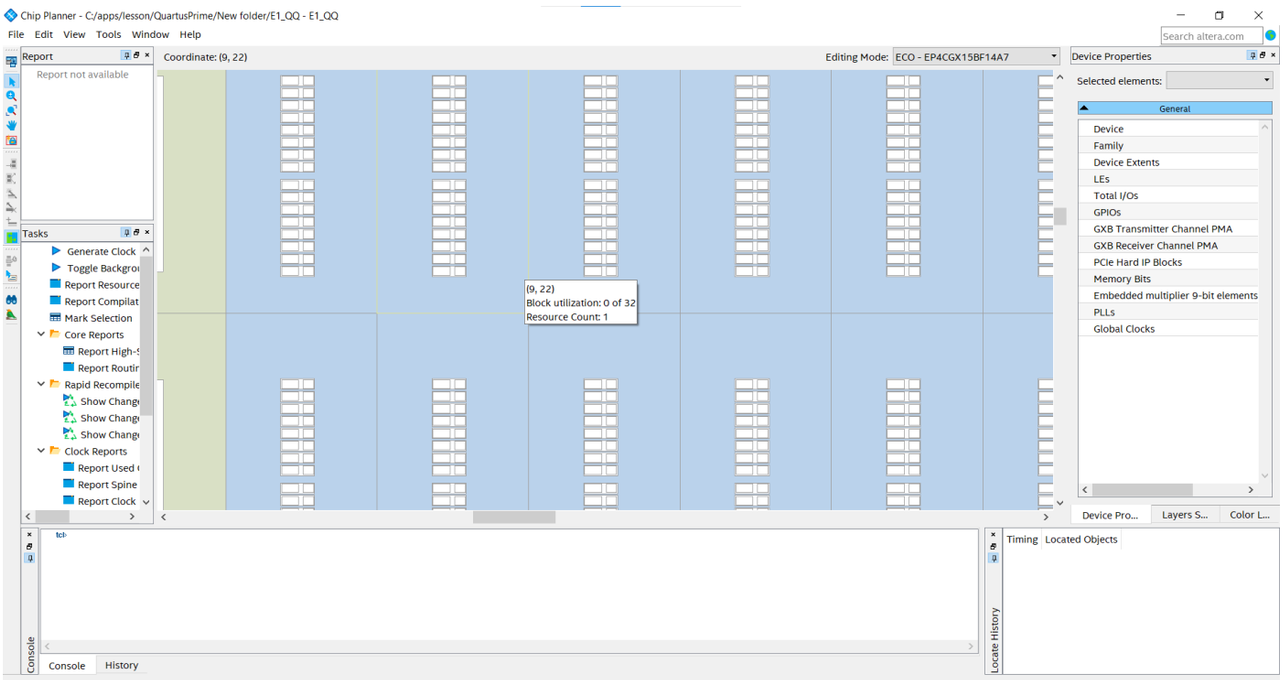


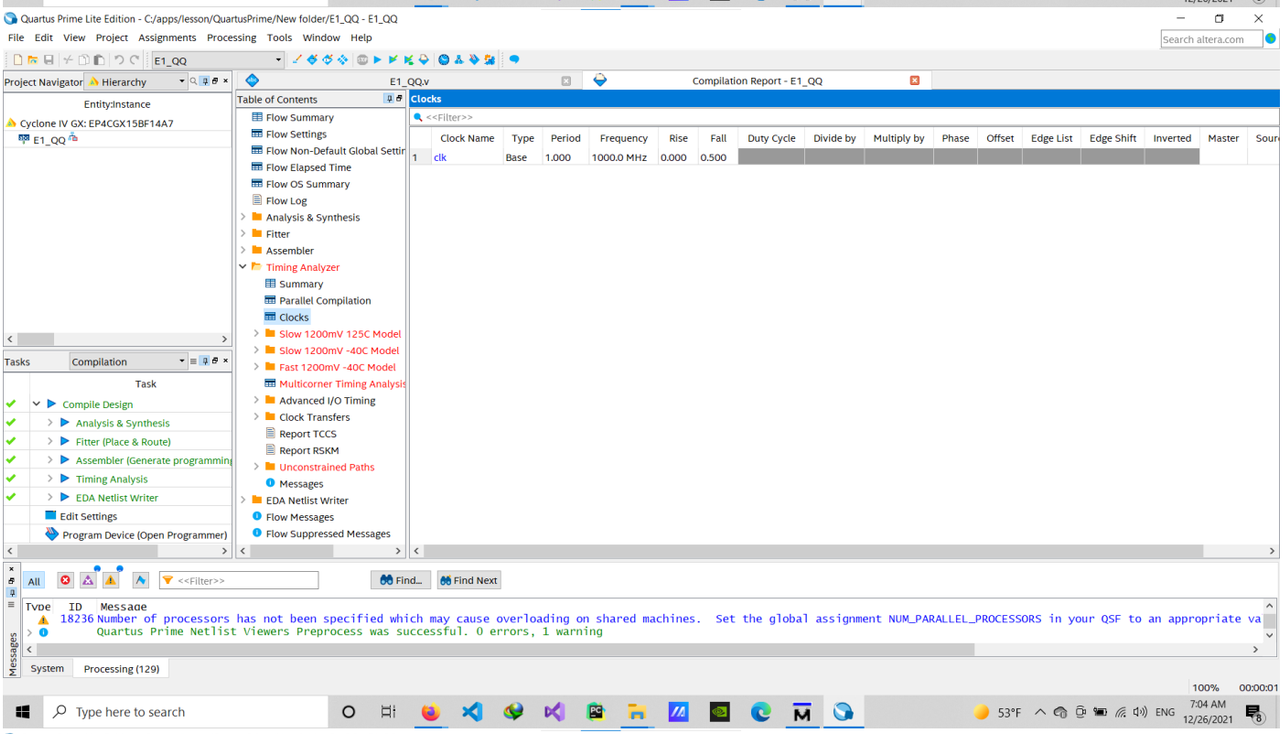
Code:

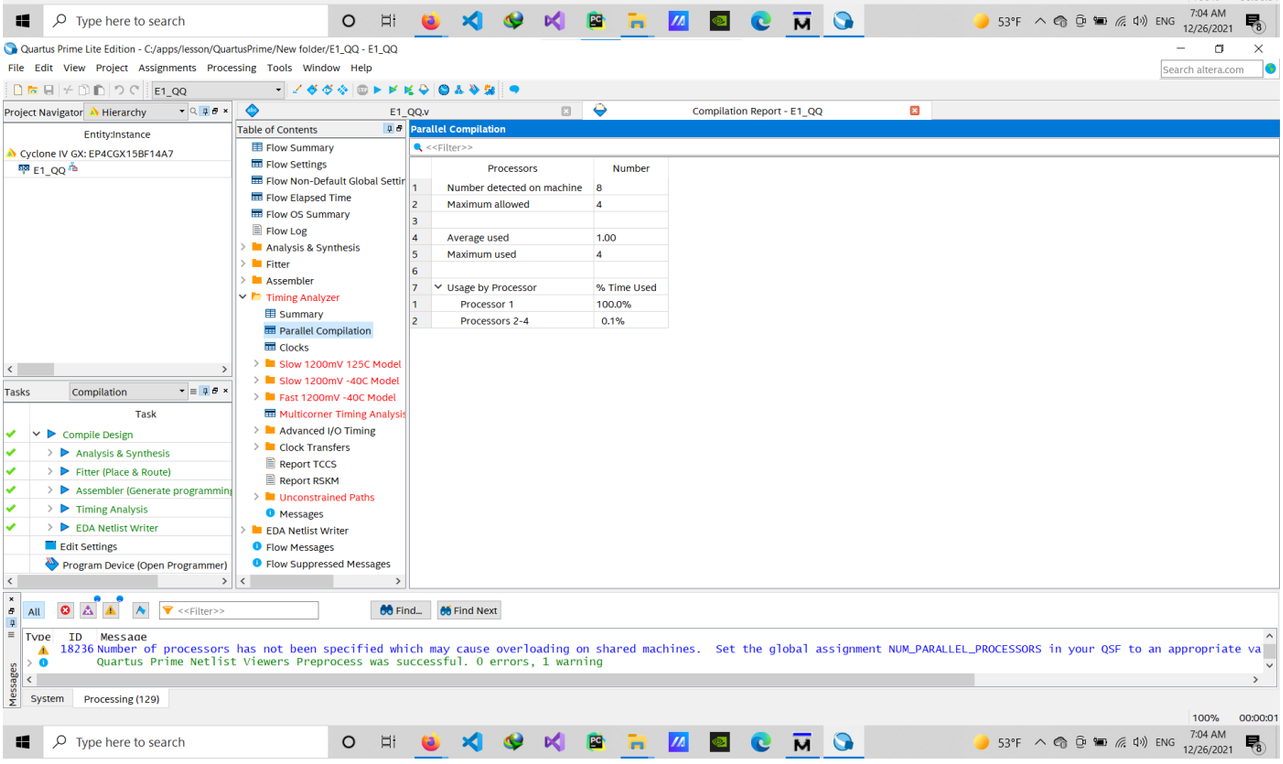
```
`timescale 1ns/1ns
module MOORE10110 (input clk,rst,j,output w);
    logic [2:0] ns,ps;
    parameter [2:0] A=3'b000,B=3'b001,C=3'b010,D=3'b011,E=3'b100,F=3'b101;
    always@(ps,j) begin
        ns=3'b000;
        case(ps)
            A: ns= j ? B : A;
            B: ns= j ? B : C;
            C: ns= j ? D : A;
            D: ns= j ? E : C;
            E: ns= j ? B : F;
            F: ns= j ? D : A;
            default: ns=A;
        endcase
    end
    assign w= (ps==F) ? 1'b1 : 1'b0;
    always@(posedge clk,posedge rst)begin
        if(rst)
            ps<=A;
        else
            ps<=ns;
    end
endmodule
```

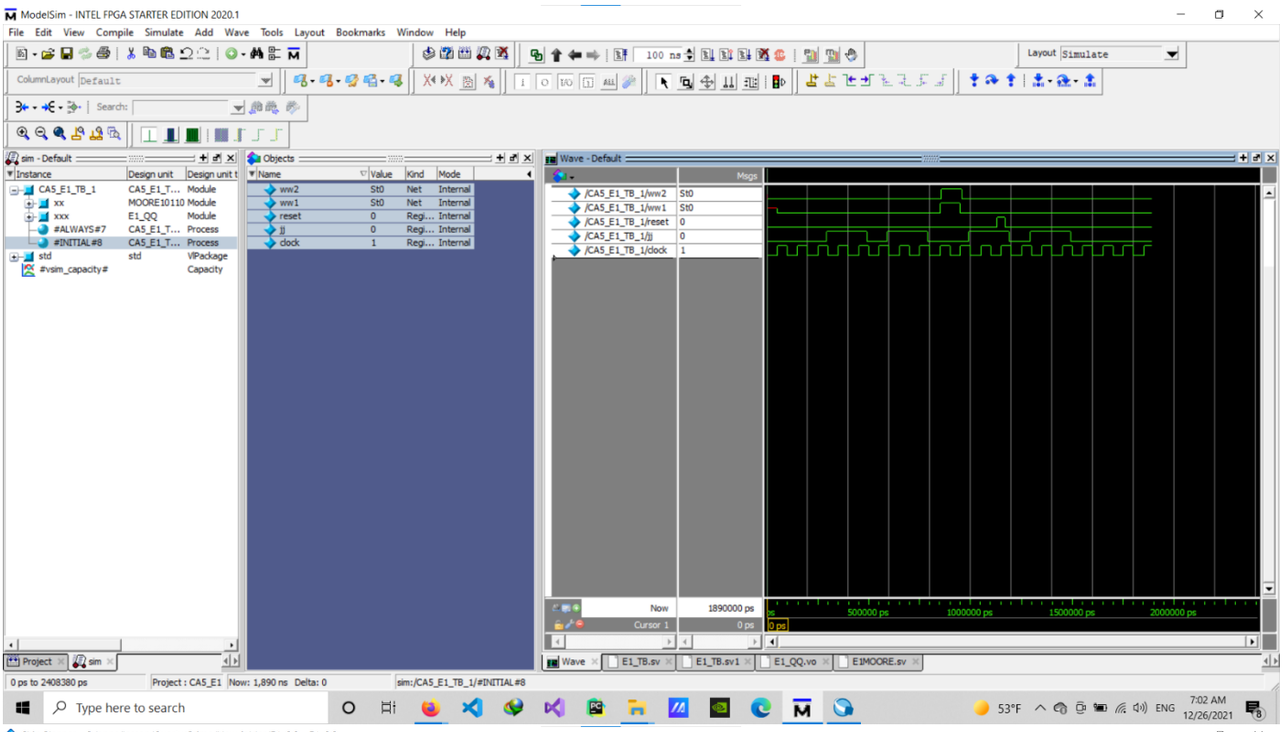
Tb:

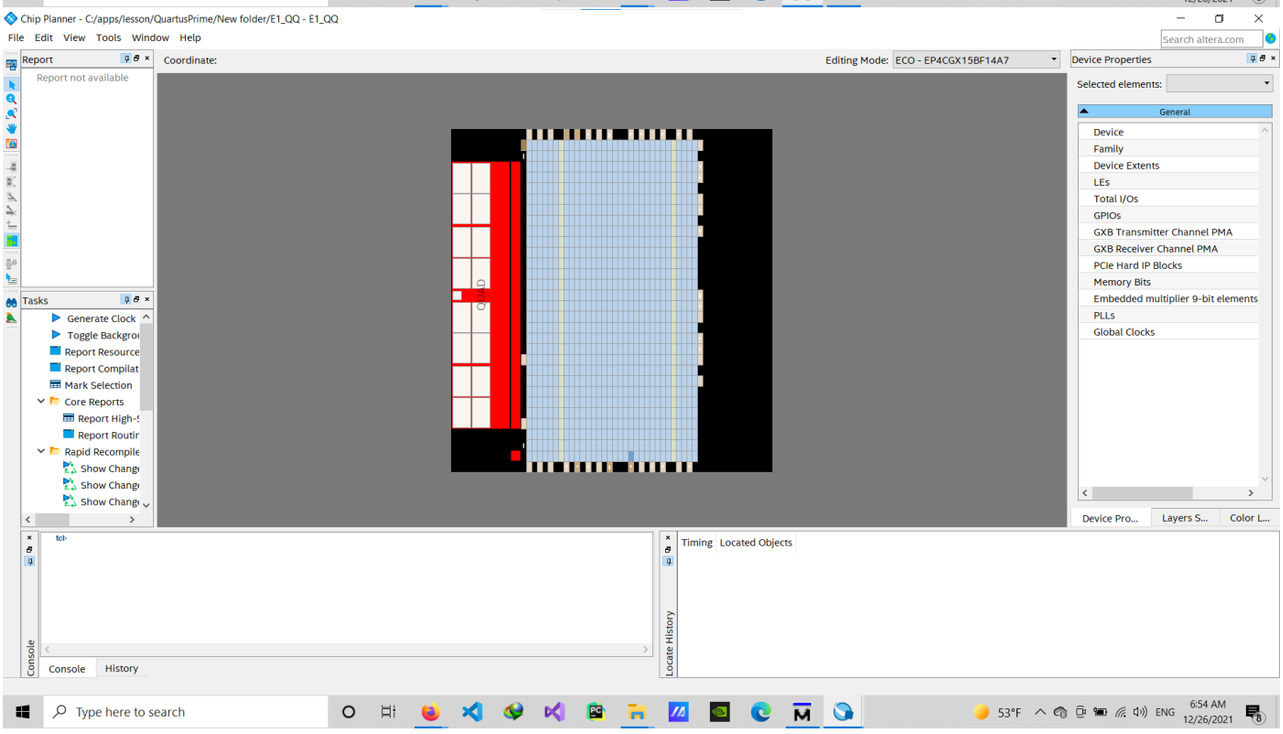
```
`timescale 1ns/1ns
module CA5_E1_TB_1 ();
    logic clock=0,jj=0,reset=0;
    wire ww1,ww2;
    MOORE10110 xx(clock,reset,jj,ww1);
    E1_QQ xxx(clock,reset,jj,ww2);
    always #50 clock=~clock ;
    initial begin
        #90 jj=0;
        #100 jj=0;
        #100 jj=1;
        #100 jj=1;
        #100 jj=0;
        #100 jj=1;
        #100 jj=1;
        #100 jj=0;
        #100 jj=0;
        #100 jj=1;
        #100 jj=1;
        #40 reset=1;
        #40 reset=0;
        #20 jj=0;
        #100 jj=1;
        #100 jj=1;
        #100 jj=0;
        #100 jj=0;
        #100 jj=0;
        #200 $stop;
    end
endmodule
```

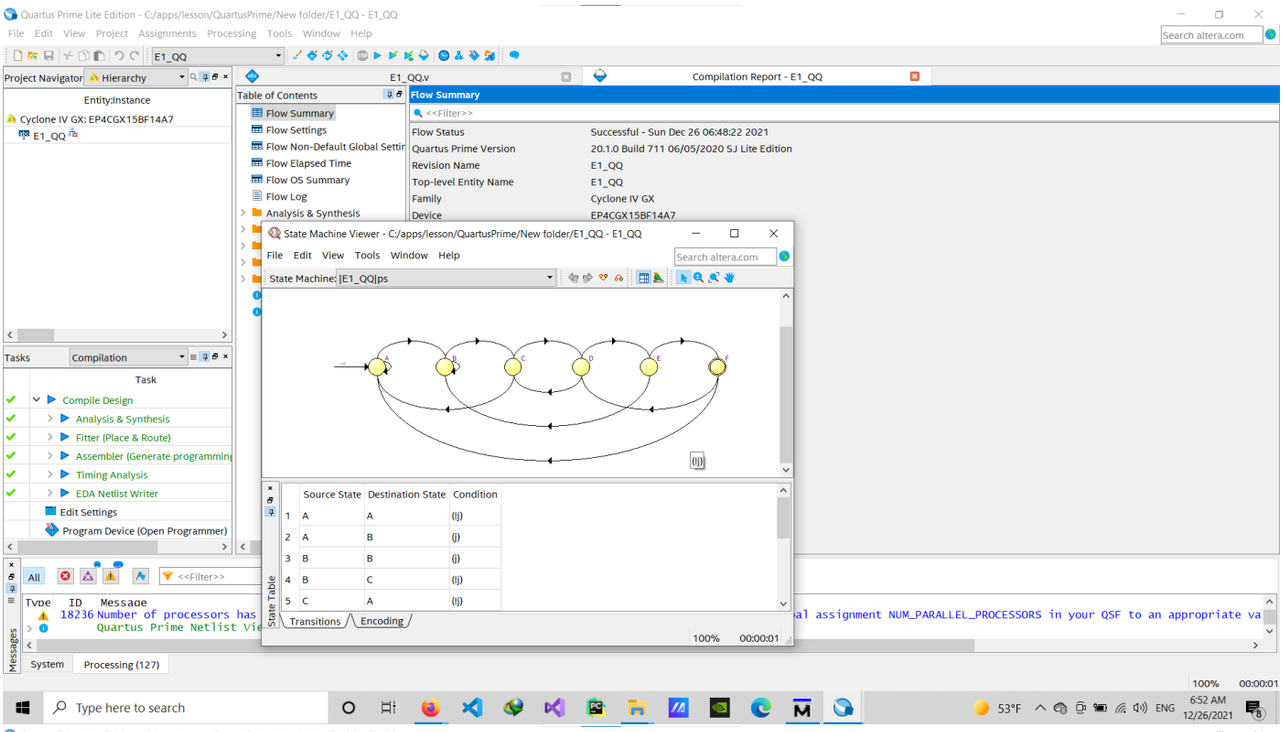

Chip Planner - C:/apps/lesson/QuartusPrime/New folder/E1_QQ - E1_QQ
File Edit View Tools Window Help
Search altera.com
Report
Report not available
Coordinate: (9, 22)
Editing Mode: ECO - EP4CGX15BF14A7
Device Properties
Selected elements:
General
Device
Family
Device Extents
LEs
Total I/Os
GPIOs
GXB Transmitter Channel PMA
GXB Receiver Channel PMA
PCIe Hard IP Blocks
Memory Bits
Embedded multiplier 9-bit elements
PLLs
Global Clocks
Tasks
Generate Clock
Toggle Backgrou
Report Resource
Report Compilat
Mark Selection
Core Reports
Report High-S
Report Routin
Rapid Recompile
Show Change
Show Change
Show Change
Clock Reports
Report Used
Report Spine
Report Clock
(9, 22)
Block utilization: 0 of 32
Resource Count: 1
Device Pro...
Layers S...
Color L...
Timing
Located Objects
Console
History
Locate History
Type here to search
53°F
ENG
7:06 AM
12/26/2021

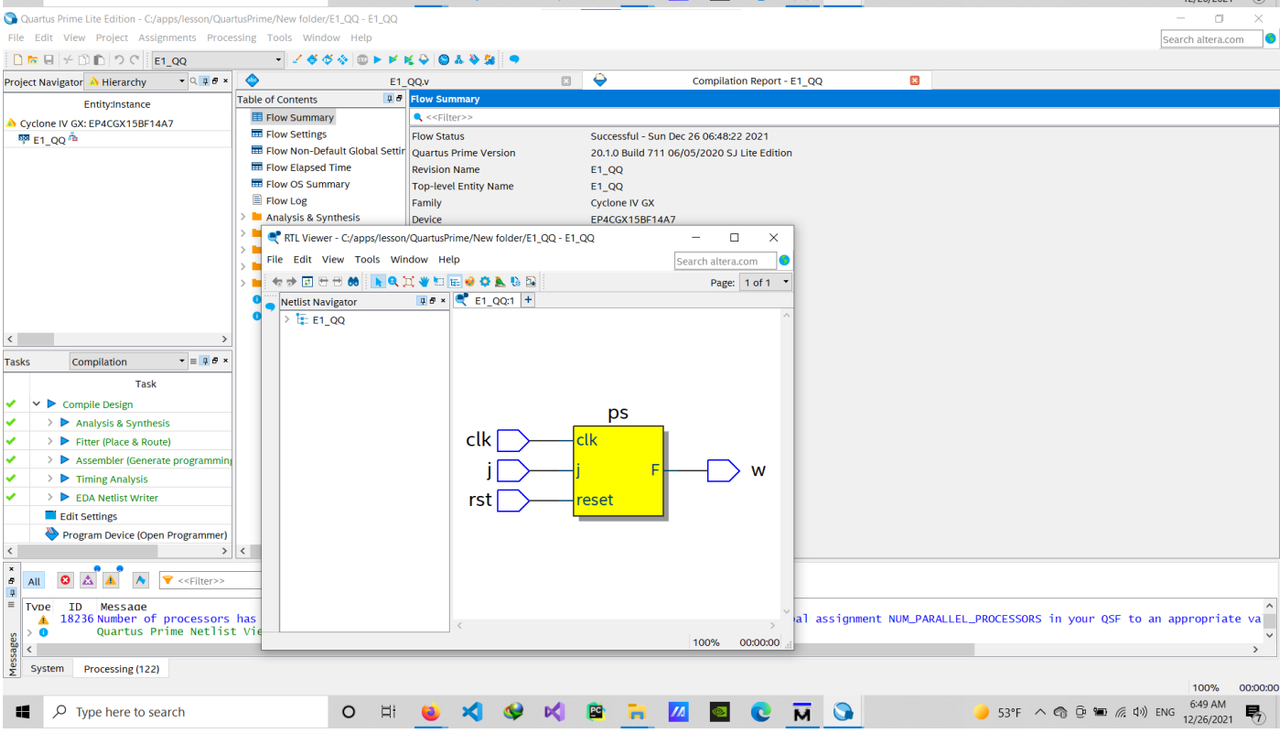

Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder/E1_QQ - E1_QQ
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
E1_QQ
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV GX: EP4CGX15BF14A7
E1_QQ
E1_QQ.v
Compilation Report - E1_QQ
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settir
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
Summary
Parallel Compilation
Clocks
Slow 1200mV 125C Model
Slow 1200mV -40C Model
Fast 1200mV -40C Model
Multicorner Timing Analysis
Advanced I/O Timing
Clock Transfers
Report TCCS
Report RSKM
Unconstrained Paths
Messages
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Clocks
<<Filter>>
Clock Name | Type | Period | Frequency | Rise | Fall | Duty Cycle | Divide by | Multiply by | Phase | Offset | Edge List | Edge Shift | Inverted | Master
1 clk | Base | 1.000 | 1000.0 MHz | 0.000 | 0.500
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
All
<<Filter>>
Find...
Find Next
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate va
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
Messages
System
Processing (129)
100%
00:00:01
Type here to search
53°F
ENG
7:04 AM
12/26/2021


Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder/E1_QQ - E1_QQ
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
E1_QQ
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV GX: EP4CGX15BF14A7
E1_QQ
E1_QQ.v
Compilation Report - E1_QQ
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settir
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
Summary
Parallel Compilation
Clocks
Slow 1200mV 125C Model
Slow 1200mV -40C Model
Fast 1200mV -40C Model
Multicorner Timing Analysis
Advanced I/O Timing
Clock Transfers
Report TCCS
Report RSKM
Unconstrained Paths
Messages
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Parallel Compilation
<<Filter>>
Processors | Number
1 Number detected on machine | 8
2 Maximum allowed | 4
3
4 Average used | 1.00
5 Maximum used | 4
6
7 Usage by Processor | % Time Used
1 Processor 1 | 100.0%
2 Processors 2-4 | 0.1%
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
All
<<Filter>>
Find...
Find Next
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate va
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
Messages
System
Processing (129)
100%
00:00:01
Type here to search
53°F
ENG
7:04 AM
12/26/2021

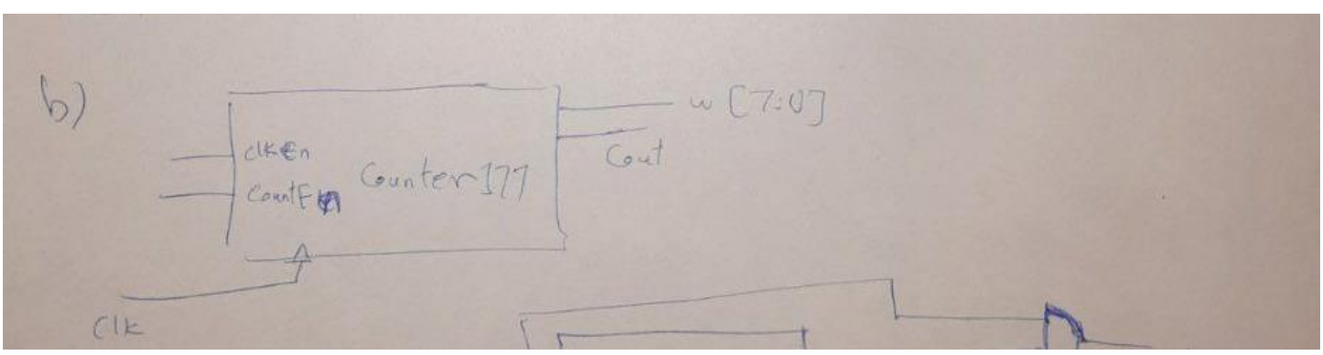

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
/CA5_E1_TB_1/ww2
/CA5_E1_TB_1/ww1
/CA5_E1_TB_1/reset
/CA5_E1_TB_1/jj
/CA5_E1_TB_1/clock
Now
Cursor 1
Wave
E1_TB.sv
E1_TB.sv1
E1_QQ.vo
E1MOORE.sv
Type here to search
7:02 AM
12/26/2021


Chip Planner - C:/apps/lesson/QuartusPrime/New folder/E1_QQ - E1_QQ
File Edit View Tools Window Help
Report
Report not available
Coordinate:
Editing Mode: ECO - EP4CGX15BF14A7
Device Properties
Selected elements:
General
Device
Family
Device Extents
LEs
Total I/Os
GPIOs
GXB Transmitter Channel PMA
GXB Receiver Channel PMA
PCIe Hard IP Blocks
Memory Bits
Embedded multiplier 9-bit elements
PLLs
Global Clocks
Tasks
Generate Clock
Toggle Backgro
Report Resource
Report Compilat
Mark Selection
Core Reports
Report High-
Report Routir
Rapid Recompile
Show Change
Show Change
Show Change
Console
History
Timing
Located Objects
Locate History
Type here to search
6:54 AM
12/26/2021





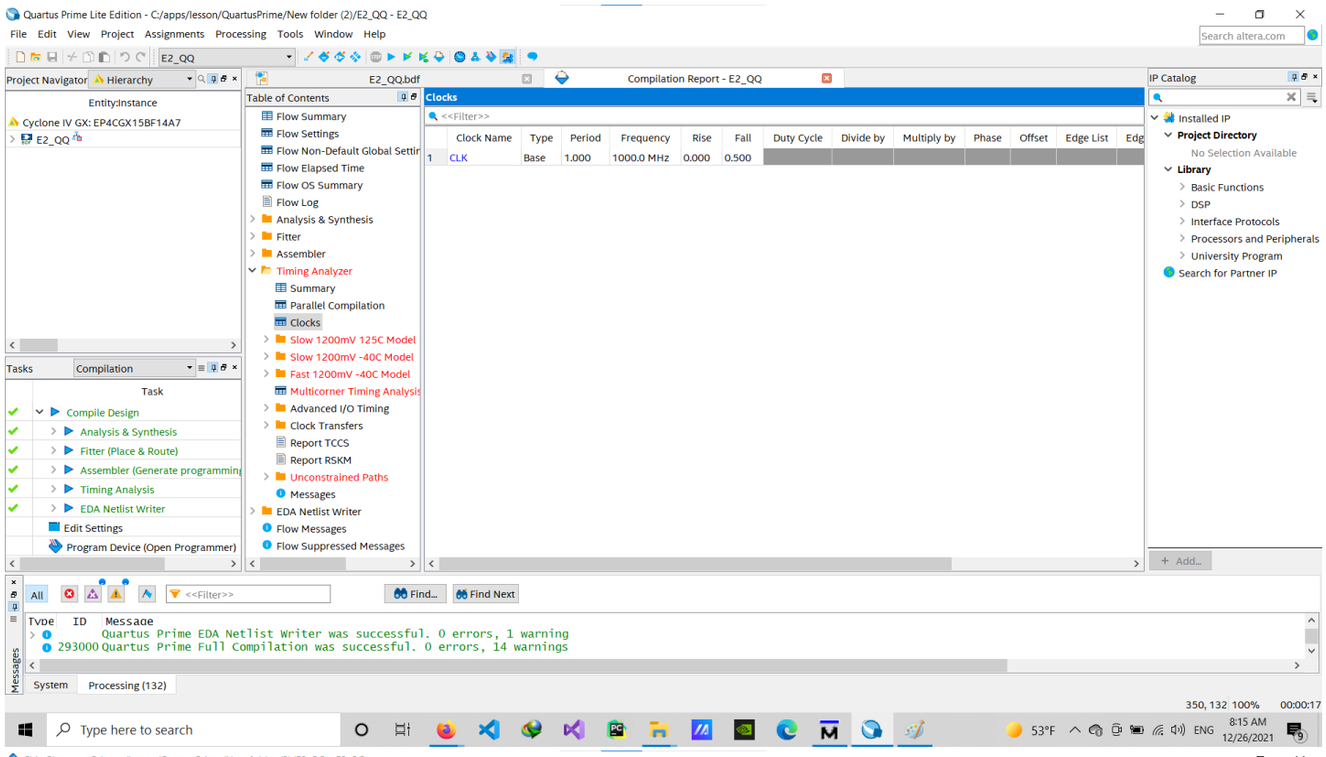
2:

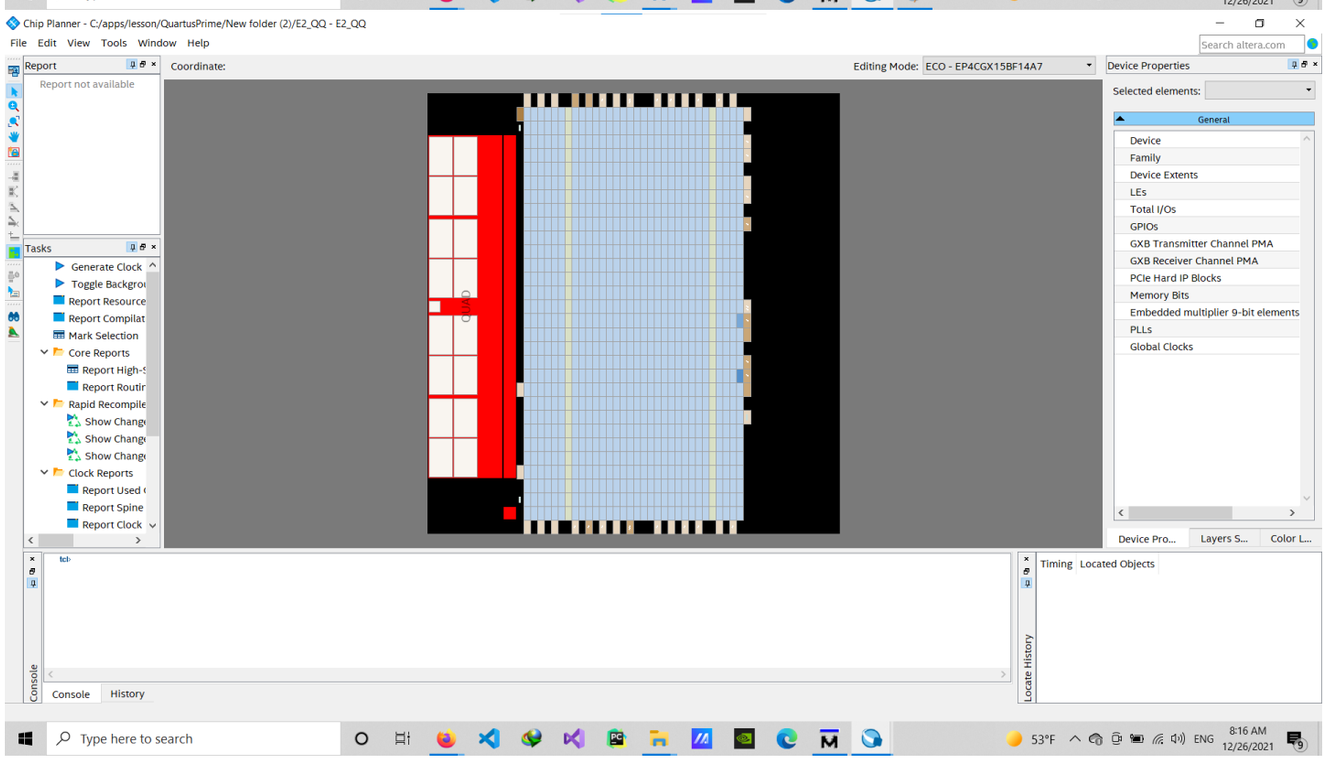


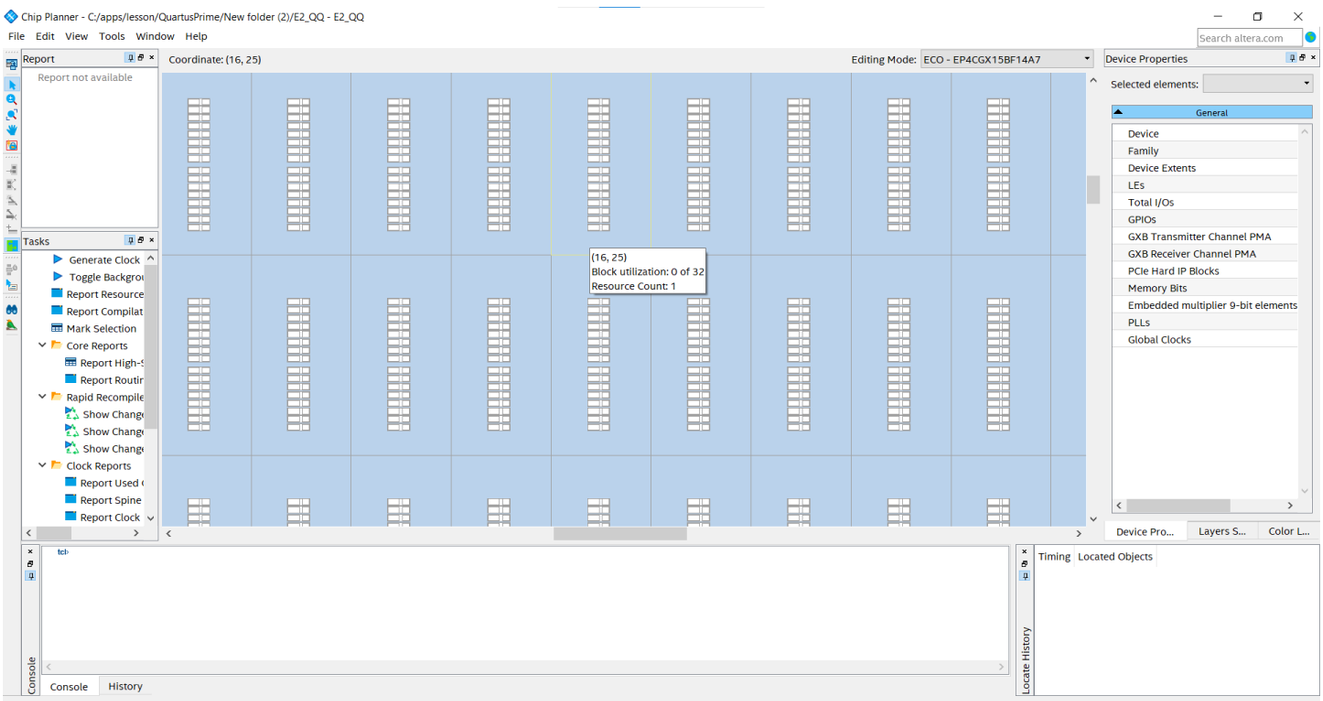
TB:

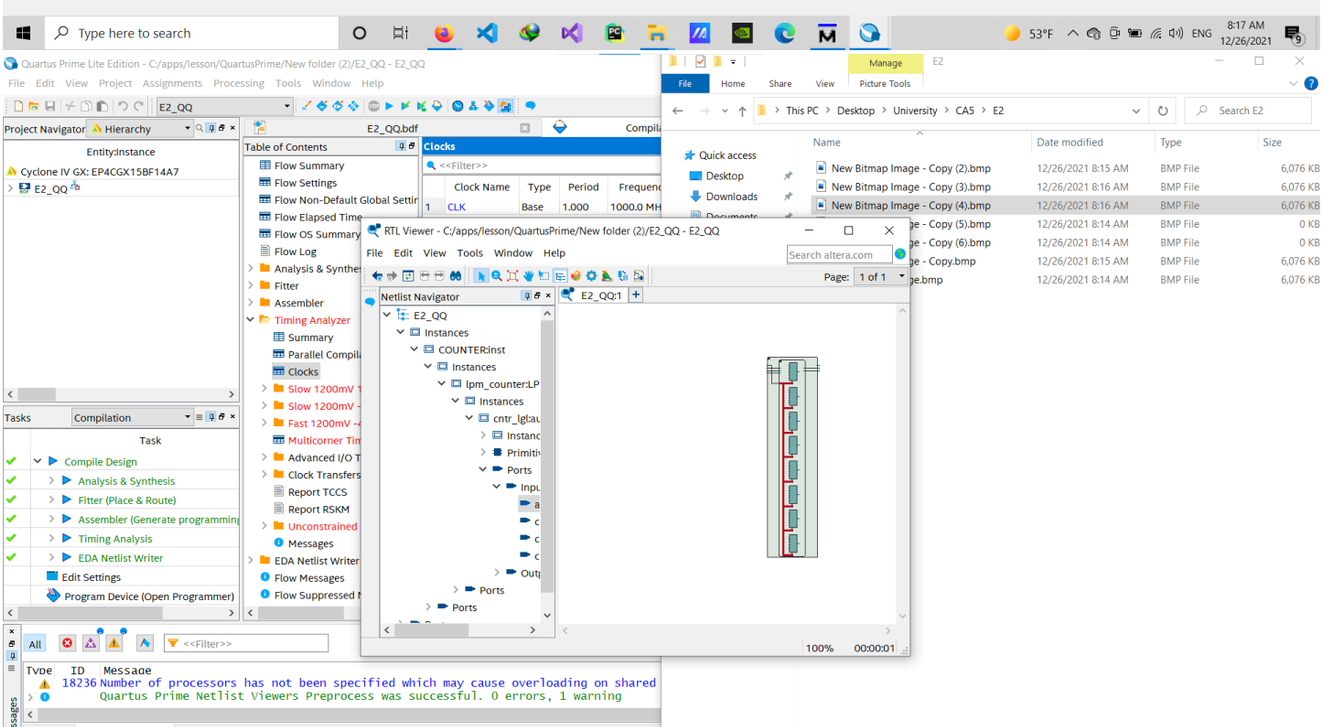
```
`timescale 1ns/1ns
module CA5_E2_TB ();
    logic clock=0,cnt=1,en=1,reset=0;
    wire ccoo;
    wire[7:0] ww;
    E2_QQ xxxx(ccoo,clock,en,cnt,reset,ww);
    always #10 clock=~clock ;
    initial begin
        #5000 cnt=1;
```

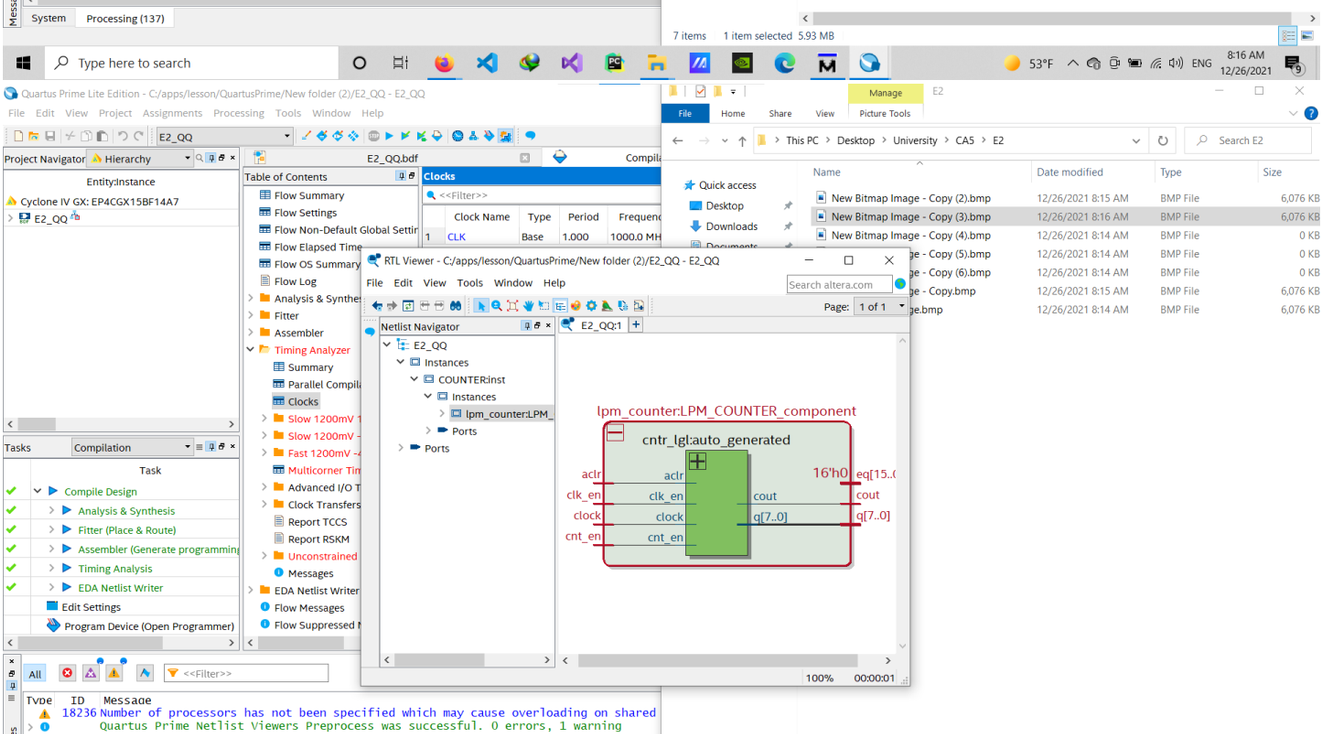
```
        #5000 cnt=0;
        #5000 cnt=1;
        #5000 reset=1;
        #5000 reset=0;
        #10000 $stop;
    end
endmodule
```

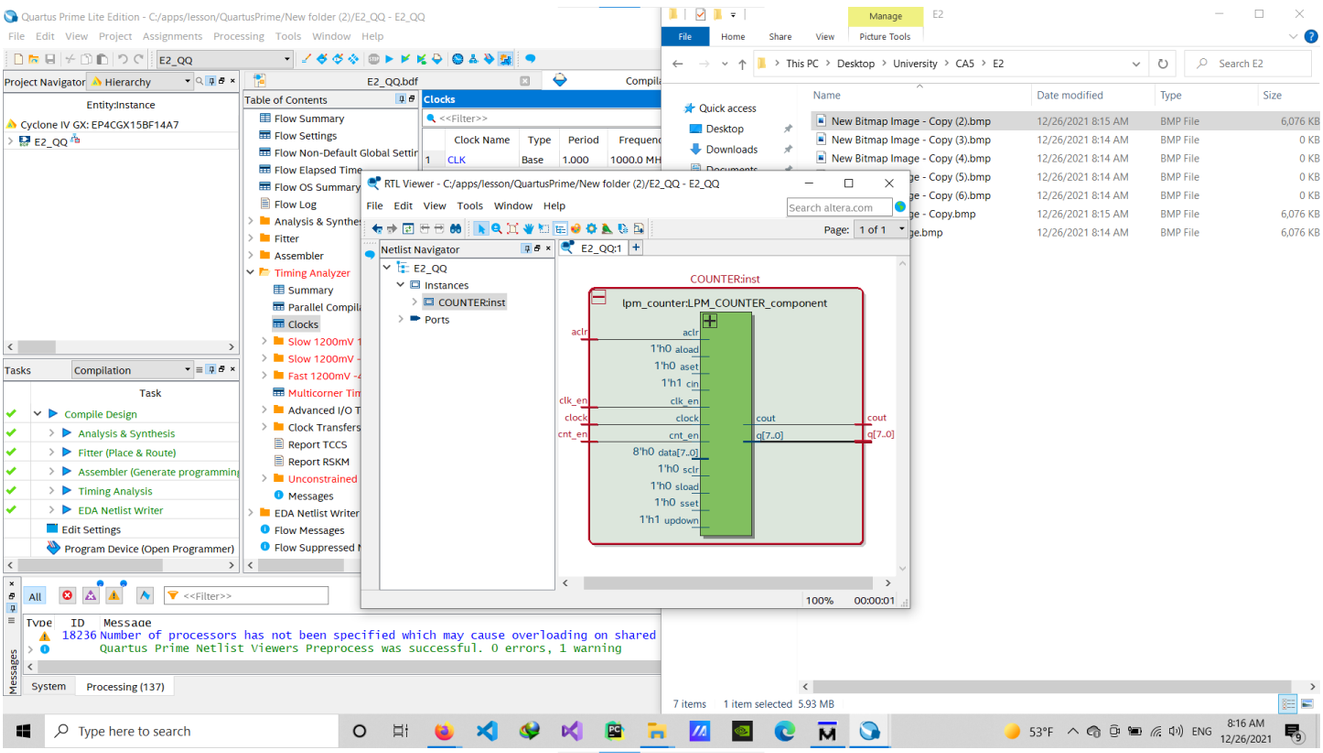


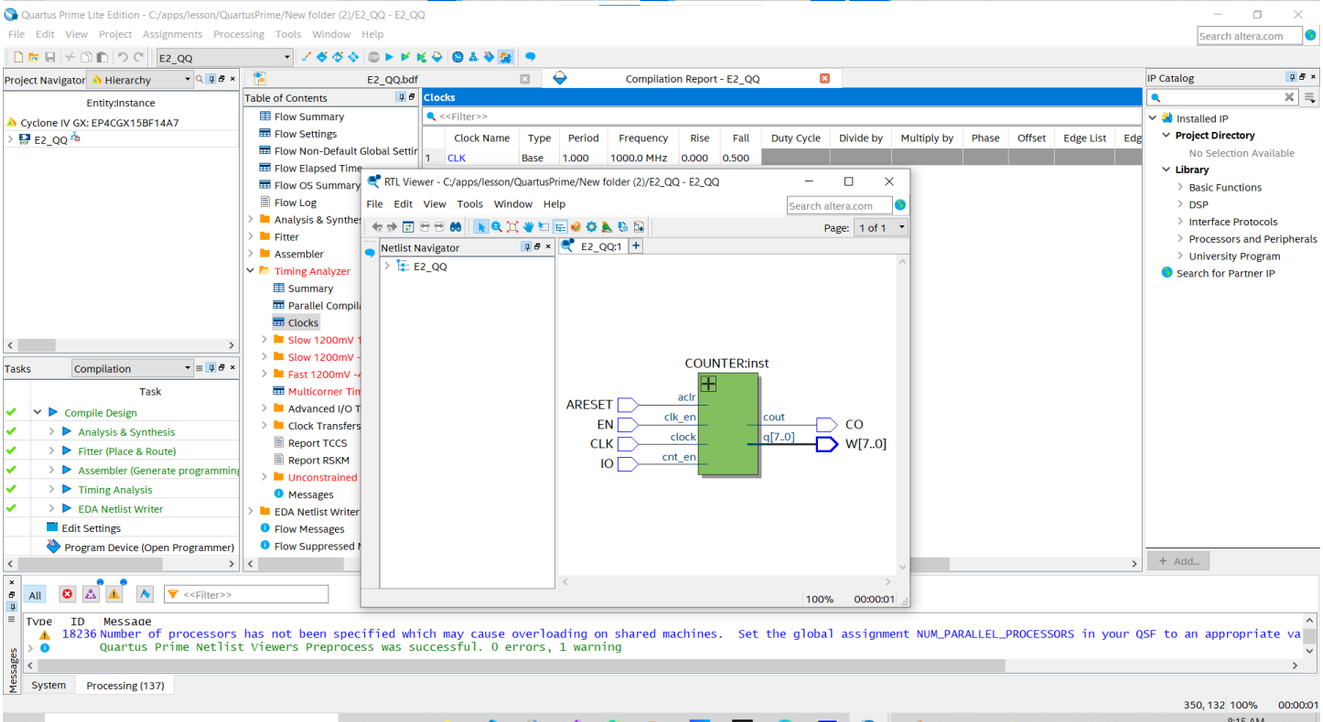


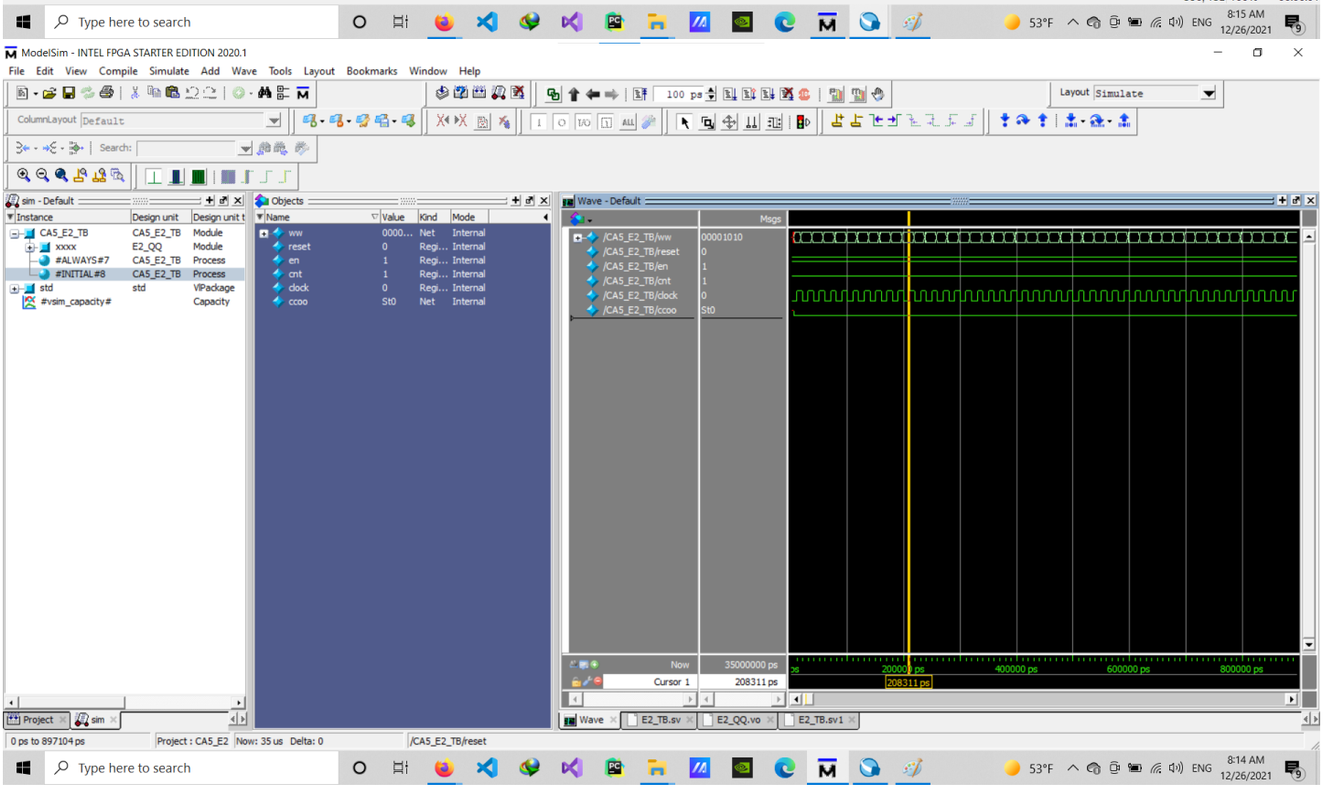

Chip Planner - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
File Edit View Tools Window Help
Report
Report not available
Coordinate: (16, 25)
Editing Mode: ECO - EP4CGX15BF14A7
Device Properties
Selected elements:
General
Device
Family
Device Extents
LEs
Total I/Os
GPIOs
GXB Transmitter Channel PMA
GXB Receiver Channel PMA
PCIe Hard IP Blocks
Memory Bits
Embedded multiplier 9-bit elements
PLLs
Global Clocks
Tasks
Generate Clock
Toggle Backgrou
Report Resource
Report Compilat
Mark Selection
Core Reports
Report High-S
Report Routir
Rapid Recompile
Show Change
Show Change
Show Change
Clock Reports
Report Used
Report Spine
Report Clock
(16, 25)
Block utilization: 0 of 32
Resource Count: 1
Device Pro...
Layers S...
Color L...
Timing
Located Objects
Console
History
Locate History


Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV GX: EP4CGX15BF14A7
E2_QQ
Table of Contents
E2_QQ.bdf
Clocks
Clock Name
Type
Period
CLK
Base
1.000
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
Netlist Navigator
E2_QQ
Instances
COUNTER:inst
lpm_counter:LP
cntr_lgl:au
Ports
E2_QQ:1
100%
00:00:01
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
System
Processing (137)
This PC > Desktop > University > CA5 > E2
Search E2
Name
Date modified
Type
Size
New Bitmap Image - Copy (2).bmp 12/26/2021 8:15 AM BMP File 6,076 KB
New Bitmap Image - Copy (3).bmp 12/26/2021 8:16 AM BMP File 6,076 KB
New Bitmap Image - Copy (4).bmp 12/26/2021 8:16 AM BMP File 6,076 KB
7 items
1 item selected 5.93 MB

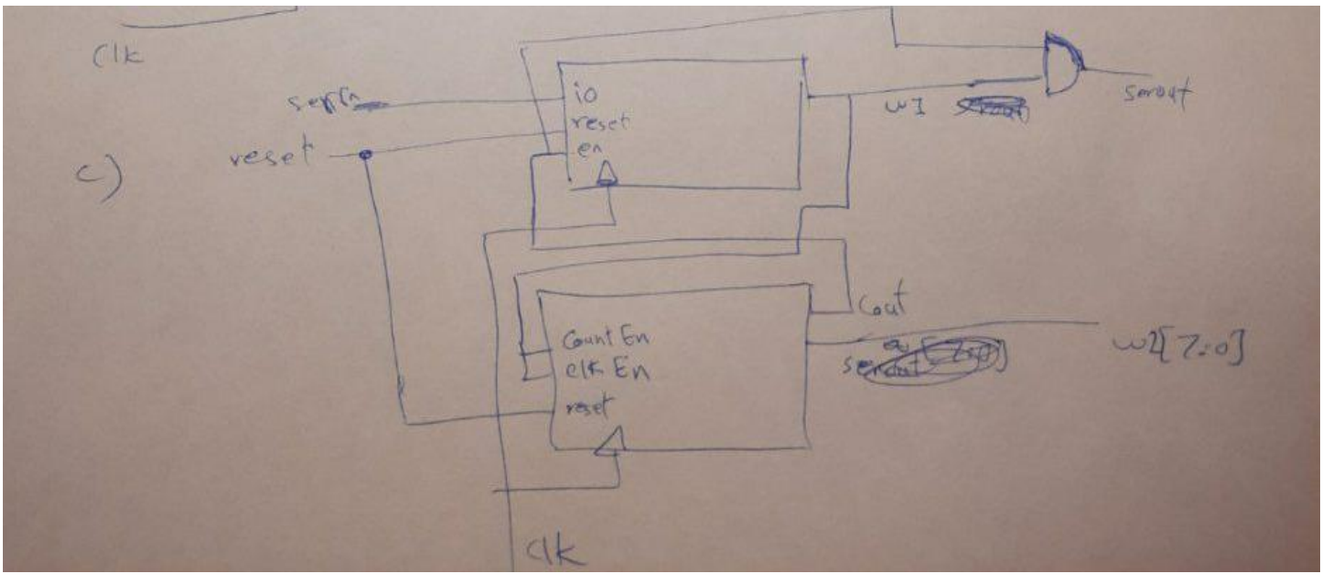

Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
lpm_counter:LPM_COUNTER_component
cntr_lgl:auto_generated
aclr
clk_en
clock
cnt_en
cout
q[7..0]
16'h0
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
7 items
1 item selected 5.93 MB


Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
COUNTER:inst
lpm_counter:LPM_COUNTER_component
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning


Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
Compilation Report - E2_QQ
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (2)/E2_QQ - E2_QQ
COUNTER:inst
ARESET
EN
CLK
IO
CO
W[7..0]
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate va
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning

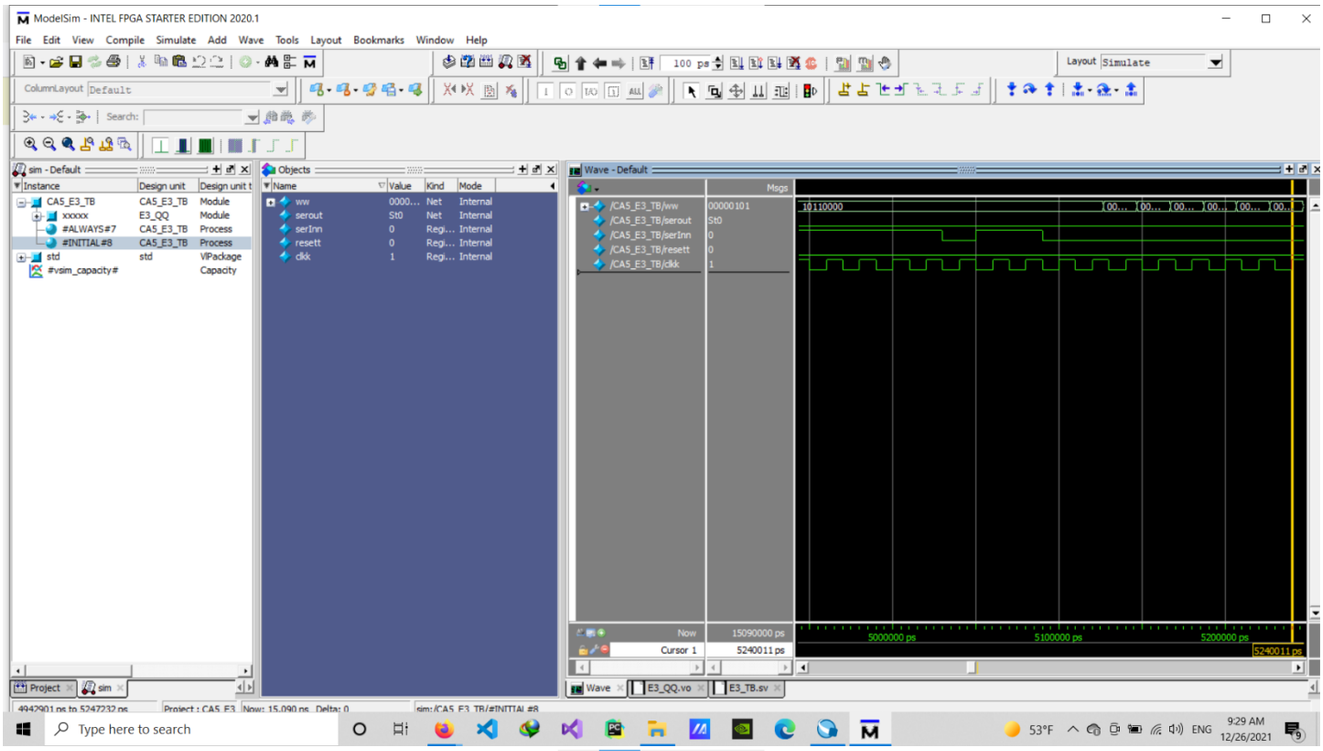

ModelSim - INTEL FPGA STARTER EDITION 2020.1
Wave - Default
/CA5_E2_TB/ww
/CA5_E2_TB/reset
/CA5_E2_TB/en
/CA5_E2_TB/cnt
/CA5_E2_TB/clock
/CA5_E2_TB/ccoo

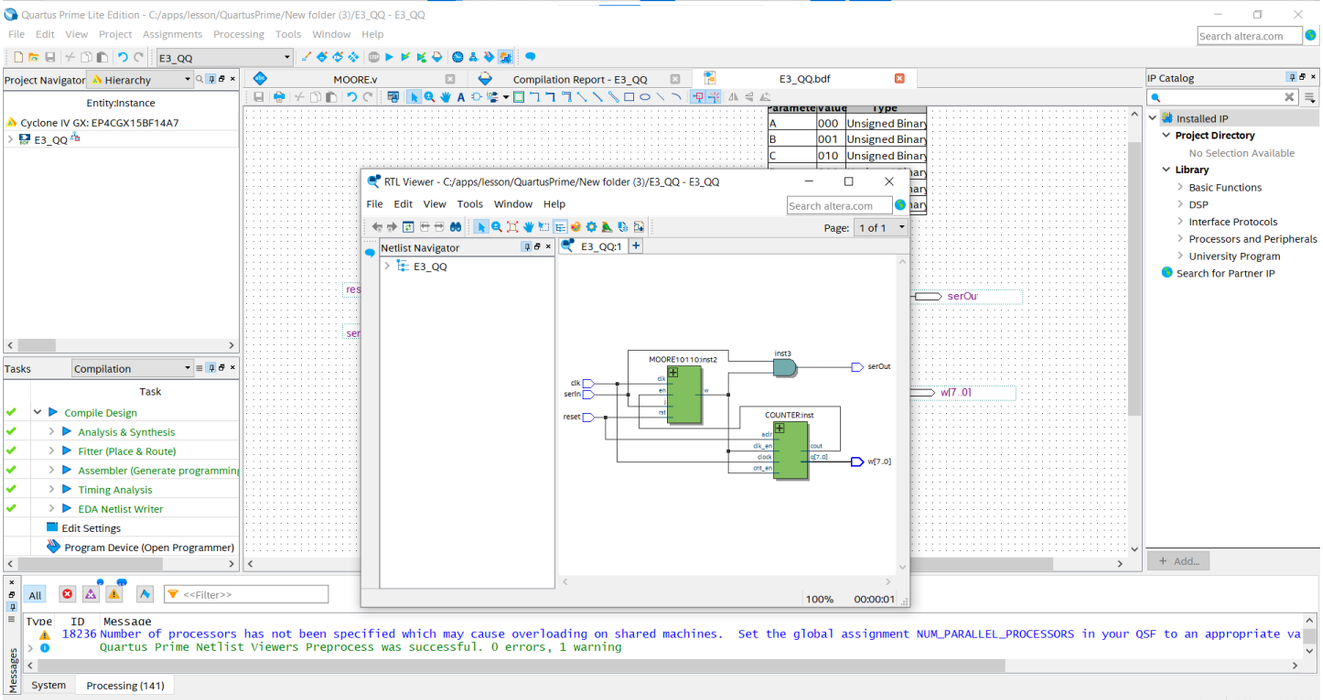
3:

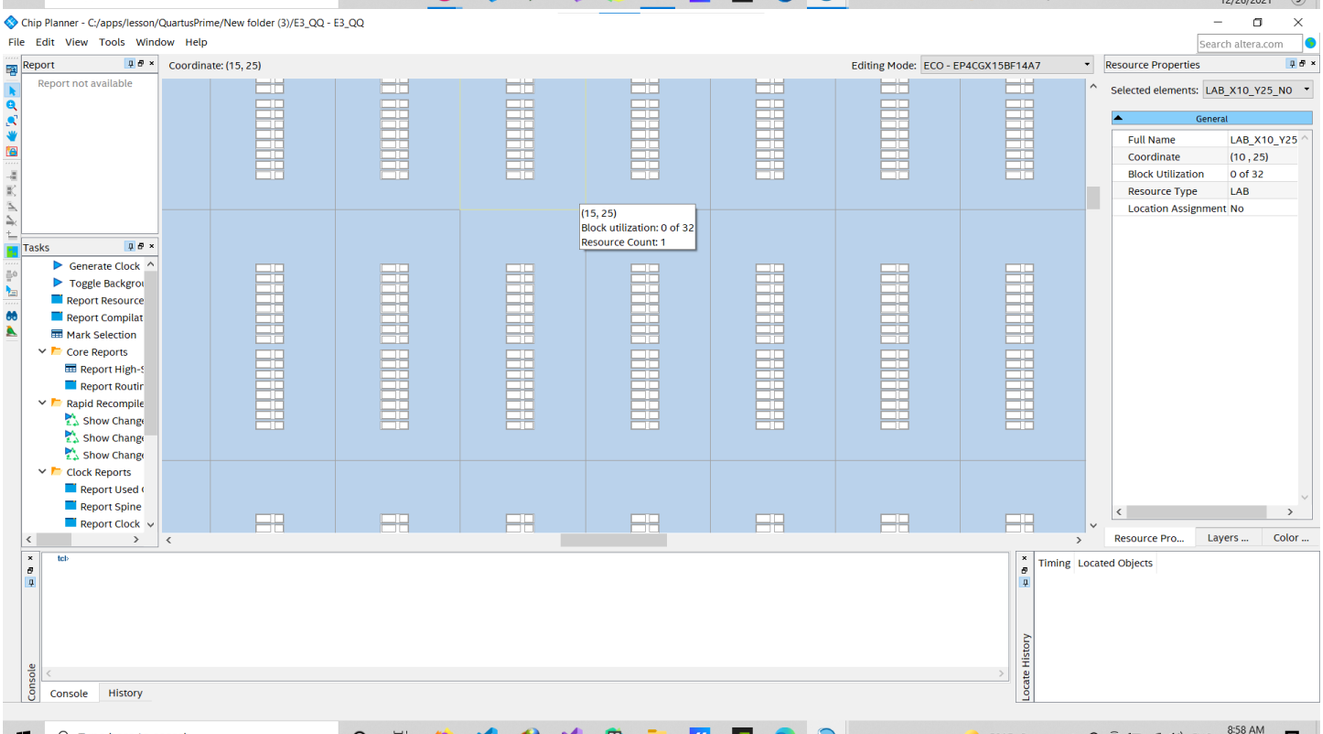


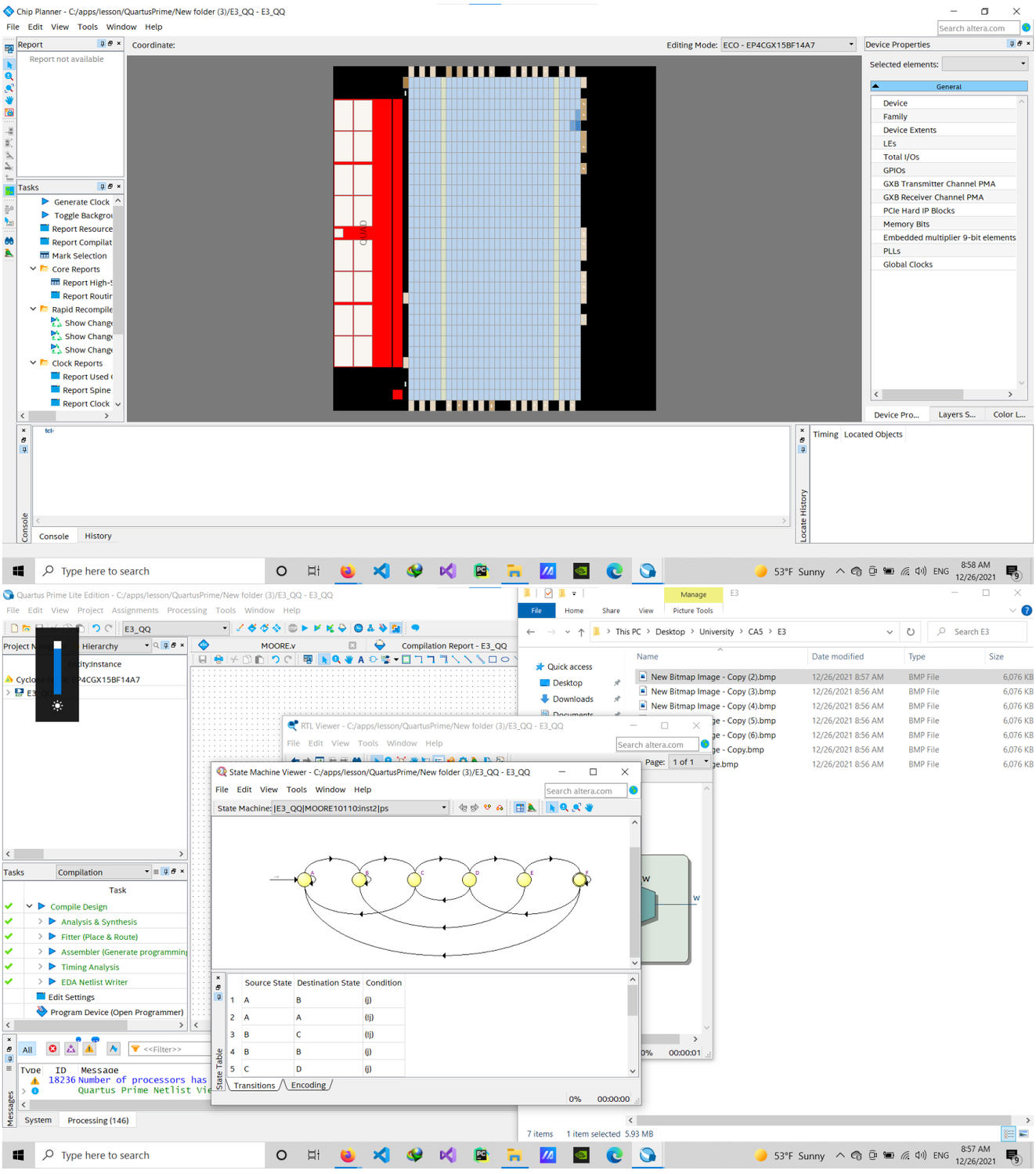
TB:

```
`timescale 1ns/1ns
module CA5_E3_TB ();
    logic serInn=1,clkk=1,resett=0;
    wire serout;
    wire[7:0] ww;
    E3_QQ xxxxx(serout,serInn,clkk,resett,ww);
    always #10 clkk=~clkk ;
    initial begin
        #4490 resett=0;
        #250 resett=1;
        #250 resett=0;
        #20 serInn=1;
        #20 serInn=0;
        #20 serInn=1;
        #20 serInn=1;
        #20 serInn=0;
        #10000 $stop;
    end
endmodule
```

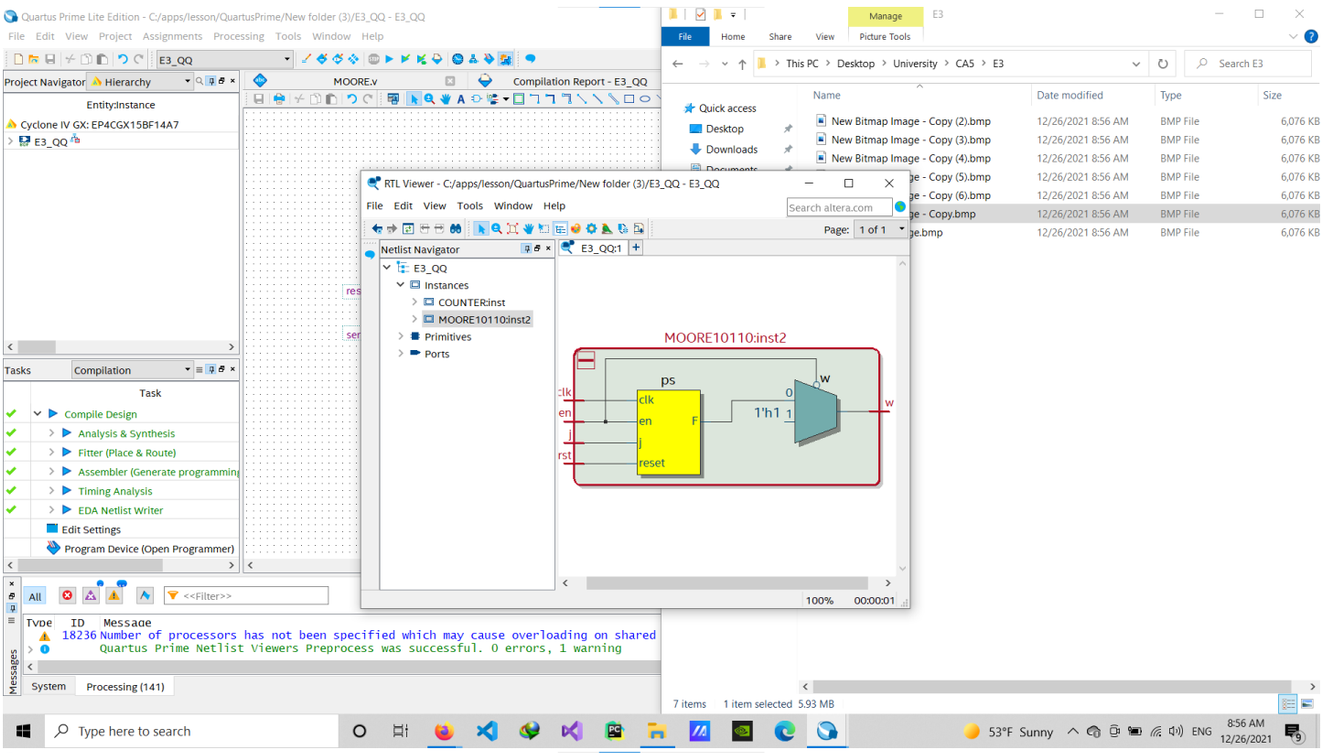

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Project
sim
Wave
E3_QQ.vo
E3_TB.sv
Type here to search
53°F
ENG
9:29 AM
12/26/2021

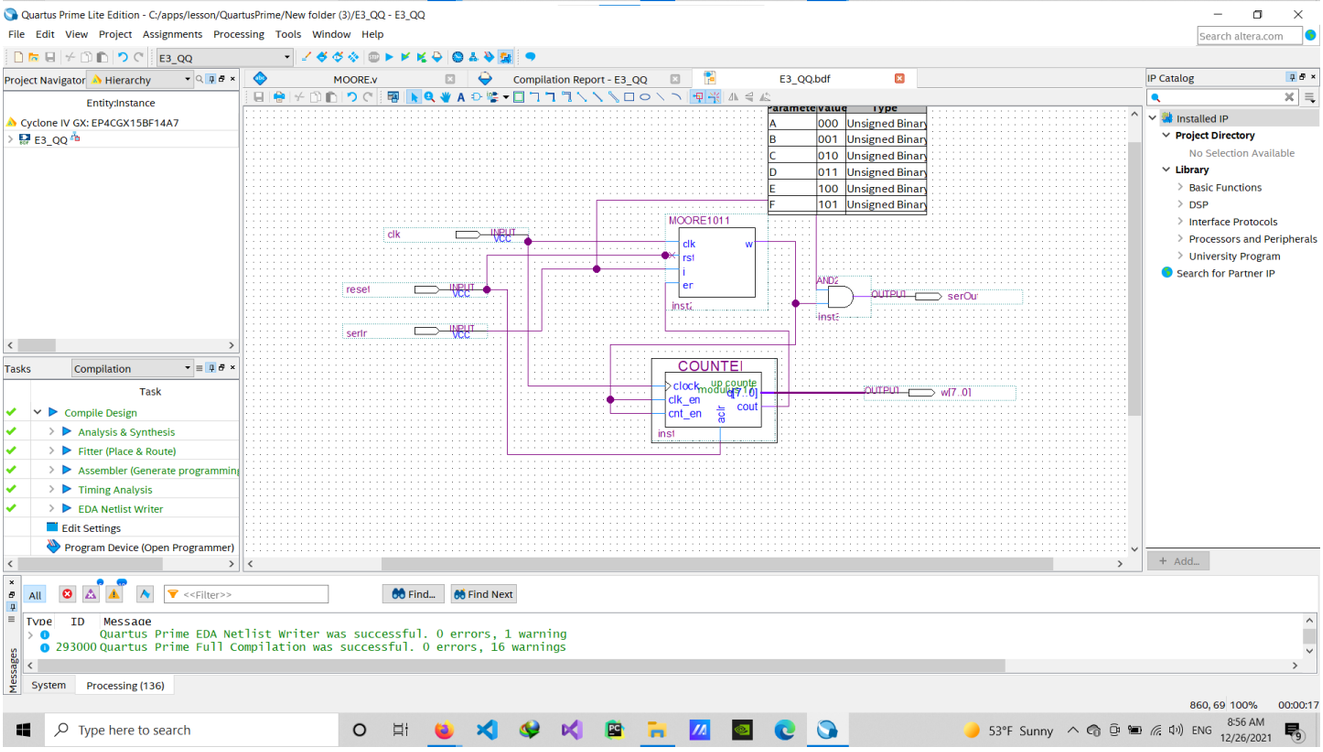

Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV GX: EP4CGX15BF14A7
E3_QQ
MOORE.v
Compilation Report - E3_QQ
E3_QQ.bdf
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
Netlist Navigator
E3_QQ:1
Tasks
Compilation
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate va
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
System
Processing (141)
Type here to search
53°F Sunny
ENG
8:56 AM
12/26/2021


Chip Planner - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
File Edit View Tools Window Help
Report
Report not available
Coordinate: (15, 25)
Editing Mode: ECO - EP4CGX15BF14A7
Resource Properties
Selected elements: LAB_X10_Y25_N0
General
Full Name LAB_X10_Y25
Coordinate (10 , 25)
Block Utilization 0 of 32
Resource Type LAB
Location Assignment No
(15, 25)
Block utilization: 0 of 32
Resource Count: 1
Tasks
Generate Clock
Report Resource
Report Compilat
Mark Selection
Core Reports
Rapid Recompile
Clock Reports
Timing Located Objects
Console
History
Type here to search
53°F Sunny
ENG
8:58 AM
12/26/2021


Chip Planner - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
File Edit View Tools Window Help
Report
Report not available
Coordinate:
Editing Mode: ECO - EP4CGX15BF14A7
Device Properties
Selected elements:
General
Device
Family
Device Extents
LEs
Total I/Os
GPIOs
GXB Transmitter Channel PMA
GXB Receiver Channel PMA
PCIe Hard IP Blocks
Memory Bits
Embedded multiplier 9-bit elements
PLLs
Global Clocks
Tasks
Generate Clock
Report Resource
Report Compilat
Mark Selection
Core Reports
Rapid Recompile
Clock Reports
Report Spine
Report Clock
Device Pro...
Layers S...
Color L...
Timing
Located Objects
Console
History
Locate History
Type here to search
53°F Sunny
ENG
8:58 AM
12/26/2021

Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
File Edit View Project Assignments Processing Tools Window Help
E3_QQ
Hierarchy
MOORE.v
Compilation Report - E3_QQ
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Messages
System
Processing (146)
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
State Machine Viewer - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
State Machine: |E3_QQ|MOORE10110:inst2|ps
Source State
Destination State
Condition
1 A B (j)
2 A A (ij)
3 B C (ij)
4 B B (j)
5 C D (j)
Transitions
Encoding
State Table
Manage
E3
File Home Share View Picture Tools
This PC › Desktop › University › CA5 › E3
Search E3
Quick access
Desktop
Downloads
Name
Date modified
Type
Size
New Bitmap Image - Copy (2).bmp 12/26/2021 8:57 AM BMP File 6,076 KB
New Bitmap Image - Copy (3).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (4).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (5).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (6).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy.bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image.bmp 12/26/2021 8:56 AM BMP File 6,076 KB
7 items
1 item selected 5.93 MB
Type here to search
53°F Sunny
ENG
8:57 AM
12/26/2021


Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
File Edit View Project Assignments Processing Tools Window Help
Project Navigator Hierarchy
Entity:Instance
Cyclone IV GX: EP4CGX15BF14A7
E3_QQ
MOORE.v
Compilation Report - E3_QQ
RTL Viewer - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
Netlist Navigator
E3_QQ
Instances
COUNTER:inst
MOORE10110:inst2
Primitives
Ports
E3_QQ:1
MOORE10110:inst2
ps
clk
en
reset
F
1'h1
w
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Type ID Message
18236 Number of processors has not been specified which may cause overloading on shared
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
System Processing (141)
This PC > Desktop > University > CA5 > E3
Search E3
Quick access
Desktop
Downloads
Name
Date modified
Type
Size
New Bitmap Image - Copy (2).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (3).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (4).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (5).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
New Bitmap Image - Copy (6).bmp 12/26/2021 8:56 AM BMP File 6,076 KB
Copy.bmp 12/26/2021 8:56 AM BMP File 6,076 KB
.bmp 12/26/2021 8:56 AM BMP File 6,076 KB
7 items 1 item selected 5.93 MB
Type here to search
53°F Sunny
ENG
8:56 AM
12/26/2021


Quartus Prime Lite Edition - C:/apps/lesson/QuartusPrime/New folder (3)/E3_QQ - E3_QQ
File Edit View Project Assignments Processing Tools Window Help
Project Navigator Hierarchy
Entity:Instance
Cyclone IV GX: EP4CGX15BF14A7
E3_QQ
MOORE.v
Compilation Report - E3_QQ
E3_QQ.bdf
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
A 000 Unsigned Binary
B 001 Unsigned Binary
C 010 Unsigned Binary
D 011 Unsigned Binary
E 100 Unsigned Binary
F 101 Unsigned Binary
clk
reset
serIr
INPUT
VCC
MOORE1011
clk
rst
i
er
w
inst
AND2
OUTPUT
serOu
inst2
COUNTER
clock
clk_en
cnt_en
up counte
modulus[7..0]
q[7..0]
cout
aclr
inst
wf7..0]
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Find... Find Next
Type ID Message
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 16 warnings
System Processing (136)
860, 69 100% 00:00:17
Type here to search
53°F Sunny
ENG
8:56 AM
12/26/2021