# ELECENG 2EI4

# Electronic Devices and Circuits I

# Design Project 5

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As a future member of the engineering profession, I, **[Ali Bandali, 400532826]** am responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

## Research

Digital-to-Analog Converters (DACs) are essential components that enable digital systems to interact with the analog world, finding applications in fields such as audio reproduction and instrumentation control. For example, in audio systems, DACs convert digital music files into analog signals to drive speakers, while in sensor and actuator networks, they precisely generate voltage levels required for accurate control or measurement. [5]

In this project, the weighted resistor DAC was selected for its simplicity and clarity in demonstrating the core principles of DAC operation. This design assigns specific resistor values to each digital bit, with the weighted contributions summed by an operational amplifier to produce the desired full-scale voltage output. However, the design must carefully consider factors such as resistor tolerances and op-amp imperfections, which can introduce gain and offset errors as well as differential non-linearity, potentially affecting overall accuracy. [1]

The full-scale voltage represents the maximum output voltage that the DAC is designed to achieve. It defines the upper limit of the analog signal range—for instance, a DAC specified for a 5V full-scale voltage should ideally produce output levels spanning from 0V to 5V. This parameter is pivotal because it directly affects the dynamic range and resolution of the conversion process. Inaccuracies in establishing V_FS can lead to clipping (if set too low) or underutilization of the available range (if set too high), which in turn impacts the fidelity of the analog signal. [3]

Gain error is the deviation between the actual output slope of the DAC and the ideal linear slope over the full input range. In an ideal DAC, each incremental increase in the digital input should lead to an equal, proportional step in the analog output. However, imperfections—such as resistor tolerances in a weighted resistor DAC and non-ideal behaviors of the operational amplifier—can alter the slope. [4]

Digital non-linearity, often quantified as Differential Non-Linearity (DNL), measures the inconsistency between successive output voltage steps. Ideally, the transition from one digital code to the next should yield identical voltage increments; however, real-world imperfections can cause these steps to vary. If the DNL exceeds one least significant bit (LSB) at any point, the DAC may exhibit non-monotonic behavior, meaning that an increase in the digital input might not produce a corresponding increase in the analog output. This non-linearity can lead to missing codes and overall degraded performance, making it crucial to carefully design and calibrate the resistor network and other circuit components in a weighted resistor DAC. [5]

## Introduction

The purpose of this project is to design, simulate, and build a 3-bit Digital-to-Analog Converter (DAC) that delivers a full-scale analog output of 5V. The converter translates digital input signals into corresponding analog voltages by employing a summing amplifier configuration. In this basic design, three digital input signals are weighted and combined through a carefully selected resistor network. Each digital input, representative of a binary bit, is applied through resistors of differing values, specifically 1kΩ, 2kΩ, and 4kΩ, to form a weighted sum that is later scaled at the output stage via a feedback resistor. This strategy yields eight unique output voltage levels that linearly span from 0V (for a digital input of 000) to 5V (for a digital input of 111).

The design not only meets the specification of a 5V full-scale range but also adheres to constraints regarding component availability and current limitations on the digital bit lines. The design also considered important practical constraints. The available DC supplies from the AD3 and the limitations on the current drawn from the digital bit lines (less than 1μA) were primary factors influencing the selection of components. Additionally, the possibility of inverting the digital logic levels (treating 0V as logic-1 and 5V as logic-0) was used to simplify the design without requiring extra inversion circuitry. The design process included both simulation and hands-on experimentation to verify that the output levels matched the intended calculations, as well as to adjust the resistor values for minimal deviation from ideal performance.

### Circuit Schematic:

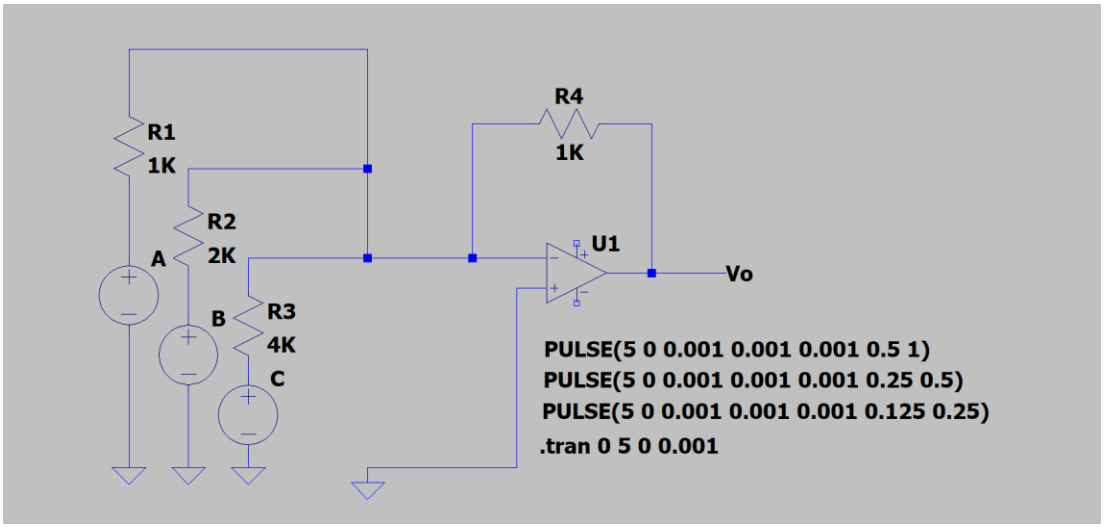



Figure 1: circuit Schematic

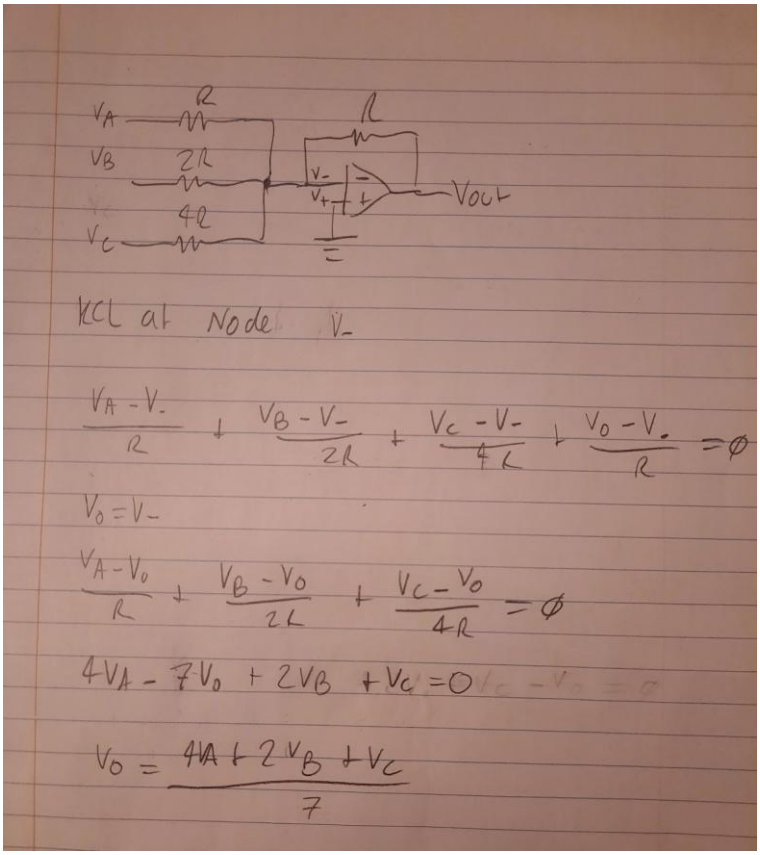
## Description

The core design of the DAC circuit is based on the operational amplifier's summing configuration. As illustrated in the circuit schematic, the circuit integrates three pulse voltage sources that simulate digital bit inputs. These inputs, with levels of 0V and 5V, are directed through individual resistor branches into the inverting input of the summing amplifier. The resistors are chosen to establish a specific weighting, 1kΩ, 2kΩ, and 4kΩ, such that the combined effect of the inputs is described by the equation:

$$Vo = \frac{(4VA + 2VB + VC)}{7}$$

The equation was derived from the resistance ratios and determines how each bit's voltage contribution is scaled before they are summed. The circuit also includes a feedback resistor from the output back to the amplifier's inverting input, thereby stabilizing the gain of the summing network.

## Calculations:



## Simulated circuit results

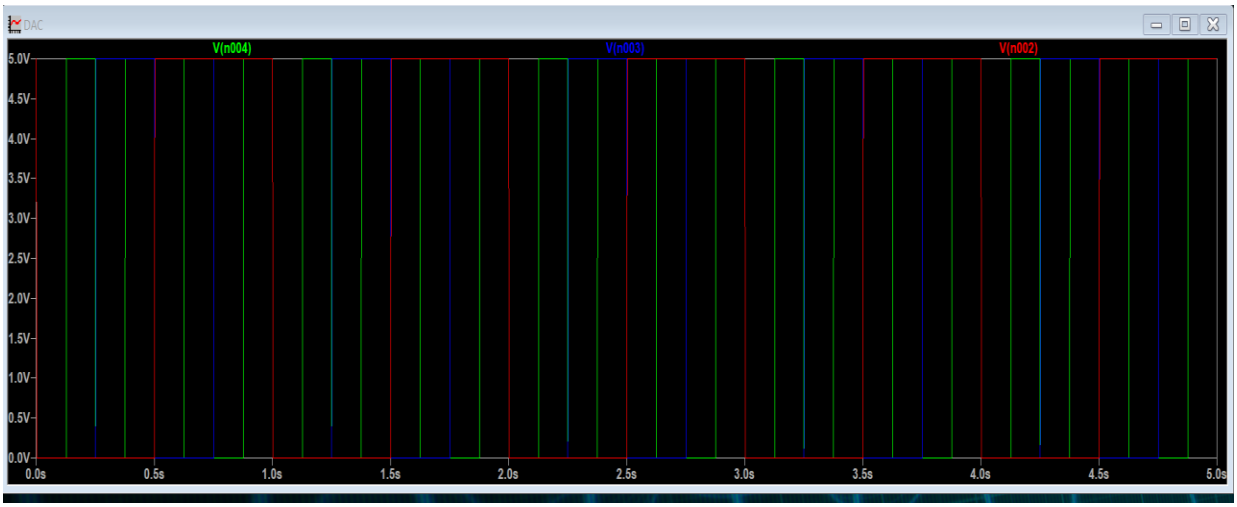



Figure 2: Simulated circuit Inputs

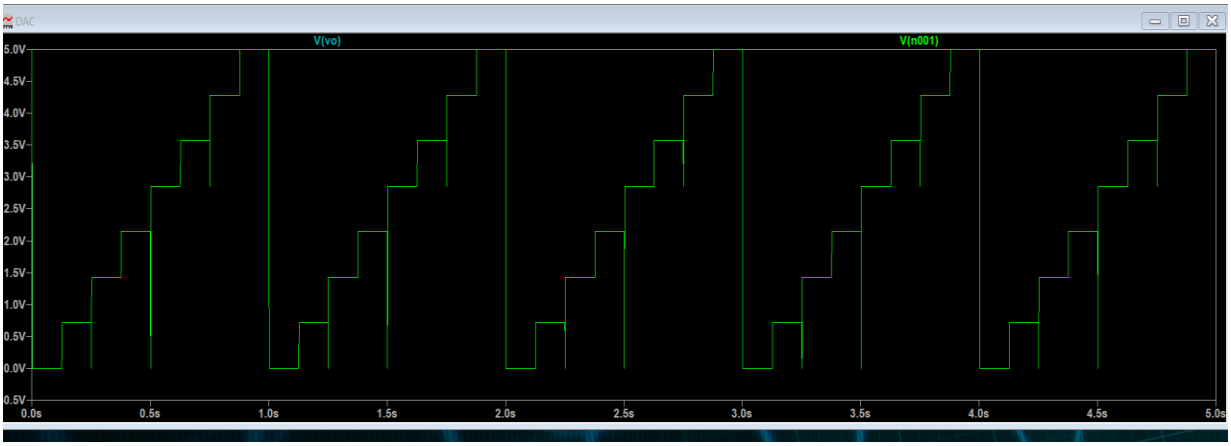


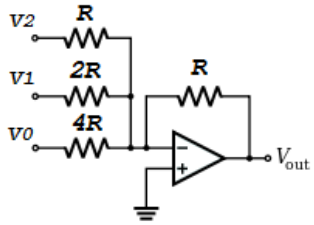

Figure 3: Simulated circuit outputs

Within this configuration, the digital bit inputs, modeled as pulse signals operating with differing periods, ensure that every combination of binary inputs appears during the simulation cycle. Through experimentation and calculation, the design achieves a set of discrete analog voltage levels corresponding to each unique digital code from 0 for 000 up to 5V for 111. Furthermore, while the resistor values primarily set the ratios necessary for the digital-to-analog conversion, they also play a significant role in dictating the overall accuracy of the output, as reflected in potential gain errors and differential non-linearity which are critical in practical applications.

- VA = 0V, VB = 0V, VC = 0V (binary 000): Analog Output = 0V
- VA = 0V, VB = 0V, VC = 5V (binary 001): Analog Output ≈ 0.712V
- VA = 0V, VB = 5V, VC = 0V (binary 010): Analog Output ≈ 1.428V
- VA = 0V, VB = 5V, VC = 5V (binary 011): Analog Output ≈ 2.141V
- VA = 5V, VB = 0V, VC = 0V (binary 100): Analog Output ≈ 2.852V
- VA = 5V, VB = 0V, VC = 5V (binary 101): Analog Output ≈ 3.574V
- VA = 5V, VB = 5V, VC = 0V (binary 110): Analog Output ≈ 4.281V
- VA = 5V, VB = 5V, VC = 5V (binary 111): Analog Output = 5V

These results  illustrate how the resistor network translates specific digital input combinations into accurate analog voltage levels.

## Circuit Design reference




From the summing amplifier circuit (see equation 6), the output voltage is

$$V_{out} = -R\left(\frac{V_2}{R} + \frac{V_1}{2R} + \frac{V_0}{4R}\right)$$

Figure 4: circuit design found using electronics course website [1]

The circuit design was further inspired by models presented in the online electronics course website [1]. The circuit model shown (figure 4) provided the initial concept for digital-to-analog conversion in a simple 3-bit design. I adapted this model to suit the constraints of my project, including the limited DC supplies from the AD3 and the available components in my kit. This approach enabled me to develop a DAC that fulfills the project requirements while maintaining accurate performance and linearity across the full range of input values.

## Measurement and Analysis

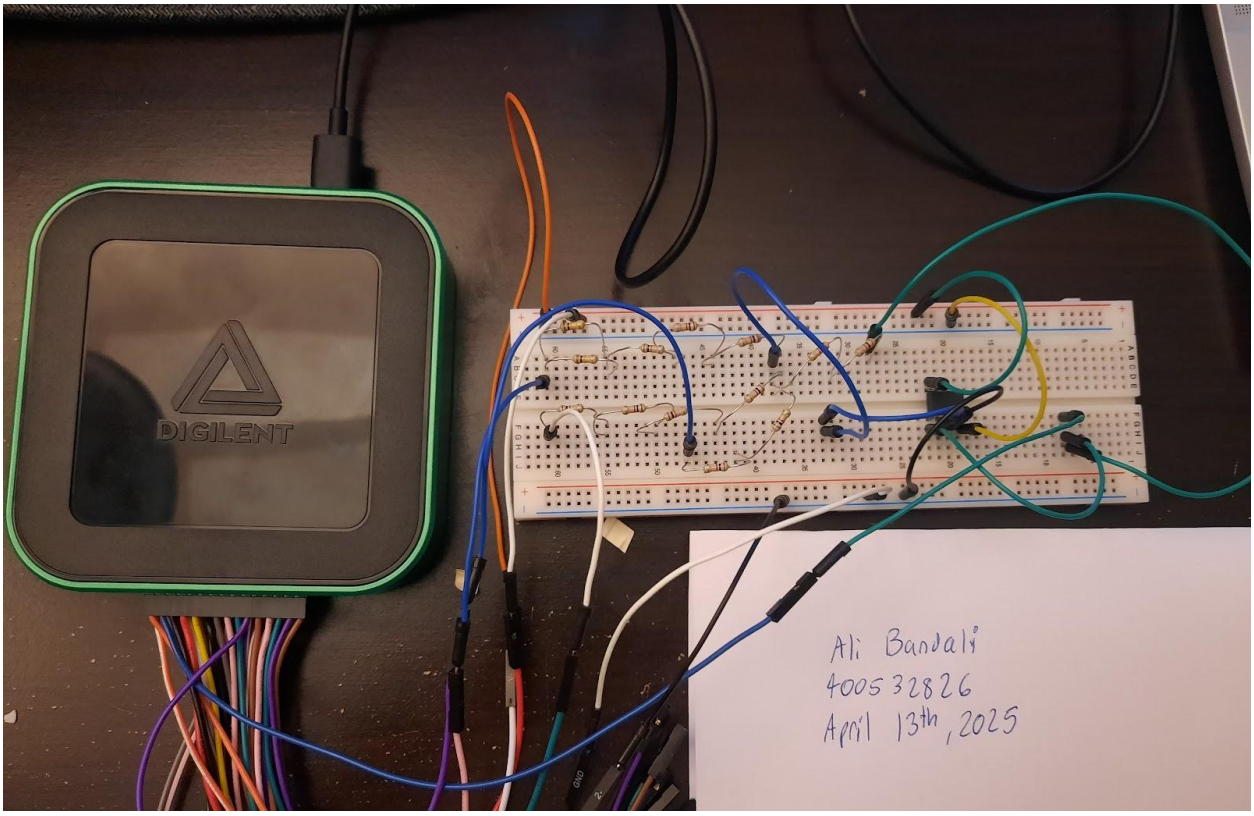



Figure 5: Physical Circuit

# Digital Inputs

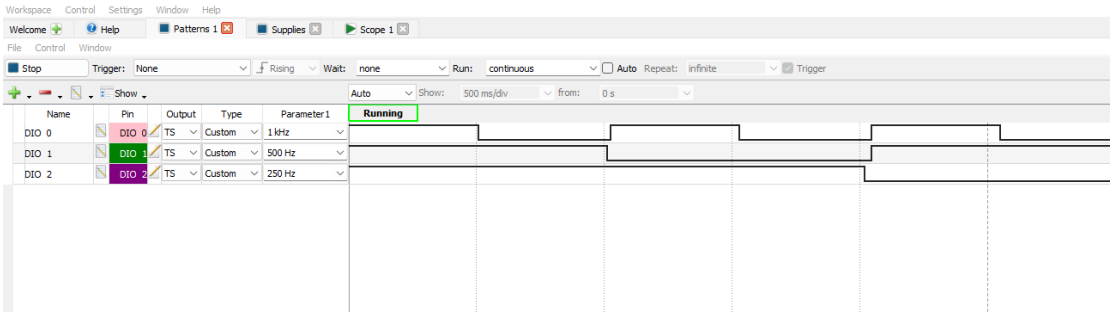



Figure 6: Patterns generator digital inputs

The Analog Discovery 3 kit's Pattern Generator was used to configure its digital I/O pins as inputs and produce clock pulses at 250 Hz, 500 Hz, and 1 kHz, matching the waveforms from our LTSpice simulations. Those signals were then captured and examined with the device's Oscilloscope feature to observe the resulting output voltage waveforms.

# Scope Output

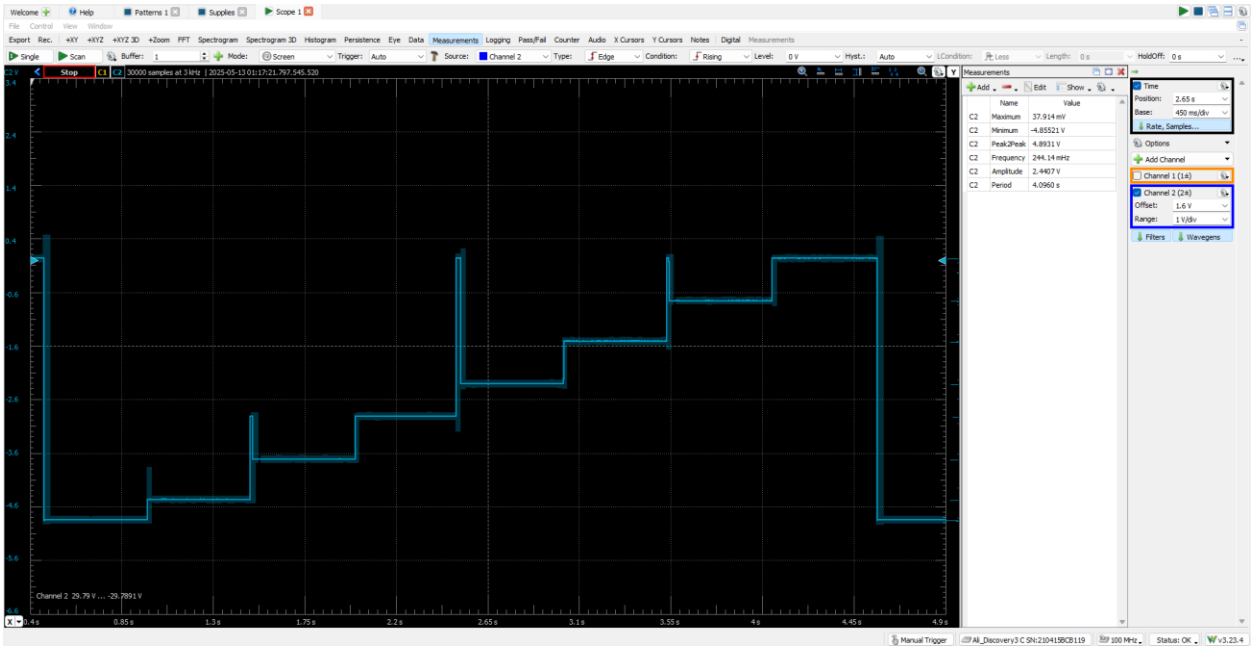


Figure 6: Physical Circuit Output

Analyzing the graph's profile, we can observe that while the voltage step drops are quite consistent and that the overall curve conforms to the expected shape of the design. The primary discrepancy lies in the range of voltage values: the maximum voltage (Vmax) was measured at -4.8521 V instead of the anticipated 5V, and the minimum voltage (Vmin) was found to be 0.38 V rather than the expected 0V.

# Gain error calculations

The gain error is the difference between the circuit's theoretically expected peak voltage and the peak voltage actually measured, arising from factors like internal resistances and measurement-device inaccuracies.

By applying the gain error equation,

$$E\_Gain = \left(\frac{(V_{measured} - V_{expected})}{V_{expected}}\right) \times 100\%,$$

the error value is (5V – 4.8521V)/ 5V x 100% = 2.96%

# Maximum differential non-linearity.

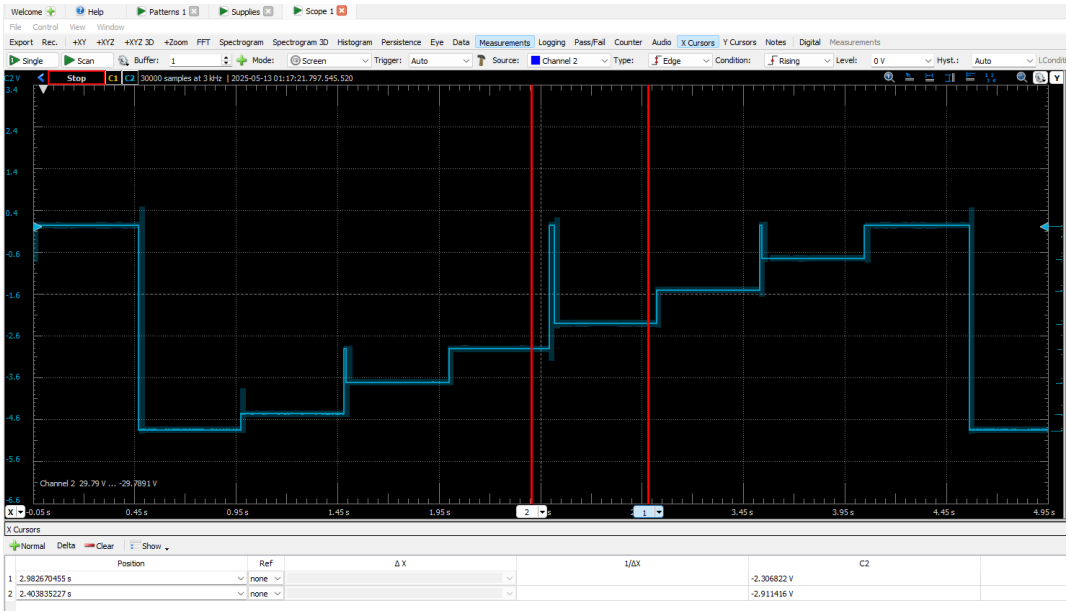



Figure 7: Voltage Step level difference measurement

In an ideal 8-step DAC with a 5 V full scale, each least significant bit represents 0.625 V. Differential non-linearity (DNL) quantifies the deviation of each measured step from this ideal increment, normalized by 0.625 . The maximum of these normalized deviations, $DNL_{max}$, defines the worst-case non-linearity. For example, a measured step of 0.6042  V yields

$$DNL = \frac{(0.625 - 0.6042V)}{0.625} \approx 3.3\%$$

A high $DNL_{max}$ reflects unevenly spaced output levels, which can cause non-linear behavior or missing codes.

# Offset Error:

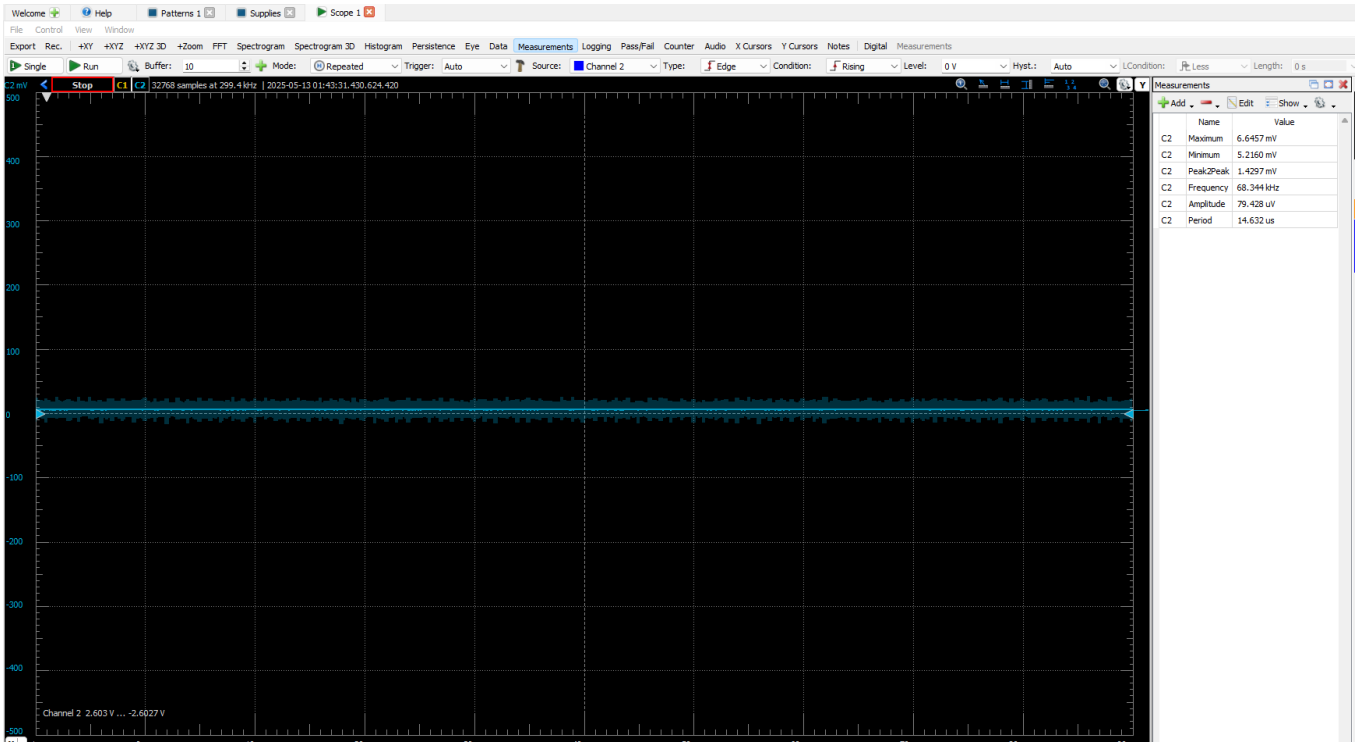



Figure 8: Scope output for bits 000

The offset error is defined as the output deviation from 0 V when the DAC's digital input word is zero. It is measured by driving all input bits to logic low (bits 000) and recording the resulting output voltage. In this implementation, the offset error varied between a minimum of 5.2160 mV and a maximum of 6.54 mV. Such a baseline shift arises from non-ideal behavior of components device mismatches, amplifier input offsets, leakage currents and internal bias networks and directly impacts linearity by introducing a constant voltage offset across the full transfer range.

# Discussion

Several factors contribute to the observed deviations in this 8-step DAC implementation. Drive waveforms were generated by the Analog Discovery 3 Pattern Generator at 250 Hz, 500 Hz, and 1 kHz and captured with the onboard oscilloscope. Resistor tolerances alter the precise summing ratios, while the finite open-loop gain, input offset voltage, and output impedance of the op-amp introduce amplification errors. In addition, slight variations in digital input timing or amplitude, supply-rail fluctuations, and loading or noise from the measurement setup further perturb the output levels.

## Justification for Design Choice and Alternative Implementations

I selected the summing amplifier configuration with resistive weighting for this 3-bit DAC due to its simplicity and direct mapping of digital inputs to analog outputs. This approach offers a straightforward circuit topology that is easy to implement and troubleshoot, which was particularly important given the constraints on available components and the need to maintain low current draw on digital lines. The design emphasizes an intuitive method for establishing voltage levels through a well-defined resistor network, where the scaling of each digital bit is directly controllable by the resistor ratios.

While alternative DAC architectures, such as the R-2R ladder design, can offer superior linearity and reduced sensitivity to component mismatches, they often require more precise resistor matching and a more intricate layout. Such alternatives can be challenging to implement with limited resources or in educational environments where ease of understanding and prototyping are prioritized. In comparison, the summing amplifier-based design allowed me to achieve a functional DAC with a clear correspondence between theory and practice, despite some non-idealities. The simplicity of this method makes it accessible for hands-on learning and iterative improvement, and it provides a solid basis upon which enhancements, such as better component matching or improved op-amp selection, could be applied in future designs.

Overall, addressing the sources of error through careful component selection, rigorous testing, and potential calibration can significantly improve DAC performance. The chosen design meets the project's primary objectives while offering opportunities for further refinement and serves as a robust platform for exploring digital-to-analog conversion principles.

## References

[1] Electronic Tutorials, “Summing Amplifier is an Op-amp Voltage Adder,” *Basic Electronics Tutorials*, Feb. 2019. https://www.electronics-tutorials.ws/opamp/opamp_4.html (accessed Apr. 13, 2025).

[2] Electronics Tutorials, “Binary Weighted Digital to Analogue Converter,” *Basic Electronics Tutorials*, Oct. 02, 2020. https://www.electronics-tutorials.ws/combination/digital-to-analogue-converter.html (accessed Apr. 13, 2025).

[3] Stack exchange, “Offset and scale a DAC output with opamps,” *Electrical Engineering Stack Exchange*, Apr. 24, 2020. https://electronics.stackexchange.com/questions/495393/offset-and-scale-a-dac-output-with-opamps (accessed Apr. 13, 2025).

[4] A. S. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press., 2004

[5] P. Horowitz and W. Hill, The Art of Electronics, Cambridge University Press., 2015