

Bandstop filter with post amplification

Given a noisy analog signal with amplitude 0–3 V containing information only in the 1 kHz–2 kHz band, design a circuit that conditions the signal for both downstream digital/analog systems and human operators, while filtering out unwanted frequencies, amplifying it to 1–5 V, providing indicator lights as needed, including reverse-polarity protection, and minimizing power consumption.

The noisy 0–3 V analog signal was conditioned using a combination of filtering, amplification, and protection circuits described below. Each circuit will be described more clearly throughout the project report.

A second-order Sallen–Key topology with high-pass (1 kHz) and low-pass (2 kHz) stages was used to create an effective stop-band filter with steep roll-off.

The filtered signal was amplified using a non-inverting op-amp and a DC offset was added to scale it to 1–5 V for downstream systems and human operators. A red LED was included to indicate signal strength visually.

Reverse-polarity protection was implemented using a P-channel MOSFET, which also minimized power loss compared to a diode. Component values were selected to achieve the desired frequency response and voltage scaling while maintaining low power consumption.

Filter circuit:

A second-order Sallen–Key topology was used to implement the stop-band filter, providing a steep 40 dB/decade roll-off near the cutoff frequencies. By combining separate high-pass and low-pass stages with an inverting amplifier, the circuit effectively rejects signals within the stop-band despite practical limitations of a standard RLC design.

Filter Schematic:

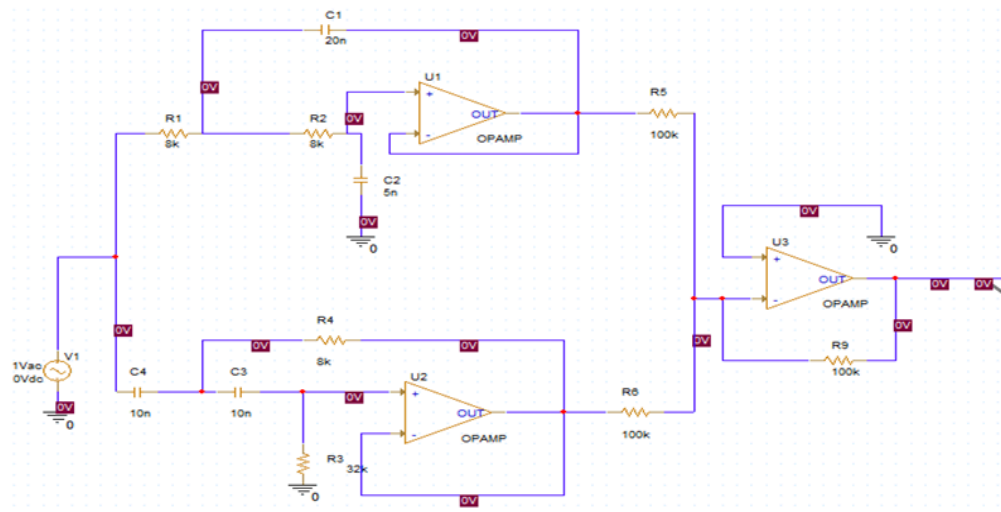


Figure 1: Image of Band stop filter circuit in Pspice

Calculations:

$f_1 = 1\text{kHz}$ -> cutoff frequency for high pass filter

$f_2 = 2\text{kHz}$ -> cutoff frequency for low pass filter

$f_0 = \sqrt{f_1 f_2} = 1.44\text{kHz}$ -> center of stop band

Consider $Q = 1$ -> for smooth edges and steeper slope in the bode diagram

R and C values will be calculated to achieve the desired quality factor (Q)

High pass filter:

$C1 = C2 = 10\text{nF}$

$$f_1 = \frac{1}{2\pi RC} = 1\text{kHz}$$

$$R = \frac{1}{2\pi f C} = \frac{1}{2\pi 1000 * 10 * 10^{-9}} = 15.9\text{k}\Omega$$

$R1 = 15.9/2 = 8\text{ k}\Omega$ and $R2 = 15.9*2 = 32\text{ k}\Omega$

Low pass filter:

$$f_2 = \frac{1}{2\pi RC} = 2\text{kHz}$$

$C = 10\text{nF}$

$$R = \frac{1}{2\pi f C} = \frac{1}{2\pi 2000 * 10 * 10^{-9}} = 7.95\text{k}\Omega = R3 = R4$$

$C3 = 10\text{nf} * 2 = 20\text{nf}$

$C4 = 10\text{nf} / 2 = 5\text{nf}$

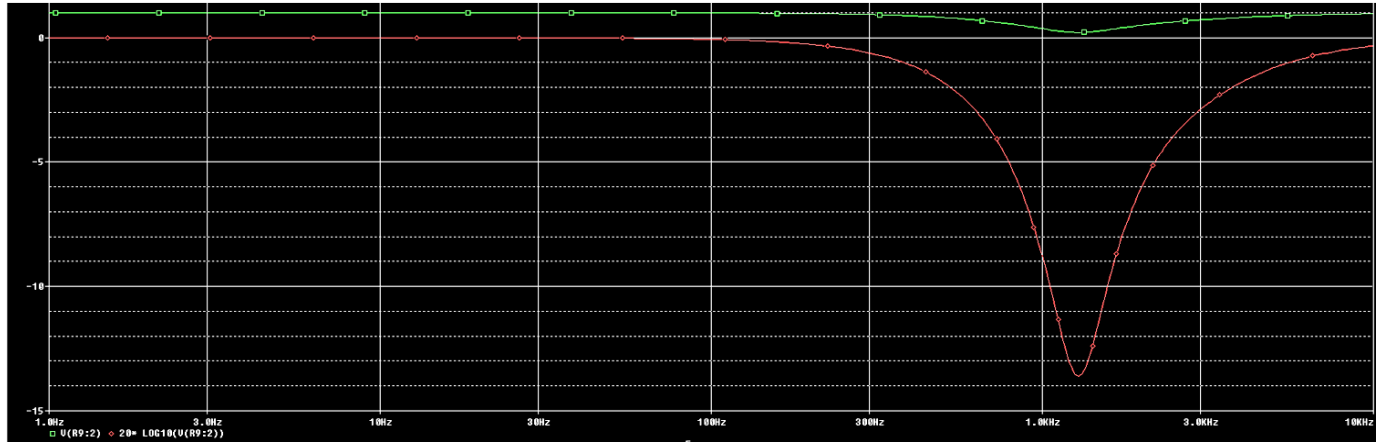
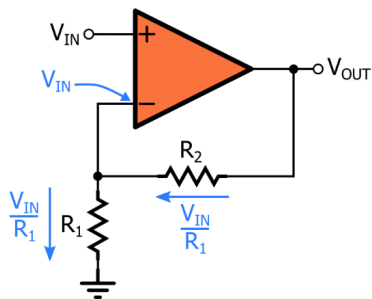


Figure 2: Filtered signals from band stop filter (x axis f , y axis dB)

Amplification and offset circuit:

Amplification Circuit: Non Inverting Op amp Voltage Amplifier



Assuming a DC offset of 1 then output voltage from the filter will be multiplied by 4/3.
Using the Gain formula for the circuit above:

$$\frac{V_{out}}{V_s} = 1 + \frac{R_f}{R_1}$$

$$\frac{V_{out}}{V_s} = \frac{4}{3}$$

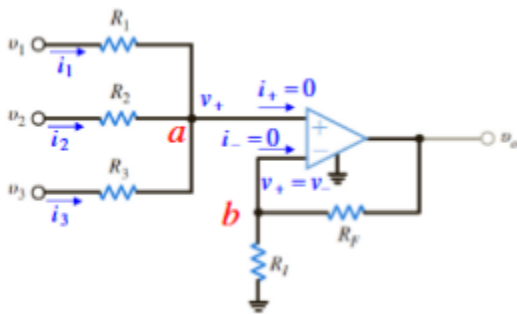
$$\frac{R_f}{R_1} = \frac{4}{3} - 1 = \frac{1}{3}$$

Use standard value resistor values:

$$R_f = 10k\Omega \text{ and } R_1 = 30k\Omega$$

Circuit implementing DC offset:

Circuit: Non inverting Summing Amplifier



Instead of 3 input voltages we will use only 2: one with which is 1V DC and the other which is the output from the amplifier circuit in Part 1

Adjust V_{out} formula for 2 voltage inputs:

$$R_1 = R_2$$

$$V_{out} = 1 + \frac{R_f}{R_1} * \frac{1}{2} (v_1 + v_2)$$

$$R_f = R_i$$

$$V_{out} = v_1 + v_2$$

$$R_f = R_i = R_1 = R_2 = 10\Omega$$

Amplifier and level shifting circuit schematic:

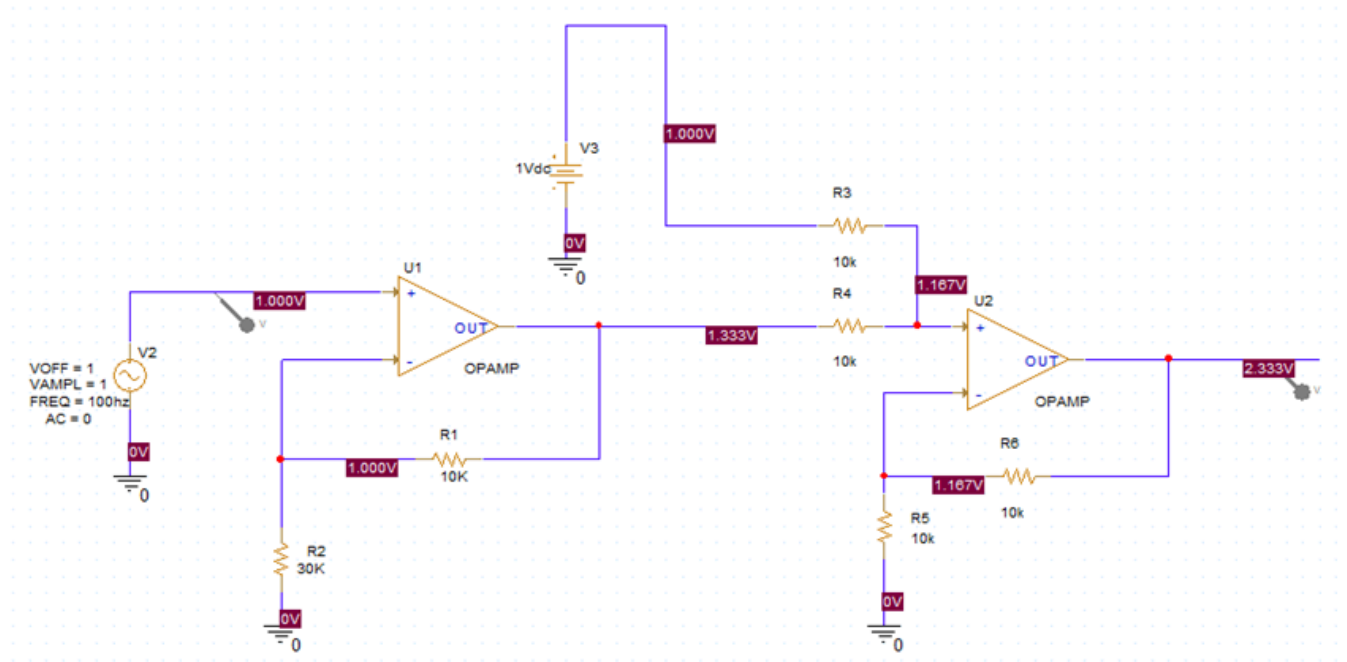


Figure 3: Amplifier and level shifting circuits connected in series

Simulation:

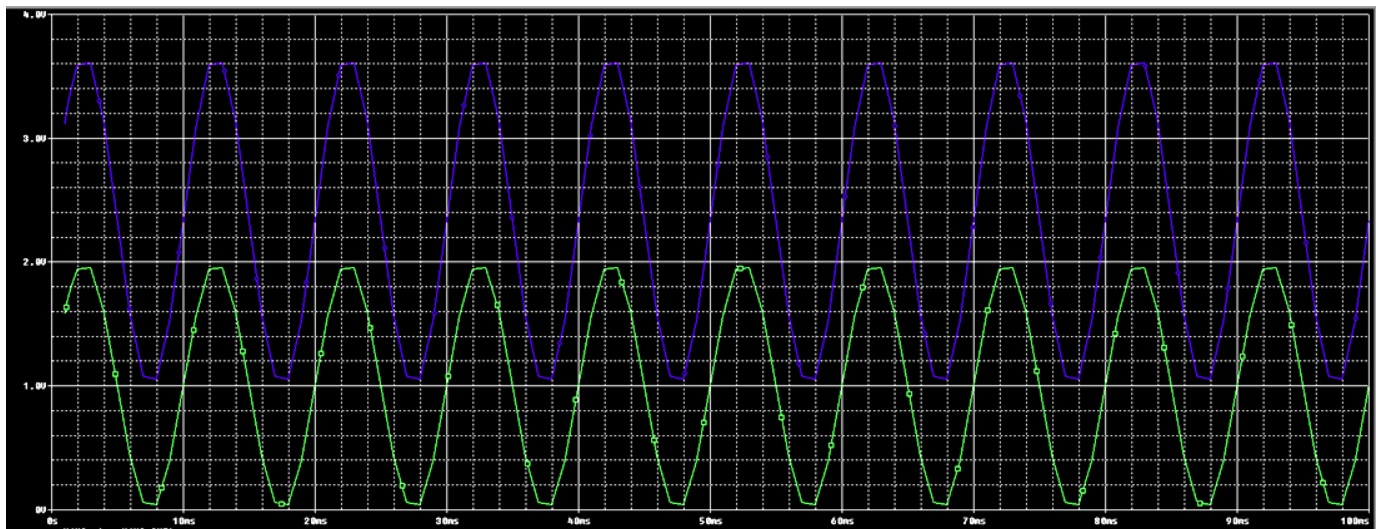


Figure 3: Image of measured values - Green (input signal), Blue (shifted and amplified output)

LED indicator

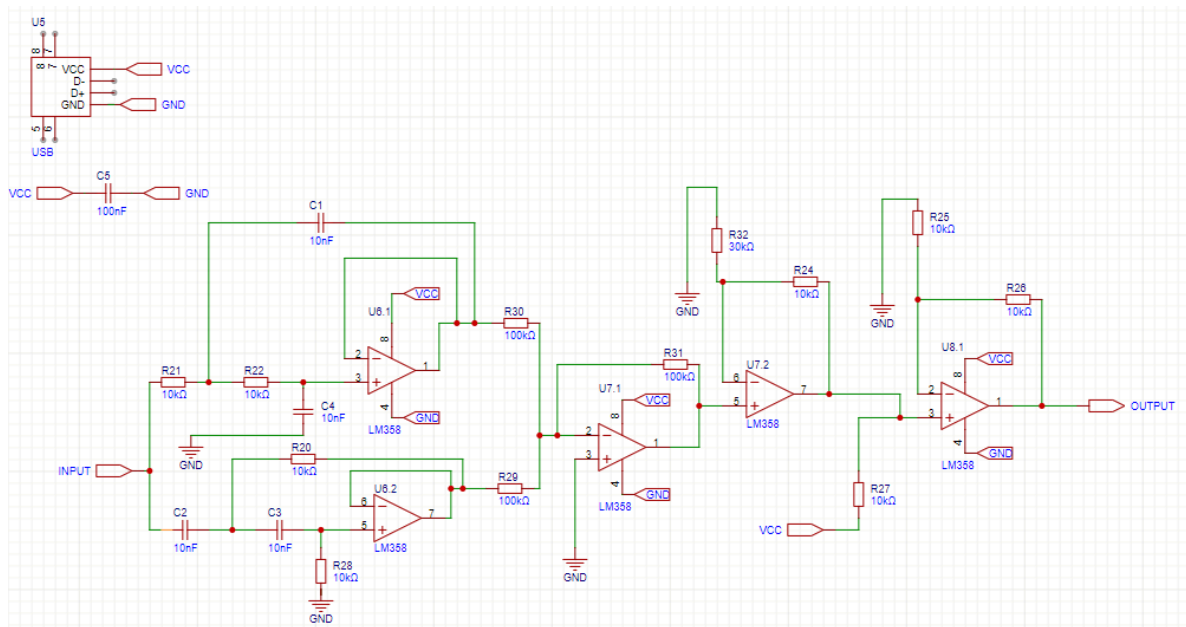


Figure 6: Image of Bandpass and level shifter circuit schematic in EasyEDA

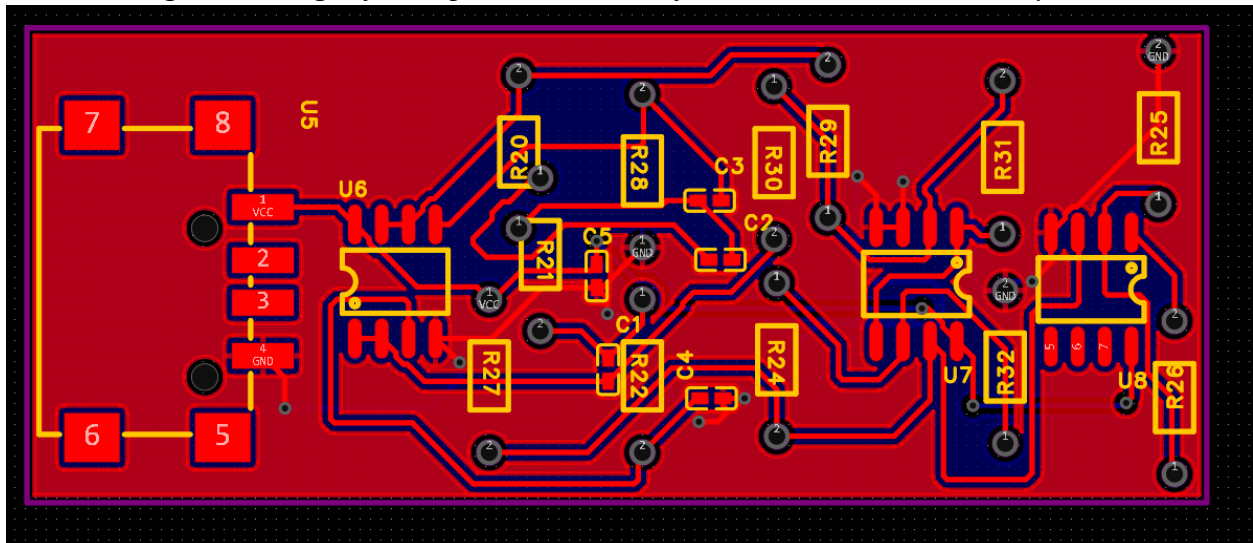


Figure 7: Screenshot of PCB design in EasyEDA

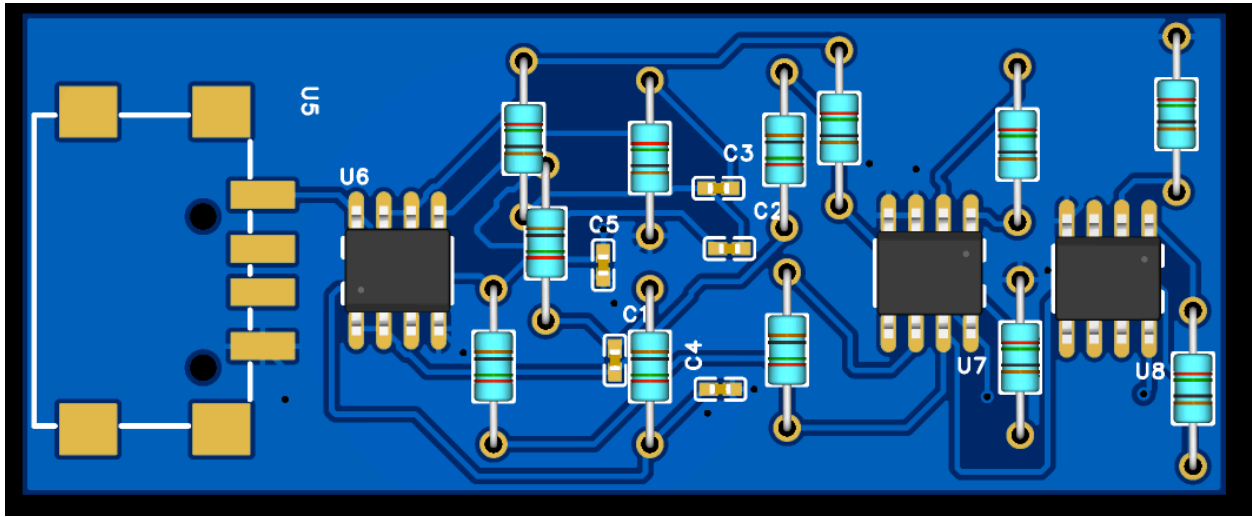


Figure 8: 3D board preview