Buck Converter Report

Design and produce a complete schematic that can reliably step down a nominal 12V input to a stable 5V output at about 1A. Apply principles of switching regulation, and explore linear regulation or any other method of your choice.

A linear regulator drops the voltage by dissipating the excess energy as heat. It's a very inexpensive solution and only requires a few capacitors. However, this is very inefficient, as it wastes a significant amount of heat. At high input voltages, they can overheat and shut down unless a heatsink is used. We are given a 12V to 5V drop (7V drop) at 1A.

$$P = (V_{drop})(I) = (7V)(1A) = 7W.$$

Furthermore, the linear regulator would need to dissipate 7W of heat. This is a lot of power for a regular to handle and would probably shut down.

As engineers, we should make something that is as optimized as possible, and a better option is a buck converter (step-down converter). They use a high-frequency switch with an inductor to lower the voltage. It is much more efficient and is a better option for a battery-powered electronic device. Although they are more expensive and complex, this is the best design decision to optimize performance and integrity.

A straightforward explanation of a buck converter is that it turns a higher DC voltage into a lower DC voltage by quickly switching the input on and off. This is basically smoothed out by the inductor and a capacitor.

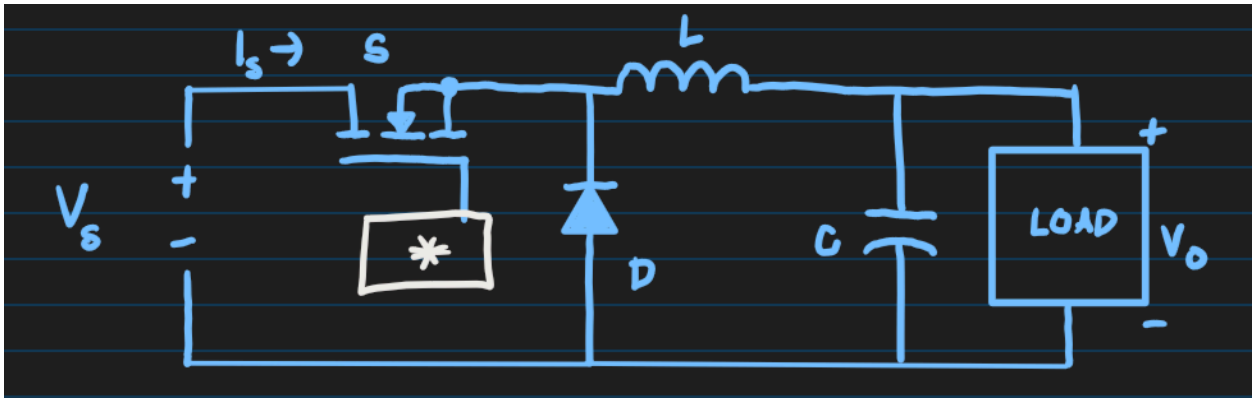

Figure 1: Image of circuit diagram of Buck Converter

1. **Switch ON or the N-MOSFET is closed:**

Vin (12 V) is applied across the inductor, and the inductor current ramps up linearly.

$$V = L\frac{di}{dt}$$

Now this current split's up and goes two places at once. One is into the load resistor and one into the capacitor. If there is extra current available, the capacitor charges up. Note that Vout ≈ $V_{CAPCATOR}$ or V_C.

2. **Switch OFF or the N-MOSFET open:**

Now the inductor is charged a bit when the switch is on, and now with the switch off, the inductor discharges that current. The inductor's magnetic field collapses and forces current to keep flowing, now through the diode into the load + capacitor. The inductor voltage reverses polarity, so its current ramps down. The capacitor still smooths the voltage, so Vout stays near 5 V.

3. **The average effect (Switch ON and Switch OFF fast with a specific time interval):**

The switch keeps repeating ON/OFF very fast, and the inductor current is a triangle wave (up when ON, down when OFF). The capacitor smooths this triangle into a nearly flat DC voltage.

$$V_{OUT} \approx D \cdot V_{IN}$$

The main components of the buck converter are the following:

- N-MOS (turns on and off at a fixed switching frequency)
- Inductor (stores/releases energy and forces current to change gradually)
- Diode (conducts when S1 is off, so inductor current keeps flowing (in synchronous bucks, this is a MOSFET).
- Capacitor (smooths the output voltage)
- R_L (what you're powering)

Now, to make the circuits, I need to do the following:

1.0 Find what information I have and assume

- Input voltage: V_{IN} = 12V
- Output voltage: V_{OUT} = 5V
- Output current: I_{OUT} = 1A
- Forward voltage rectifier diode: V_D = 0.4V [assuming]
- Switching frequency = 500 kHz (How fast the high-side switch turns on/off each cycle)
- Max. Bandwidth control loop Crossover Frequency: f_C = 10kHz (how fast the buck converter can respond to changes like load steps. Normally it should be set about 1/10–1/20 of the switching frequency so it reacts fast but stays stable) [assuming]

- Ripple current factor: r = 0.35 (Designers often pick r around 0.2–0.4. It's another way to choose how bouncy you allow the inductor current to be relative to load current) [assuming]

2.0 Find inductor value

1. Duty Cycle (D):

$$D = \frac{V_{out}+V_D}{V_{in}+V_D} = \frac{5+0.4}{12+0.4} = 0.435$$

2. Inductor Value (L):

$$L = \frac{(V_{out}+V_D)(1-D)}{r \cdot I_{out} \cdot f_{sw}} = \frac{(5+0.4)(1-0.435)}{(0.35)(1\,A)(500\,kHz)} = 1.74 \times 10^{-5}\,H = 17.4\,\mu H$$

3. Ripple Current (ΔI):

$$\Delta I = \frac{(V_{in}-V_{out})(D)}{L \cdot f_{sw}} = \frac{(12-5)(0.435)}{17.4\,\mu H \cdot 500\,kHz} = 0.358\,A$$

The above equation is just to find the ripple current. ΔI determines the minimum peak current stress.

3.0 Find Capacitor Value and Capacitor Design Requirements

The capacitor design must ensure that the output voltage remains stable under both steady-state switching conditions and transient load changes. To do this, the capacitor must satisfy two key requirements:

1. **Maximum Permissible Ripple**
    a. **Capacitance Ripple**
    b. **ESR (equivalent series resistance) Ripple Equation**
2. **Maximum Permissible Voltage Droop**

3.1 Setting the Target Ripple and Droop

The first step in the design process is to define allowable limits for ripple and droop. These are usually set as a percentage of the output voltage.

- Voltage ripple target - Max ripple allowed by the capacitor. A common rule of thumb is 1% of Vout.

$$V_{ripple,max} = 0.01 \cdot V_{out}$$

$$V_{ripple,max} = 0.01 \cdot 5V = 50\,mV$$

- Voltage droop target - Voltage droop is how much the output voltage can safely fall during a sudden load step (when current suddenly changes up or down) while the capacitor buys time to catch up and bring it back to normal V_{OUT}. For transient load steps, many designs allow 3–5% of Vout. Here,

$$V_{droop,max} = 0.03 \cdot V_{out}$$

$$V_{droop,max} = 0.03 \cdot 5V = 150\,mV$$

Now, another common design practice is to split the ripple budget evenly between capacitive ripple and ESR ripple:

- 25 mV allocated to the capacitor value
- 25 mV allocated to ESR

This ensures both ripple sources are controlled. This way, both the capacitor value and its ESR are controlled. With the inductor ripple current, switching frequency, and step current given, we can calculate:

Voltage ripple

$$\Delta V_{C,pp} \approx \frac{\Delta I_L}{8 f_{sw} C_{out}}$$

Where:

- ΔI_L = ripple current through the inductor
- f_{sw} = switching frequency
- C_{out} = output capacitance

It must be verified mathematically that the AC through the output capacitor remains below the maximum ripple current specified above. The following equation describes the relationship between the output capacitance and the ripple voltage for a buck converter topology (assumption: ideal capacitor):

$$\Delta V_{C,out} = \frac{\Delta I}{8 \cdot C_{out} \cdot f_{sw}} = 25\,mV$$

(took from the half split voltage ripple mentioned above)

The next equation is used to calculate the minimum capacitance required for the given capacitance-dependent ripple:

$$C_{out} > \frac{\Delta I}{8 \cdot f_{sw} \cdot \Delta V_{C,out}}$$

$$C_{out} > \frac{0.36}{8 \cdot 500k \cdot 25mV} = 3.5\,\mu F$$

ESR Ripple Equation

The next equation describes the relationship between the ESR (equivalent series resistance) of the output capacitor and the ripple voltage for a buck converter.

$$\Delta V_{ESR,C,out} = \Delta I \cdot ESR_{C,out}$$

$$ESR_{C,out} < \frac{\Delta V_{ESR,C,out}}{\Delta I} = \frac{25\,mV}{0.36\,A} \approx 69.4\,m\Omega$$

Used to calculate the maximum allowable ESR of the output capacitor based on the given ESR-dependent ripple voltage. Therefore, we have to choose a capacitor that is lower $69.4\,m\Omega$ so that the ESR doesn't add significant ripple on top of the capacitive ripple.

Maximum permissible voltage droop during a load step

This equation is used to calculate the minimum output capacitance to maintain a given maximum voltage droop during a load step:

$$V_{droop} = \frac{I_{step}}{2\pi f_c C_{out}}$$

Rearranging for Cout:

$$C_{out} > \frac{I_{step}}{2\pi f_c V_{droop}}$$

With updated values:

- $V_{droop} = 3\% \cdot 5V = 0.15V = 150\,mV$
- $I_{step} = 0.5\,A$
- $f_c = 10\,kHz$

$$C_{out} > \frac{0.5}{2\pi \cdot 10{,}000 \cdot 0.15} \approx 53.05\,\mu F$$

Because the load step requirement dominates voltage ripple capacitance ($53.05\,\mu F > 3.5\,\mu F$. The maximum allowable voltage change during load transients requires that $C_{out} \geq 53\,\mu F$. The minimum required capacitance was 53 µF, so a 100 µF polymer capacitor was chosen to improve extra stability.

4.0 Selecting Parts

1. Inductor (SD7030-180-R)
    a. I = $17.3\,\mu H$ - matches calculated inductance.
    b. Current Rating (Amps) = 1.7A rated - covers 1A peak load with some margin.
2. Capacitor (GRM32ER61A107ME20L)
    a. C = 100 µF
    b. ESR in the milliohm range and therefore $\ll$ 69 mΩ (meets ripple budget)
    c. V = 10V - A higher voltage rating means more effective capacitance. This is because of DC bias derating more as the applied voltage gets closer to the capacitor's rated voltage. Therefore, the higher voltage rating would be the best.
3. N Channel MOSFET (AO3400A)
    a. VDS = 30V - Good for 12V systems.
    b. Continuous Drain = 5.7A
    c. RDS(on) = 26.5m = To be expected, also not too high
    d. Vgs = 4.5 V and Vgs (Max) = ±12V therefore to turn on the mosfet it should be around 5V
4. Diode (SS34)
    a. $V_{Reverse}$ = 40 V - Good for 12 V input.
    b. I = 3 A - perfect for approx 1
    c. $V_{FORWARD} \approx 0.5$ V @ 3 A, which is not bad because I estimated 0.4V
    d. Speed/Type: Schottky = fast, ideal for 500 kHz.
5. Resistor (PWR163S-25-5R00JE)
    a. $R_1 = \frac{V_{OUT}}{I_{OUT}} = \frac{5V}{1A} = 5\Omega$
    b. Most resistors can't withstand 5W of power; we need a different type of resistor and a high power rating with a proper heatsink.

Simulating Buck Converter

Now we need to create the PWM for the N-MOS switch. We know the following:

- Duty cycle: $D \approx 0.435$
- Switching frequency: $f_{sw} = 500\,kHz$ and $T_s = \frac{1}{f_{sw}} = 2\,\mu s$
- On-time: $T_{on} = D \cdot T_s = 0.435 \times 2\,\mu s \approx 0.87\,\mu s$
- Off-time: $T_{off} = (1 - D) \cdot T_s = 1.13\,\mu s$
- Amplitude = 5V

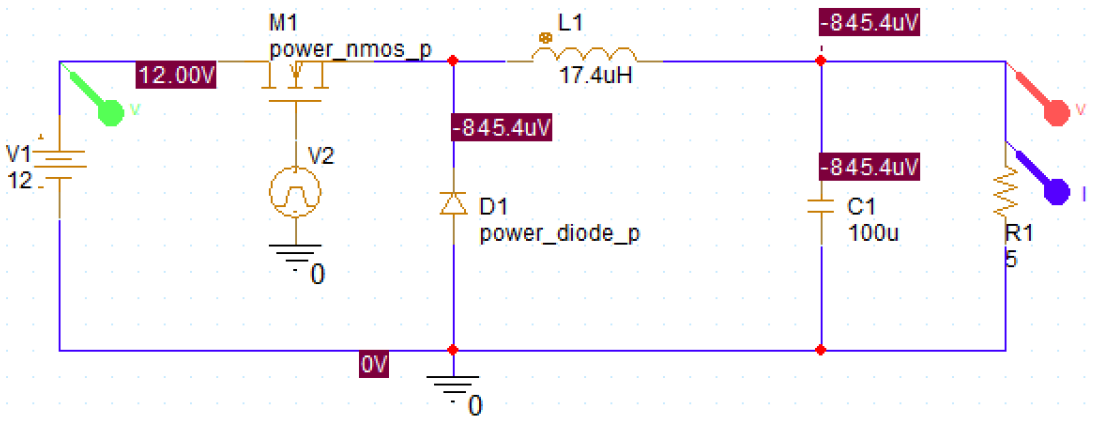

Figure 2: Image of Buck Converter circuit in Pspice

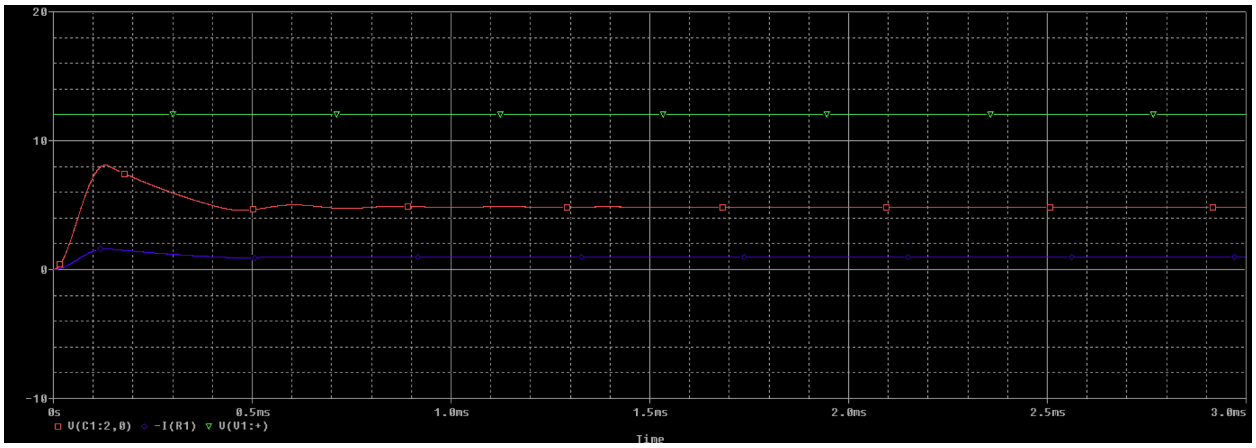

Figure 3: Image of measured values - Green (V_{IN}=12V), Red(V_{OUT} ≈ 5) and Blue (I_O = 1A)

As you can see, our output is really close to what we want with a Vout ≈ of 5 and Iout ≈ 1A. However, there is an overshoot at the start of the Vout. This is because the inductor dumps a lot of energy very quickly, and the capacitor has very low ESR. The circuit acts like a spring that overshoots up to 7 V and then oscillates before settling down to 5 V.

To fix this, I added a 1 Ω resistor in series with the capacitor to add damping. That makes the overshoot smaller and the voltage settles to 5 V faster.

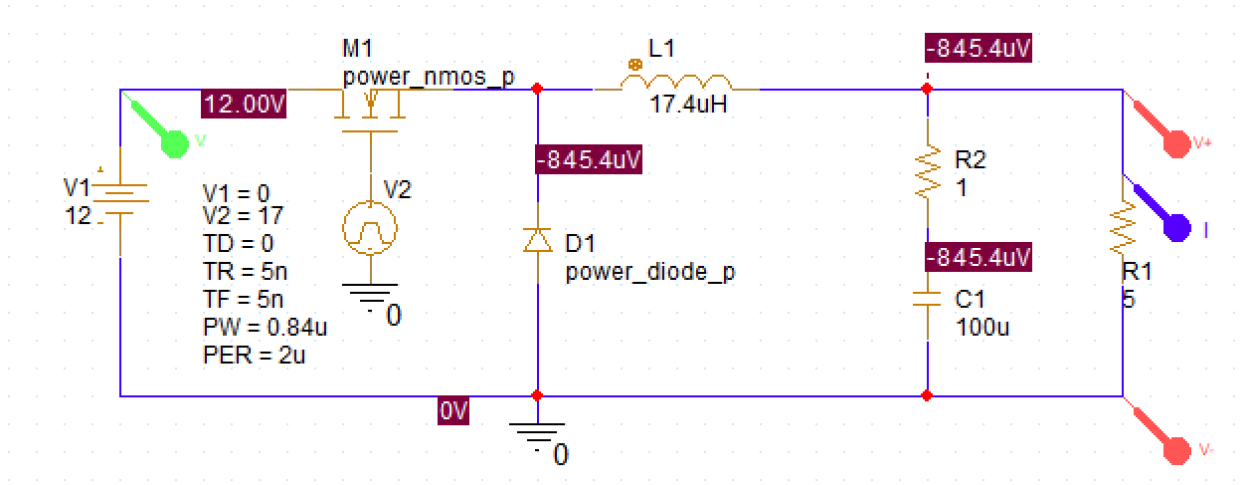

Figure 4: Image of Buck Converter circuit in Pspice (added R2)

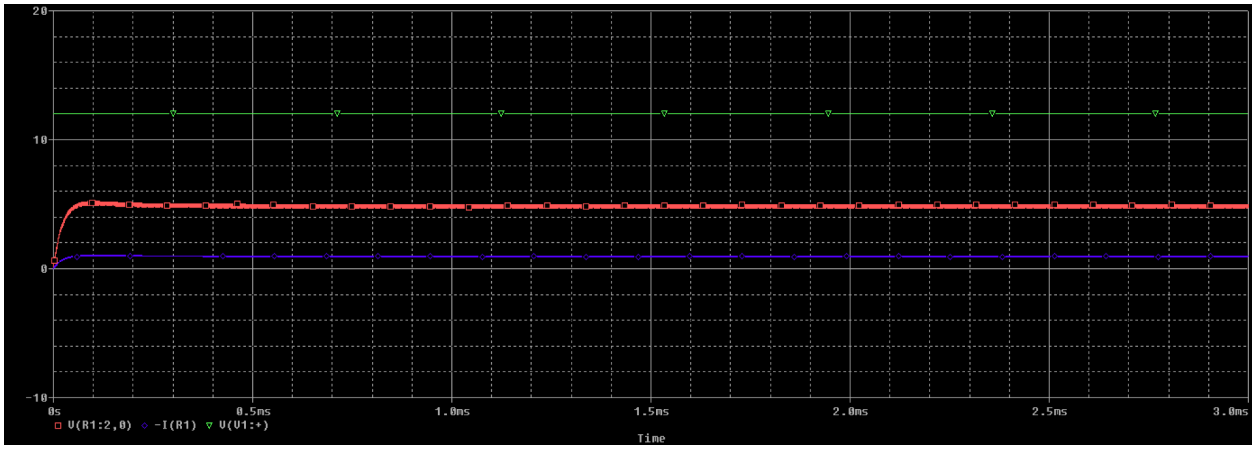

Figure 5: Image of new measured values - Green (V_{IN}=12V), Red($V_{OUT} \approx 5$) and Blue (I_O = 1A)

4.2. PCB Design

Now, with all the parts mentioned in 4.0, I was able to make the PCB in EasyEDA

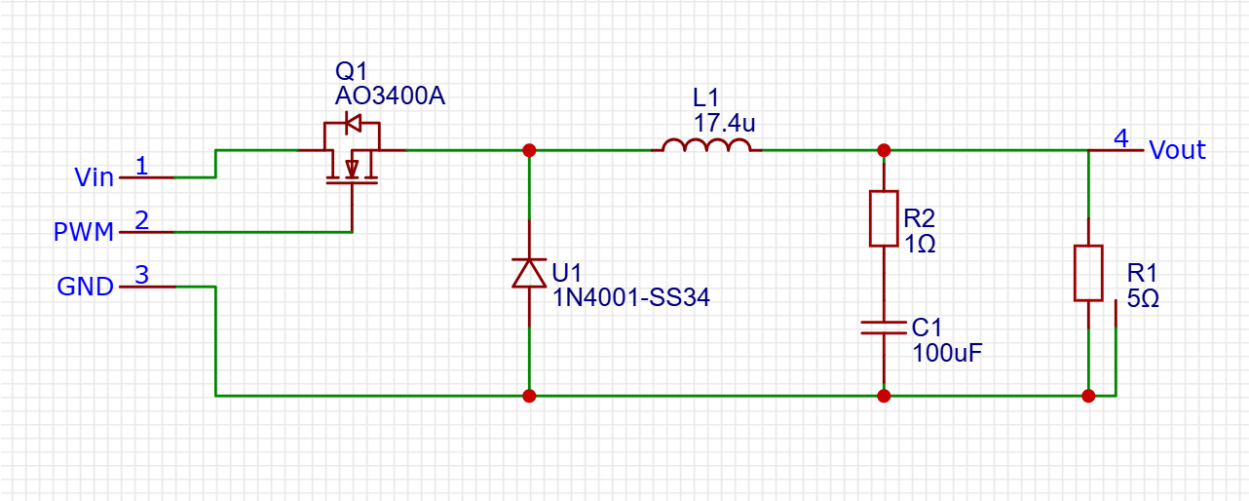

Figure 6: Image of Buck Converter circuit schematic in EasyEDA

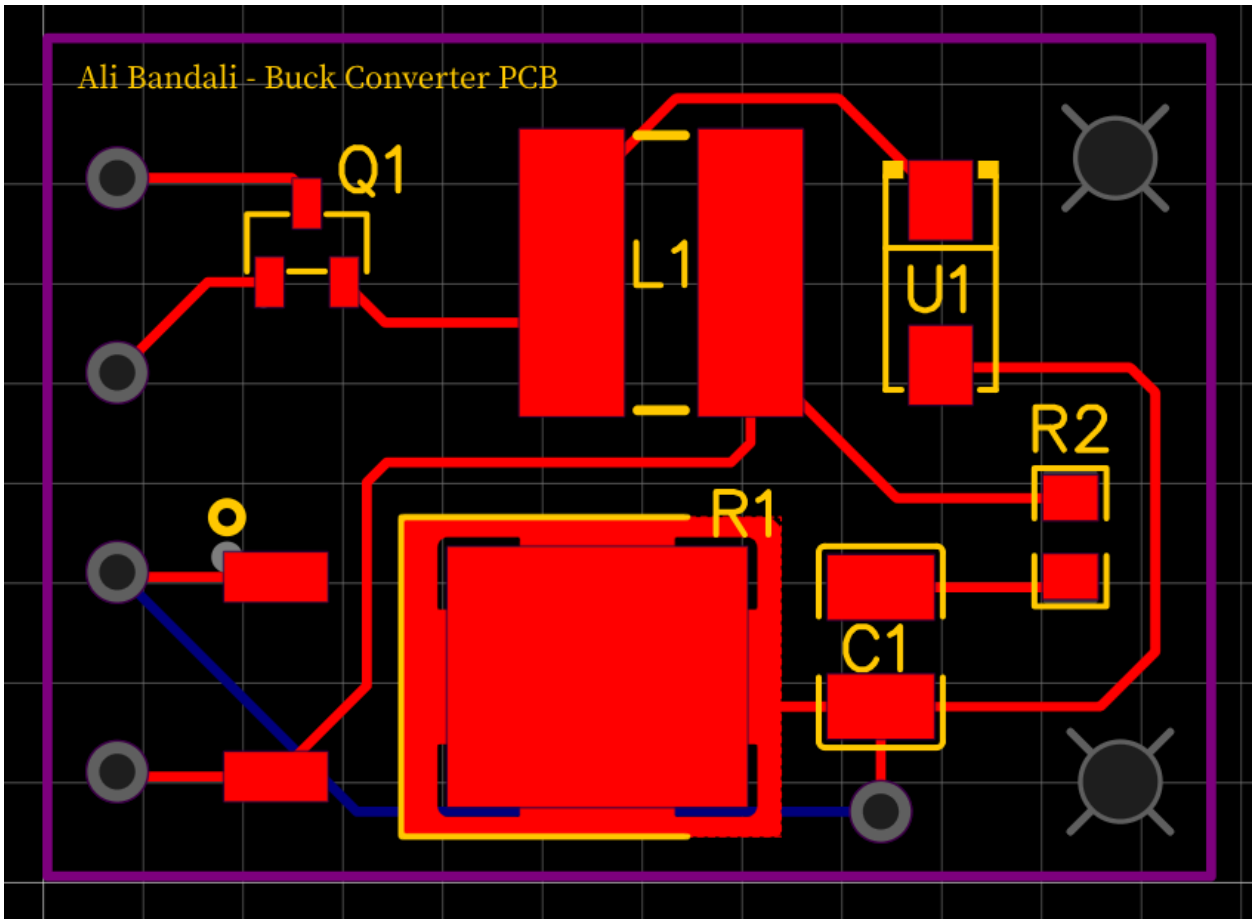

Figure 7: Screenshot of PCB design in EasyEDA
(added holes on the right side to implement screws)