Computer System Overview

1.1 Basic Elements

a) What are the two main categories of processor registers? What are they used for?

1.2 EVOLUTION OF THE MICROPROCESSOR

True or False:

a) GPUs are used for dealing with streaming signals such as audio or video
b) SoC is a microchip with all the necessary system components on it.

1.3 INSTRUCTION EXECUTION

a) What are the four distinct actions that a machine instruction can specify?

b) Suppose the hypothetical processor of Figure 1.3 also has two I/O instructions:
0011 = Load AC from I/O
0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular external device. Show the program execution (using the format of Figure 1.4) for the following program:

a. Load AC from device 5.
b. Add contents of memory location 940.
c. Store AC to device 6.

Assume that the program counter started with 300, the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

1.4 INTERRUPTS

True or False:

a) Program interrupts are used to signal the normal completion of an operation or to signal a variety of error conditions.

Answer the following questions:

b) Interrupt process involves overhead (in interrupt handling), Nevertheless, the processor can be employed much more efficiently with the use of interrupts. Explain.
c) Explain, by example, handling the multiple interrupts via a priority scheme, and mention its advantages over the disabling-interrupts scheme.

1.5 THE MEMORY HIERARCHY

a) Why are there different kinds of memory hierarchies?
   What are the characteristics distinguishing them?
b) Explain the term "locality of reference".
c) Consider the following code:

```
for (i = 0; i < 20; i++)
    for (j = 0; j < 20; j++)
        a[i] = a[i] * j
```

1. Give one example of the spatial locality in the code.
2. Give one example of the temporal locality in the code.

1.6 CACHE MEMORY

a) Consider a memory system with cache having the following parameters:

   Sc = 32 KB Cc = 0.1 cents/bytes TC = 10 ns
   Sm = 256 MB Cm = 0.0001 cents/bytes Tm = 100 ns

   1. What was the total cost prior to the addition of the cache?
   2. What is the total cost after the addition of the cache?
   3. What is the percentage decrease in time due to the inclusion of cache with respect to a system without cache memory considering a cache hit ratio of 0.85

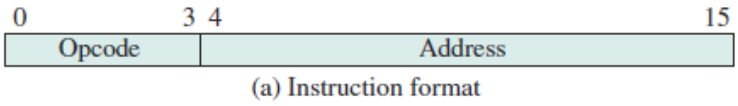
b) Suppose that a large file is being accessed by a computer memory system comprising of a cache and a main memory. The cache access time is 60 ns. The time to access main memory (including cache access) is 300 ns. The file can be opened either in read or in write mode. A write operation involves accessing both the main memory and the cache (write-through cache). A read operation accesses either only the cache or both the cache and main memory depending upon whether the access word is found in the cache or not. It is estimated that read operations comprise 80% of all operations. If the cache hit ratio for read operations is 0.9, what is the average access time of this system?

1.7 DIRECT MEMORY ACCESS

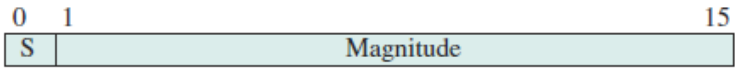
a) A computer consists of a CPU and an I/O device D connected to main memory M via a shared bus with a data bus width of one word. The CPU can execute a maximum of 10^6 instructions per second. An average instruction requires five processor cycles, three of which use the memory bus. A memory read or write operation uses one processor cycle. Suppose that the CPU is continuously executing "background" programs that require 95% of its instruction execution rate but not any I/O instructions. Assume that one processor cycle equals one bus cycle. Now suppose that very large blocks of data are to be transferred between M and D.
    1. If programmed I/O is used and each one-word I/O transfer requires the CPU to execute two instructions, estimate the maximum I/O data transfer rate, in words per second, possible through D.
    2. Estimate the same rate if DMA transfer is used.

1.8 MULTIPROCESSOR AND MULTICORE ORGANIZATION

a) What are the advantages of An SMP organization over a uniprocessor organization?
b) What is a chip multiprocessor? What is the motivation for its development?



(a) Instruction format



(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

0011 = Load AC from I/O
0111 = Store AC to I/O

(d) Partial list of opcodes

Figure 1.3 Characteristics of a Hypothetical Machine

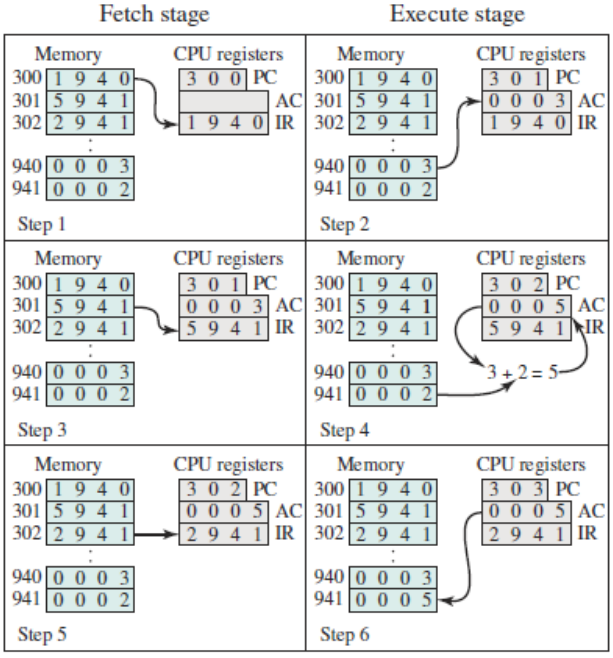


Figure 1.4 Example of Program Execution (contents of memory and registers in hexadecimal)