DATE: / /

SUBJECT:

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1.1 BASIC ELEMENTS

a- Processor registers have 2 main categories:

1- Memory address register (MAR) used to store the address of the next write or read

2- Memory buffer register (MBR) used to store the data to be read or written to memory.

1.2 Evolution ~~of~~ THE MICROPROCESSOR

a- False (DSPs) b- True

1.3 INSTRUCTION EXECUTION

a- 1- T~~F~~ransfer data between processor and memory

2- Transfer data between processor and I/o device

3- Data Processing

4- Control or alter the sequence of execution

b- suppose the address of device 5 = 123 H

and ~ ~ ~ ~ 6 = 456 H

	Fetch	Execute
1	PC : 300 AC : IR : 3123	PC : 301 AC : 3 IR : 3123
2	PC : 301 AC : 3 IR : 5940	PC : 302 AC : 5 IR : 5940
3	PC : 302 AC : 5 IR : 7456	PC : 303 AC : 5 → 456 5 IR : 7456

1.4 INTERRUPTS

a- False

b- It's obvious that there is some overhead involved in the process. This because extra instructions in the ISR need to be executed to determine the nature of the interrupt and to decide the appropriate action. Nonetheless, because of ~~the~~ a large amount of the Processor's time would be wasted waiting for the I/o device to finish the execution, using interrupts is much more efficient.

c- In the priority scheme approach, Priorities are assigned to the interrupts. A higher priority interrupt will cause a lower priority interrupt handler to be interrupted. For example, a printer and a disk ~~are~~ with priorities 2 and 5 respectively. During the execution of the user program, the printer issued an interrupt. The current status of the user Program will be saved onto stack and the ISR of the printer will be executed. During this ISR, the disk issued an interrupt. Since it has higher priority, the current status of the printer ISR will be saved onto the control stack and the control is transferred to the disk ISR. when it's finished, the control will be transferred back to the printer ISR, the ISR is over then to the user Program again. The advantage of this approach is that it takes into account the priorities and time-critical needs.

1.5 MEMORY HIERARCHY

a- Because each type of memory has its own adWantages and limitations. The designer would like to use memory technologies that Provide for large-capacity memory which in turn has slow access time. But, he also wants to meet Performance requirements. This forces him to use expensive lower capacity memories that have fast access time. To solve this dilemma, a memory hierarchy was employed. The hierarchy is divided into 5 levels, each level is characterized by a number of factors.

Registers → Cache → main memory → Secondary memory → magnetic tape

Fastest, most expensive, lowest capacity → Slowest, cheapest, highst capacity.

b- A Computer Program tends to access data and instructions that are Placed near each other in memory. In many Computer programs, an instructions needs to be executed so many times in a short period, as in the Case of loops, and nearby instructions are to be accessed afterwards. once a loop is entered, there are repeated references to a set of instructions in a short Period.

C- As an example of temporal locality is accessing and modifying the array elements many times in a short period in the inner loop.

As an example of spatial lacality is accessing the array itself repeatedly within the outer loop.

1.6 CACHE MEMORY

b- $P_{read} = ,8$ ∴ $P_{write} = 1 - ,8 = ,2$, $T_{m+C} = 300ns$

$P_{hit} = ,9$ ∴ $P_{miss} = 1 - ,9 = ,1$, $T_C = 60ns$

$T = P_{write} \times T_{m+C} + P_{read} \left(P_{hit} \times T_C + P_{miss} \times T_{m+C} \right)$

$= ,2 \times 300ns + ,8 (,9 \times 60ns + ,1 \times 300ns)$

$= 127,2\ ns$ (closer to the access time of the faster memory))

a- 1) $S_m = 256 \times 1024 \times 1024$

Cost $= S_m \times ,0001 = 26,84 \times 10^3$ cents

2) total cost $=$ Cost $+ S_c \times 1024 \times ,1$

$= 26,84 \times 10^3 + 32 \times 1024 \times ,1$

$= 30,12 \times 10^3$ cents

3) time before adding cache $= 100ns$

time after adding cache $= ,85 \times 10 + ,15 \times 110 = 25ns$

∴ % decrease in time $= \frac{100 - 25}{100} \times 100 = 75\ \%$

1.8 MULTIPROCESSOR AND MULTICORE

a- 1. Higher Performance: due to multi processors working in Parrallel

2. Reliability: The failure of one processor will degrade the performance but won't drive the entire system to fail.

3- Incremental growth: Performance can be enhanced by adding an additional processor.

4- scaling : a wide range of products with different prices are offered by vendors depending on the number of processors

b - A Chip ~~micro~~ multiprocessor combines two or more processors (called cores) on a single silicon chip. Each core has its own set of components of that of an independent processor. like registers and caches.

The motivation for this development raised when designers came up against practical limits in the ability to achieve greater performance by means of more complex processors. The best way to improve performance was to put multiple processors and cache memory on a single chip.