Politecnico di Torino

Integrated Systems Architecture

Lab 2

Digital arithmetic

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1 Digital arithmetic and logic synthesizers

1.1 Introduction

In this lab session, we are going to do floating point multiplication. To achieve the aims of this lab, we start with implementing the multiplication using the design ware components that can be used as CSA or PPARCH, then by R8-MBE (Radix 8 Modified Booth's Encoder) and implement Dadda-like adder plane we can obtain a faster multiplier. Dadda tree uses a selection of full and half adders to sum the partial products in stages until two numbers are left. The design is similar to the Wallace multiplier, but the different reduction tree reduces the required number of gates and makes it slightly faster (for all operand sizes).

The IEEE 754 standard specifies a binary32 as having:

Sign bit: 1 bit

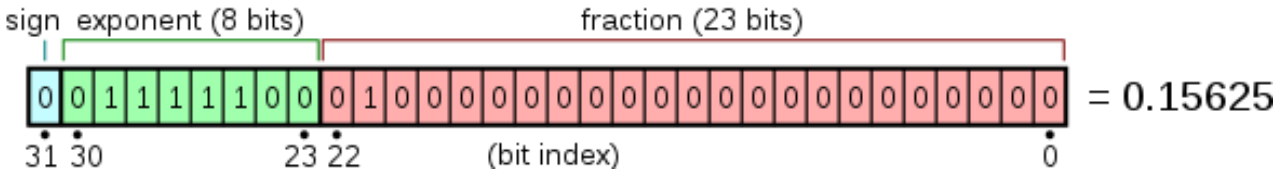
Exponent width: 8 bits

Significant precision: 23 bits

This gives from 6 to 9 significant decimal digits precision. If a decimal string with at most 6 significant digits is converted to the IEEE 754 single-precision format, giving a normal number, and then converted back to a decimal string with the same number of digits, the final result should match the original string. If an IEEE 754 single-precision number is converted to a decimal string with at least 9 significant digits, and then converted back to single-precision representation, the final result must match the original number.

The sign bit determines the sign of the number, which is the sign of the significant as well. The exponent is an 8-bit unsigned integer from 0 to 255, in the biased form: an exponent value of 127 represents the actual zero. Exponents range from −126 to +127 because exponents of −127 (all 0s) and +128 (all 1s) are reserved for special numbers.

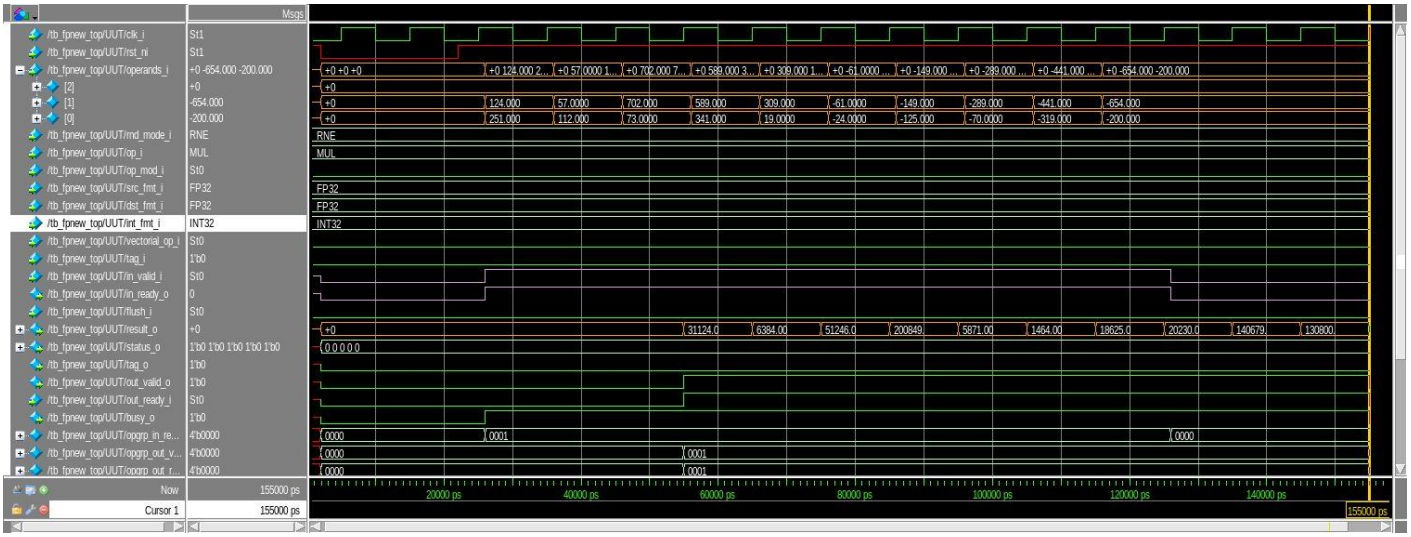
The true significand includes 23 fraction bits to the right of the binary point and an implicit leading bit (to the left of the binary point) with value 1, unless the exponent is stored with all zeros. Thus only 23 fraction bits of the significant appear in the memory format, but the total precision is 24 bits (equivalent to log10(224) ≈ 7.225 decimal digits). The bits are laid out as follows:



Simulations and Logic Synthesis

2 . Synthesis Strategies

Simulation and verification of the test bench:



ctvalA	sign	Exponent	Mantissa	Mantissa bits	zeros bits	ctvalB	sign	Exponent	Mantissa	Mantissa bits	zeros bits	multiplication
251	0	134	123	7	16	124	0	133	15	4	19	31124
112	0	133	3	2	21	57	0	132	25	5	18	6384
73	0	133	9	6	17	702	0	136	95	8	15	51246
341	0	135	85	8	15	589	0	136	77	9	14	200849
19	0	131	3	4	19	309	0	135	53	8	15	5871
-24	1	131	1	1	22	-61	1	132	29	5	18	1464
-125	1	133	61	6	17	-149	1	134	21	7	16	18625
-70	1	133	3	5	18	-289	1	135	33	8	15	20230
-319	1	135	63	8	15	-441	1	135	185	8	15	140679
-200	1	134	9	4	19	-654	1	136	71	8	15	130800

2.1 Synthesize with compile. Find the maximum frequency and the area.

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:38:42 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         3458
Number of nets:                         11321
Number of cells:                         7974
Number of combinational cells:           7606
Number of sequential cells:               297
Number of macros/black boxes:               0
Number of buf/inv:                       2081
Number of references:                      18

Combinational area:               8835.189996
Buf/Inv area:                     1335.319997
Noncombinational area:            1587.222051
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 10422.412048
Total area:                 undefined
1
```

2.2 Repeat the previous step issuing the optimize registers command after compile. Find the maximum frequency and the area. Verify the netlist behavior via simulation.

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:41:08 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         3391
Number of nets:                          9709
Number of cells:                         7675
Number of combinational cells:           6362
Number of sequential cells:               955
Number of macros/black boxes:               0
Number of buf/inv:                       1463
Number of references:                      13

Combinational area:               7483.111990
Buf/Inv area:                      851.998003
Noncombinational area:            5083.526164
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 12566.638154
Total area:                 undefined
1
```

2.3 Repeat the previous step issuing only the compile ultra command. Find the maximum frequency and the area. Verify the netlist behavior via simulation.

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:42:32 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          317
Number of nets:                          4832
Number of cells:                         4174
Number of combinational cells:           3891
Number of sequential cells:               279
Number of macros/black boxes:               0
Number of buf/inv:                        468
Number of references:                       5

Combinational area:               5176.094021
Buf/Inv area:                      262.276002
Noncombinational area:            1488.270048
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  6664.364069
Total area:                 undefined
1
```

2.4 Force Design Compiler to flatten the hierarchy and to implement the Significands multiplier (Mantissa multiplier in fpnew_fma.sv (3)) as a CSA multiplier. Find the maximum frequency and the area with the commands compile and optimize registers. Verify the netlist behavior via simulation.

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:43:47 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          675
Number of nets:                          5026
Number of cells:                         3863
Number of combinational cells:           3572
Number of sequential cells:               278
Number of macros/black boxes:               0
Number of buf/inv:                        566
Number of references:                      44

Combinational area:               5435.178046
Buf/Inv area:                      323.456002
Noncombinational area:            1483.216047
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  6918.394093
Total area:                 undefined
1


****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:44:24 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          677
Number of nets:                          5457
Number of cells:                         4310
Number of combinational cells:           3690
Number of sequential cells:               610
Number of macros/black boxes:               0
Number of buf/inv:                        681
Number of references:                      44

Combinational area:               5498.752047
Buf/Inv area:                      383.838003
Noncombinational area:            3245.732104
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  8744.484151
Total area:                 undefined
1
```

2.5 Repeat the previous step by forcing the Design Compiler to implement the Significands multiplier as a PPARCH multiplier. Find the maximum frequency and the area with the commands compile and optimize registers. Verify the netlist behavior via simulation.

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:45:29 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          774
Number of nets:                          5123
Number of cells:                         3865
Number of combinational cells:           3572
Number of sequential cells:               278
Number of macros/black boxes:               0
Number of buf/inv:                        566
Number of references:                      45

Combinational area:               5435.178046
Buf/Inv area:                      323.456002
Noncombinational area:            1483.216047
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  6918.394093
Total area:                 undefined
1

****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 16:46:08 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          778
Number of nets:                          5553
Number of cells:                         4305
Number of combinational cells:           3688
Number of sequential cells:               605
Number of macros/black boxes:               0
Number of buf/inv:                        679
Number of references:                      45

Combinational area:               5497.688047
Buf/Inv area:                      382.774003
Noncombinational area:            3219.132103
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  8716.820150
Total area:                 undefined
1
```

Results Summary:

	Slack(ns)	maximum frequency (MHz)	maximum area
compile	2.52	396.8254	10422.412048
optimize registers	1.71	584.7953	12566.638154
ultra	2.55	392.1569	6664.364069
CSA multiplier	2.37	421.9409	6918.394093
CSA multiplier (optimize registers)	1.69	591.716	8744.484151
PPARCH multiplier	2.32	431.0345	6918.394093
PPARCH multiplier (optimize registers)			8716.820150