Ali Jahanshahi

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Education

University of California Riverside, Riverside CA — Sept. 2017 - Present
PhD., Computer Science, GPA: 4/4.

University of Tehran, Tehran — Sept. 2013 - June 2016
M.Sc., Computer Architecture, GPA: 3.55/4.

Shahid Beheshti University, Tehran — Sept. 2009 - June 2013
B.Sc., Computer Engineering, GPA: 3.47/4.

Experience

Senior Hardware Engineer, — Feb. 2017 - Aug. 2017
Institute of IT security, Sharif University of Technology
Hardware Security Module (HSM) Project for Secure Inter-bank Transactions

System Administrator, — June 2012 - Sept. 2012
Department of IT, Shahid Beheshti University
University Alumni Association System Project

Skills

Languages:
C/C++
Python
Bash
Keras
TensorFlow
CUDA
Scala

Hardware Description Language:
Verilog
VHDL
CHISEL

Simulation and Synthesis:
GPGPU-Sim
Xilinx Vivado
Quartus

Projects

Adding a New CPUIdle Governor to Linux Kernel for HPC Applications, *Research Project (Ongoing)* — Summer 2019

Machine Learning Based Border Gateway Protocol (BGP) Anomaly Detection, *Data Mining Course Project* — Spring 2018
Language: *Python*, **Tool**: *MATLAB*

An LLVM pass for Path Profiling Based on Ball-Larus Method, *Compiler Construction Course Project* — Spring 2018

Tiny Modular CNN Accelerator for Embedded FPGA, *DAC 2019 System Design Contest* — Spring 2018
Language: *Python, CHISEL*, **Libraries**: *Keras, TensorFlow*, **Platform**: *PYNQ FPGA Board*

Adding Support for Resource Reservation to Linux Kernel, *Real-time Embedded Systems Course Project* — Winter 2018
Language: *C*, **Platform**: *Raspberry Pi*

GPU Accelerated Network Function Virtualization (NFV), *Research Project* — Fall 2017
Language: *CUDA*, **Library**: *DPDK*

AES-GCM Authenticated Encryption Hardware Accelerator, *HSM Project* — Winter 2017
Language: *CHISEL*

User-space API and Kernel Driver for Exposing Hardware Accelerators to Software Stack, *HSM Project* — Spring 2017
Language: *C/C++*

Graph Processing Framework for Evolutionary Dynamics of Complex Networks, *Research Project* — Spring 2016
Language: *C/C++*

High-level Synthesis Framework for Approximate Sequential Circuits, *M.Sc. Thesis* — Fall 2015
Languages: *C/C++, Linear programming*, **Tool**: *Gurobi Optimizer*

Power-&Latency-aware AMBA Bus High-level Synthesis for SoC Applications, *Research Project* — Fall 2015
Languages: *C/C++, Verilog, Linear programming*, **Tool**: *Gurobi Optimizer*

Design of a Simple MUX-Based FPGA Chip — Summer 2012
Languages: *Java, Verilog*, **Tools**: *Synopsys Design Compiler, Cadence SoC Encounter*

Honors and Awards

Ranked 1st in National Digital System Design Contest (FPGA Challenge Section) — Oct. 2013
17th International Symposium on Computer Architecture and Digital Systems (CADS)

Ranked 13rd in National Entrance Exam — Sept. 2013
For M.Sc. in Hardware Engineering among 30,000+ participants

Ranked 19th in the 18th National Scientific Olympiads in Computer Engineering — Aug. 2013
Among over 1000 selected top students, Tarbiat Modares University

Ranked 9th in the ACM-ICPC West Asia Regional Contest — Dec. 2011
Among over 100 teams, University of Tehran