

L1 Instruction Cache

L0 Instruction Cache

Warp Scheduler (32 thread/clock)

Dispatch Unit (32 thread/clock)

Register File (16,384 x 32-bit)

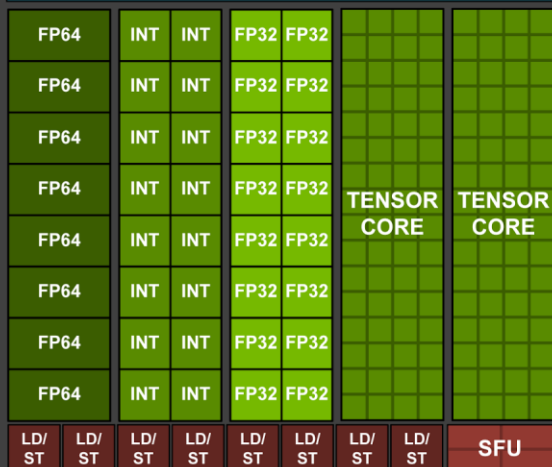


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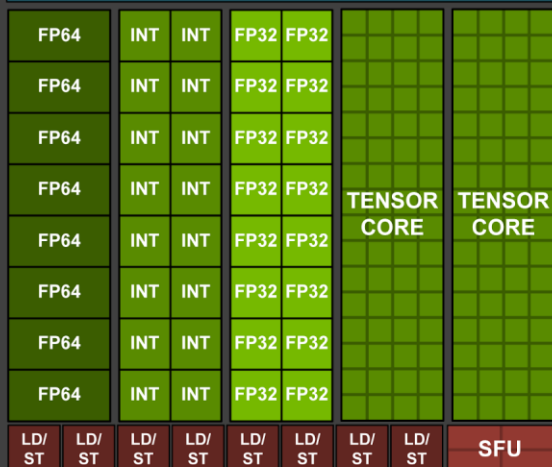


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128KB L1 Data Cache / Shared Memory

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