

Mentor® Verification IP Altera® Edition Release Notes

Software Version 10.2b

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Introduction

The Mentor® Verification IP Altera® Edition provides Bus Functional Models (BFMs) that simulate the behavior and facilitate the verification of design IP. This release includes support for the ARM AMBA® AXI3TM and AXI4TM bus interfaces. These BFMs conform to the *AMBA® AXITM* and *ACETM Protocol Specification*, *AXI3TM*, *AXI4TM*, and *AXI4-LiteTM*, *ACE*, and *ACE-LiteTM* (ARM IHI 0022D) with restrictions to AMBA AXI3 and AXI4 functionality, described in the section "Protocol Restrictions" in the *Mentor Verification IP Altera Edition AXI3/AXI4 User Guide*.

Note This release supports only the AMBA AXI3 and AXI4 protocols; AMBA AXI4-Lite, ACE, and ACE-lite protocols are not supported.

Release v10.2b includes the following features:

- AMBA AXI3 master, monitor, and slave bus functional models (BFMs).
- AMBA AXI4 master, monitor, and slave bus functional models (BFMs).
- Protocol checks that monitor and report any protocol violations.
- Support for both SystemVerilog (Verilog) and VHDL testbenches.
- Ready-to-use AXI3 and AXI4 master, monitor, and slave components for the Qsys integration tool included with the Altera Quartus II software.
- Support for the Altera Quartus II software, version 13.1.
- Support for the following functional simulation tools:
 - Mentor Graphics ModelSim/Questa Sim 10.2b
 - Synopsys VCS/VCSMX 2013.06
 - o Cadence IES 12.20.014
- Examples showing how to connect and use the BFMs including
 - Qsys system with master, monitor, and slave BFMs connected back to back.
 - o SystemVerilog and VHDL master, monitor, and slave test programs.
- User Guide with tutorials.

These release notes summarize the Changes and Enhancements in this release, Authorization Codes required, and Support Information.

Changes and Enhancements

The following assertions were fixed:

- AXI3 BFM for an incorrect firing of assertion AXI_WRITE_STROBE_ON_INVALID_BYTE_LANES on crossing address boundary.
- AXI4 BFM for an incorrect firing of assertion AXI4_INVALID_WRITE_STROBES_ON_ALIGNED_WRITE_TRANSFER on crossing address boundary.

Authorization Codes

The following authorization codes are required for this release:

- mgcvipae, required to use Mentor Verification IP Altera Edition
- mgcvipaeaxi, required to use AXI3 functionality
- mgcvipaeaxi4, required to use AXI4 functionality

Mentor Verification IP (VIP) Altera Edition is a separately licensed product that is not part of the Modelsim-Altera simulator. Licenses need to be requested from Altera, or your local distributor similar to licenses for the Modelsim-Altera subscription edition.

Support Information

Mentor Verification IP Altera Edition is supported by Altera Corporation Altera World-Wide-Web Support: http://www.altera.com/mySupport.