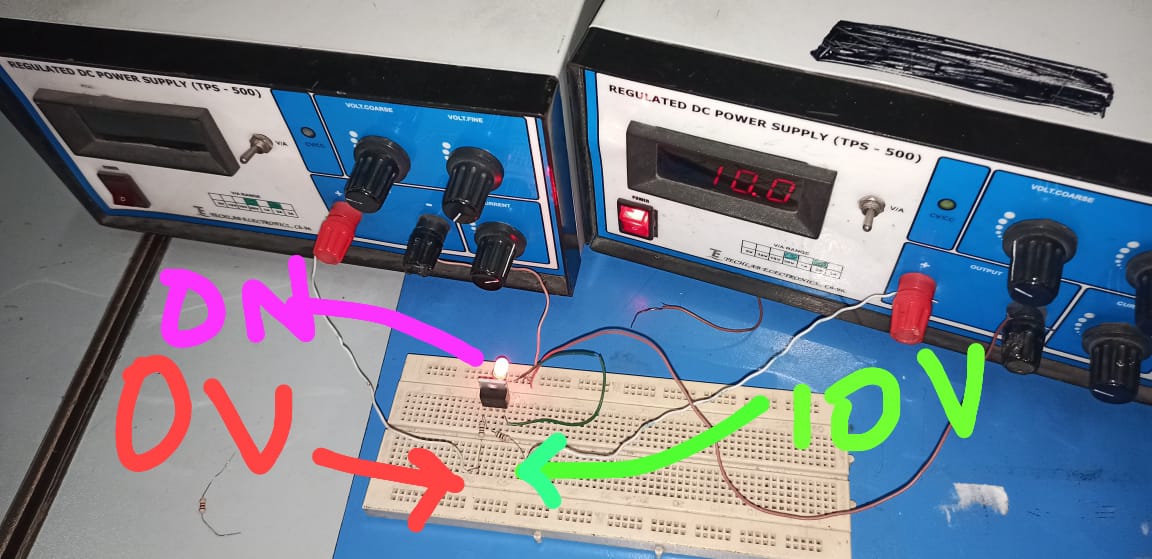
|  |  |
| --- | --- |
| Name: Ali Maaz | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-21 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

**Circuit:**

I patched the circuit in accordance with fig 1.1a



**Tasks:**

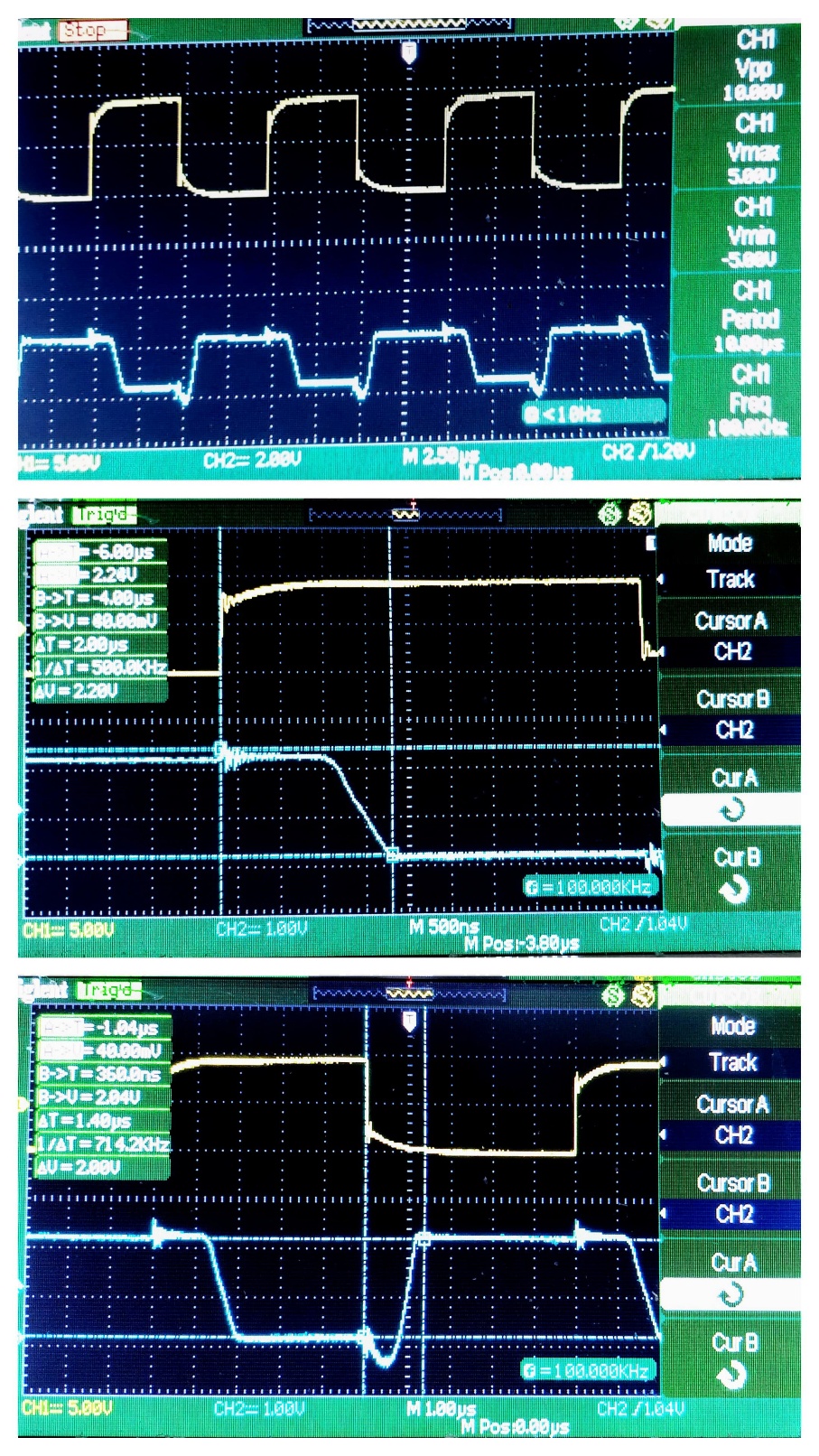
1. Voltage at terminal B is 0V & LED is not glowing
2. Voltage at terminal B is 1.97V & LED is glowing



Output takes **1.6 micro seconds** to go from low voltage to high voltage.

Output takes **2.12 micro seconds** to go from high voltage to low voltage.

**4.**



Output takes **1.4 micro seconds** to go from low voltage to high voltage.

Output takes **2.0 micro seconds** to go from high voltage to low voltage.

1. I think transistor spends less time in the **linear region**, which leads to decreased **power loss**