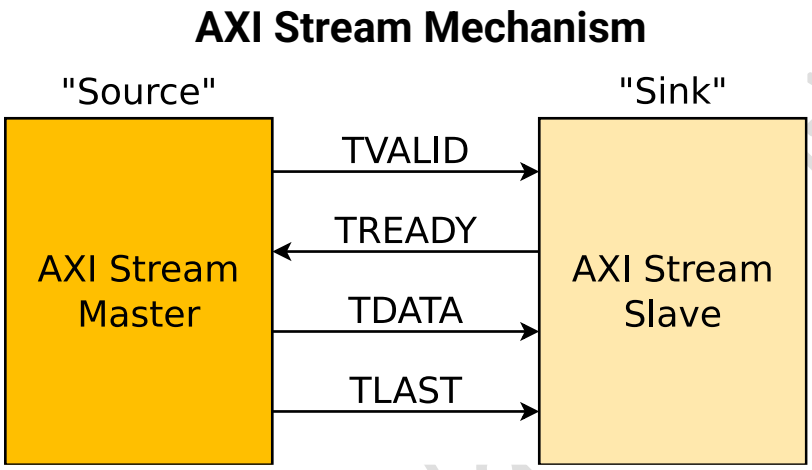
RTL Design of AXI Stream Protocol

AXI (Advanced Extension Interface) is a bus protocol used for high-speed communication between different IP (Intellectual Property) cores in SOC.

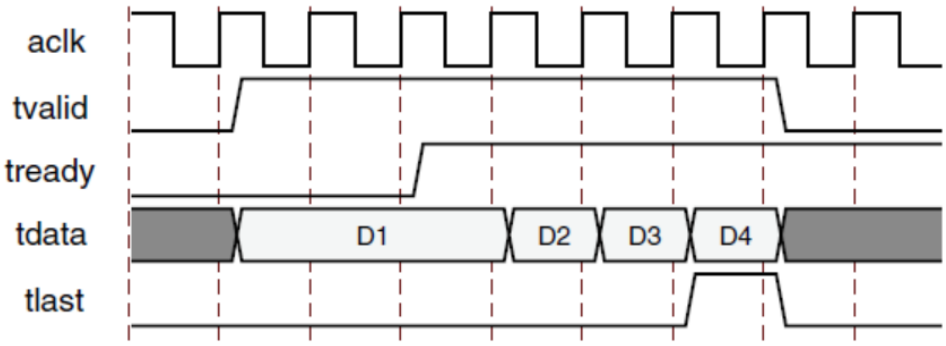
The AXI protocol is used to transfer the data between different component such as memory, input/output interface and processor cores.

AXI Stream =>

AXI Stream protocol is a standard interface to exchange data between connected components. AXI Stream is a point-to-point link, connecting the transmitter known as master and the receiver as slave.



- AXI Stream mechanism is based on tready and tvalid signal as shown above in diagram.
- The tvalid signal is driven by the source(master) side of the channel and tready is driven by the destination or sink (slave) side.
- The tvalid signal indicates that the values in the payload fields (tdata and tlast) are valid. The tready signal indicates that the slave is ready to accept data. When both tvalid and tready are asserted in the same clock cycle, a transfer occurs.
- The order of tvalid or tready going High or Low is not important; data is only transferred when both tvalid and tready are High.



Data Transfer in AXI Stream Channel

AXI Stream Interface Signals

Clock =>

Each component uses a signal, **aclk**. All input signals are sampled on the rising edge of **aclk**. All outputs signal changes must occur after the rising edge of **aclk.**

Reset =>

The protocol includes a single active-LOW reset signal. **aresetn.** The reset signal can be asserted asynchronously, but deasserted must be synchronous after the rising edge of **aclk.**

tvalid=>

tvalid indicates that the master in driving a valid transfer. A transfer takes place when both tvalid and tready are asserted.

tready=>

tready indicates that the slave can accept a transfer in the current cycle.

tdata =>

tdata is primary payload of the AXI stream interface and is used to transport data from a source to destination.

tlast =>

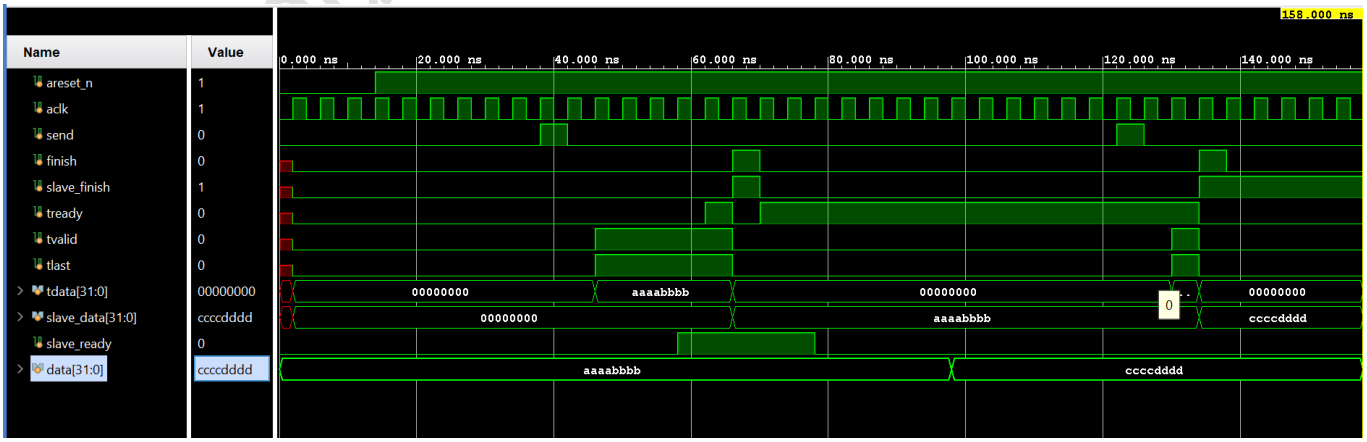
tlast indicates an efficient point to make an arbitration change on a shared link and can be used by a destination to indicates a packet boundary. [**Packet:** Is a grouping of bytes that are transmitted together across the interface]

[**Note:** There is more signals which are optional, I have not covered like tkeep, tstrb, tid, tdest, tuser...]

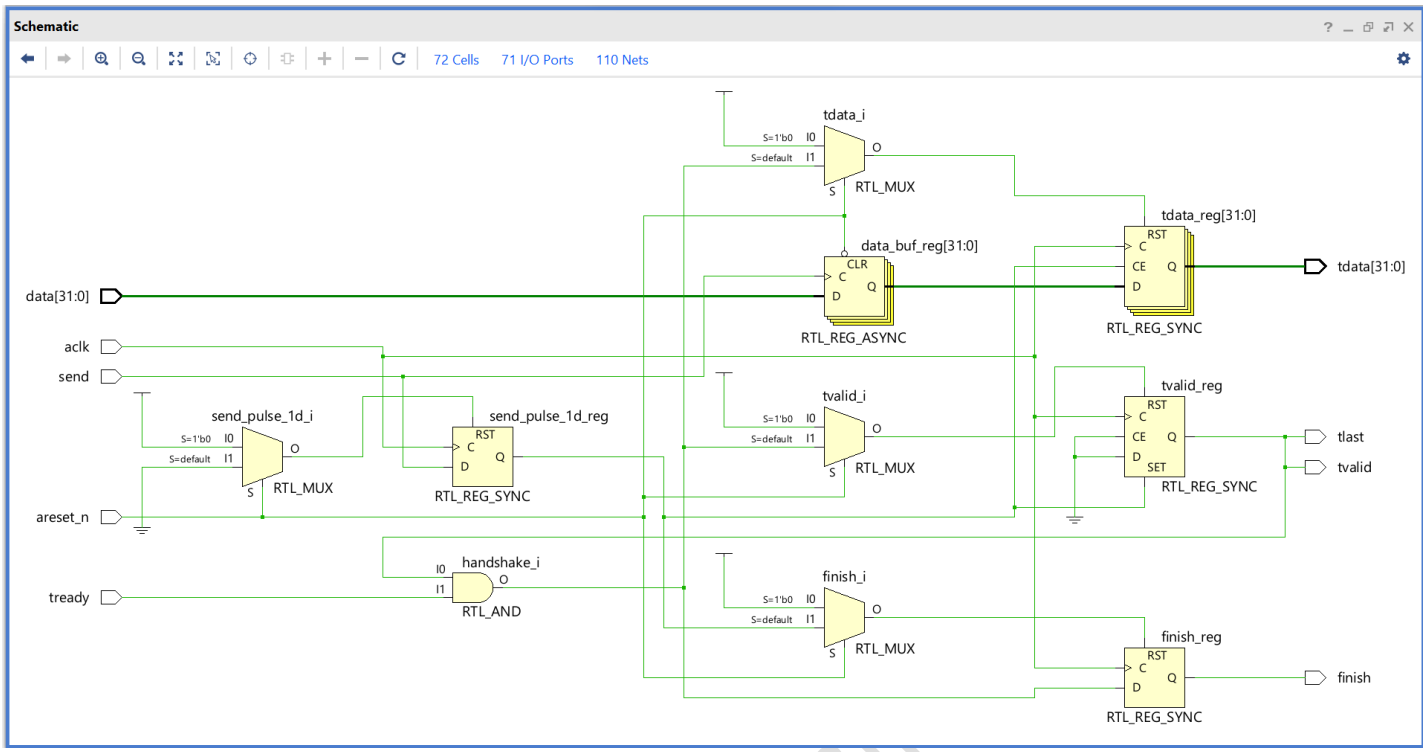
GitHub Code: https://github.com/asimkhan8107/AXI-Stream

Tool: Xilinx Vivado

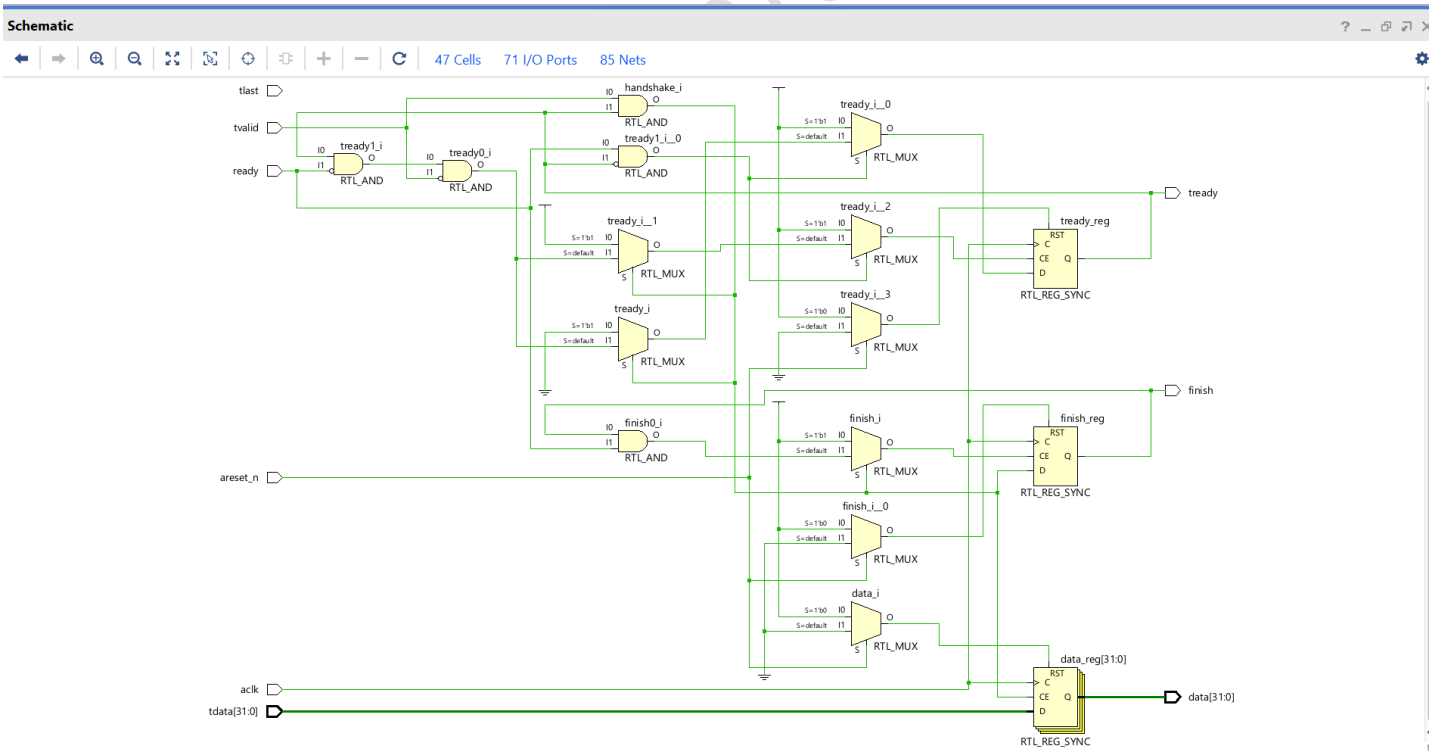
Simulation Result=>



Master RTL Schematic =>



Slave RTL Schematic =>



Reference: pg256 (AMD Xilinx Documentation)