Habib University

Dhanani School of Science and Engineering

Computer Architecture and Organization
EE 371 / CS 330 / CE 321 (Spring 2023)

Homework 2

Instructions:
1. This assignment should be done individually.
2. All questions should be answered in **black ink only**.
3. Scan your answer sheet and upload it on HU LMS before the due date.

Grading Criteria:
1. Your assignments will be checked by instructor/TA.
2. You can also be asked to give a viva where you will be judged whether you understood the question yourself or not. If you are unable to answer correctly to the question you have attempted right, you may lose your marks.
3. Zero will be given if the assignment is found to be plagiarized.
4. Untidy work will result in reduction of your points.

Submission policy:
1. No submission will be accepted after the instructor releases the solution on HU LMS.

CLO Assessment:
This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	***Explain*** the role of ISA in modern processors and instruction encodings and assembly language programming	
CLO 2	***Explain*** the architecture and working of a single cycle processor	✓
CLO 3	***Design*** the architecture to mitigate issues of a pipelined processor	
CLO 4	***Analyze the*** performance of cache operations	

Q1) [10 marks]

You are given with following register values:

x5 = 0x00000000AAAAAAAA, x6 = 0x1234567812345678

a) For the register values shown above, what is the value of x7 for the following sequence of instructions?

```
slli x7, x5, 4
or x7, x7,x6
```

b) For the register values shown above, what is the value of x7 for the following sequence of instructions?

```
slli x7, x6, 4
andi x7, x7, 7
```

c) For the register values shown above, what is the value of x7 for the following sequence of instructions?

```
srli x7, x5, 3
andi x7, x7, 0xFE
```

Q2) [10 marks]

Here is a small C code:

```
while (you_can_do_this_homework[i] == k)
        i+= 1;
```

You are given that the array named "you_can_do_this_homework" has some base address stored in x25. i and k correspond to register x22 and x24. Please translate the above C code to an equivalent assembly code with appropriate instructions. Write explanation for your code.

Q3) [10 marks]

Translate the following C procedure to RISC-V assembly code.

Use a minimum number of instructions. Assume that the values of a, b and i are in registers x5, x6, and x7, respectively. Also, assume that register x10 holds the base address of the array D. Preserve the values of temporary registers used in the procedure using stack.

```
long long int (long long int a, long long int b, long long int i, long long int D[]) {
        int temp = a + b + i;
        if (a > b)
                D[a] = b;
        else
                D[b] = a;
}
```

Q4) [10 marks]

If you have a-bit multiplicand and b-bit multiplier. How many bits you need to represent the product. Give explanation.

Q5.) [10 marks]

A	B
185	122
151	214
216	255
100	120

a) Given A and B are un signed 8-bit number. Is there overflow, underflow, or neither when A-B is done.
b) Given A and B are un signed 8-bit number. Is there overflow, underflow, or neither when A+B is done.
c) Given A and B are signed 8-bit number. Is there overflow, underflow, or neither when A+B is done.
d) Given A and B are signed 8-bit number. Is there overflow, underflow, or neither when A-B is done.

Q6) [10 marks]

Use a table similar to what is shown below, calculate the product of the octal unsigned 6-bit integers 40 and 60. You should show the contents of each register on each step.

Note: Use the same format as given in the table and show each and every step.

Iteration	Step	Multiplier	Multiplicand	Product
0	Initial values	0011	0000 0010	0000 0000
1	1a: 1 ⟹ Prod = Prod + Mcand	0011	0000 0010	0000 0010
	2: Shift left Multiplicand	0011	0000 0100	0000 0010
	3: Shift right Multiplier	0001	0000 0100	0000 0010
2	1a: 1 ⟹ Prod = Prod + Mcand	0001	0000 0100	0000 0110
	2: Shift left Multiplicand	0001	0000 1000	0000 0110
	3: Shift right Multiplier	0000	0000 1000	0000 0110
3	1: 0 ⟹ No operation	0000	0000 1000	0000 0110
	2: Shift left Multiplicand	0000	0001 0000	0000 0110
	3: Shift right Multiplier	0000	0001 0000	0000 0110
4	1: 0 ⟹ No operation	0000	0001 0000	0000 0110
	2: Shift left Multiplicand	0000	0010 0000	0000 0110
	3: Shift right Multiplier	0000	0010 0000	0000 0110

Fig 2

Q7) [15 marks]

Given the RISC V processor implementation below, answer the following:

a) Explain what is meant by a single cycle data path.

b) Explain the working of the Control Unit, and why it is needed?

c) Explain in as much detail as possible, the process of accessing the next instruction, which elements of the above processor are used, and why?

d) Explain the purpose of each of the multiplexers, as they are labeled, in the given processor

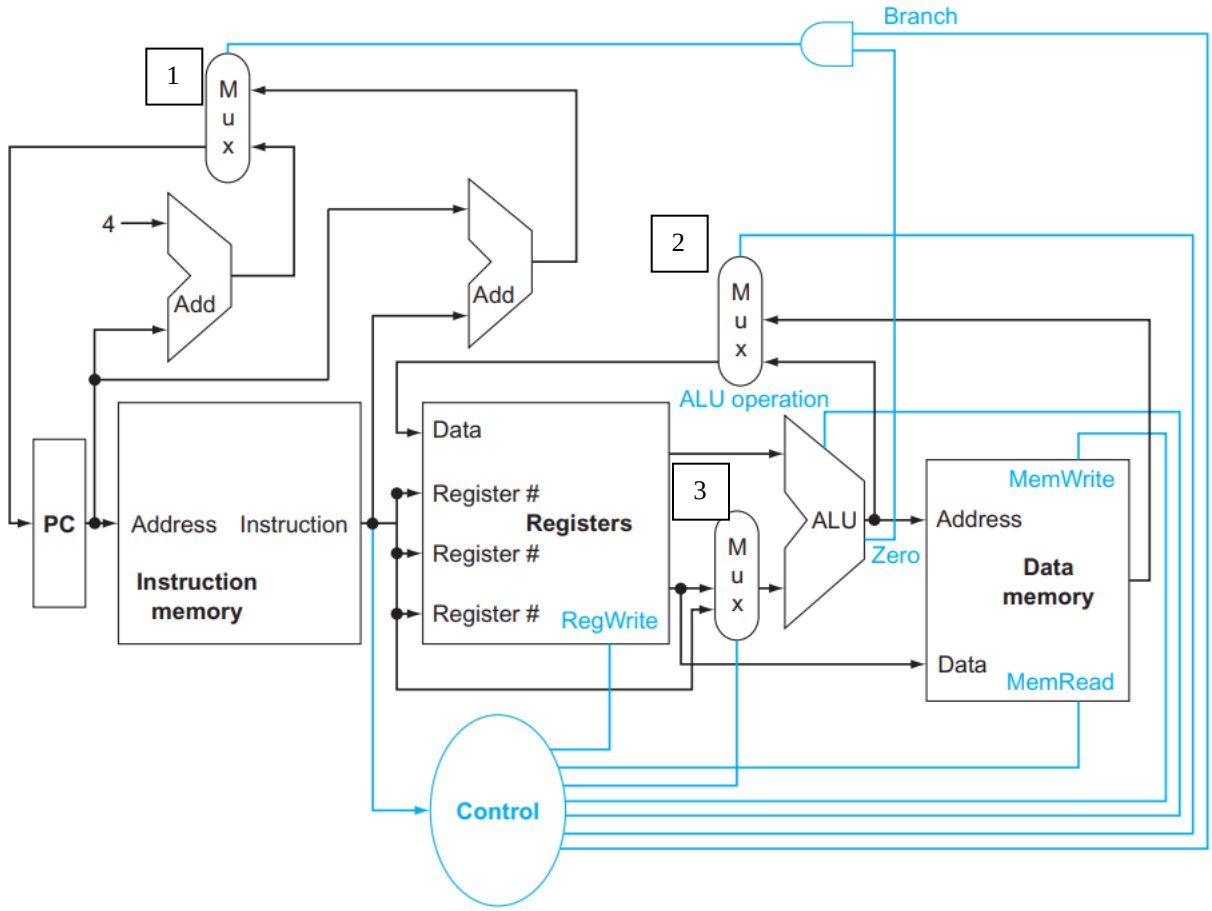

Fig. 3

Q8) [15 marks]

Given the RISC V processor implementation below, answer the following

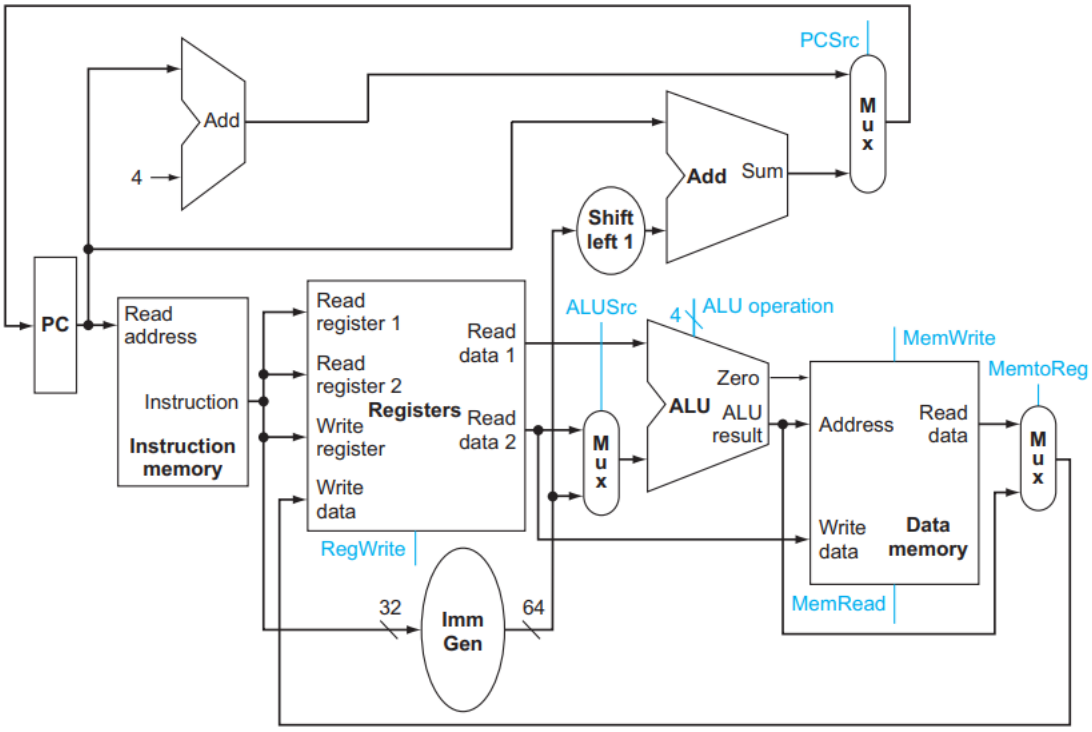

Fig. 4

a) For the instructions below, identify the components of the processor it uses and what are the values of MemRead, MemWrite, RegWrite, and MemtoReg.

i) add x5, x6, x7

ii) ld x5, 64(x2)

iii) sd x6, 80(x2)

iv) addi x5, x6, 5

b) To support branch instructions, what must be added to the processor shown above? What other components of the processor are used when a branch instruction is being run and why are they used?

c) In reference to the above processor implementation, explain the significance and benefit of the generalization of the RISC V instruction format.

Q9) [10 marks]

On a Single Cycle Processor

Consider the following instruction mix:

R-type	I-type (non-LD)	Load	Store	Branch	Jump
20%	16%	30%	18%	9%	7%

(a) What fraction of all instructions use data memory?

(b) What fraction of all instructions use instruction memory?

(c) What fraction of all instructions use the sign extend?

(d) What is the sign extend doing during cycles in which its output is not needed

References

[1] Patterson & Hennesy - “Computer Organization and Design RISC-V Edition ”