Habib University

Dhanani School of Science and Engineering

Computer Architecture
EE 371 / CS 330 / CE 321 (Spring 2023)

Homework 1

Release Date: January 26, 2023	**Due by:** February 02, 2023 11:59 PM

Total marks: 100	**Marks obtained:**

Student Name:	**Student ID:**	**Section:**

Purpose:

The purpose of this assignment is to help you in understanding the role of ISA in modern processors. In addition, this homework will aid you in practicing assembly language programming, and instruction encoding of RISC-V microprocessor.

Instructions:

1. This assignment should be done individually.
2. All questions should be answered in **black ink only**.
3. Scan your answer sheet and upload it on HU LMS before the due date.

Grading Criteria:

1. Your assignments will be checked by instructor/TA.
2. You can also be asked to give a viva where you will be judged whether you understood the question yourself or not. If you are unable to answer correctly to the question you have attempted right, you may lose your marks.
3. Zero will be given if the assignment is found to be plagiarized.
4. Untidy work will result in reduction of your points.

Submission policy:

1. No submission will be accepted after the instructor releases the solution on HU LMS.

CLO Assessment:

This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	***Explain*** the role of ISA in modern processors and instruction encodings and assembly language programming	✓
CLO 2	***Explain*** the architecture and working of a single cycle processor	
CLO 3	***Design*** the architecture to mitigate issues of a pipelined processor	
CLO 4	***Analyze the*** performance of cache operations	

Note: Questions 1 to 4 are worth 15 marks each while questions 5 and 6 are worth 20 points each.

Question 1

Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second? (5 marks)

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. (5 marks)

c. We are trying to reduce the execution time by 30%, but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction? (5 marks)

Question 2

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

a. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2? (5 marks)

b. What is the global CPI for each implementation? (5 marks)

c. Find the clock cycles required in both cases. (5 marks)

Question 3

Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns. (5 marks)

b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code? (5 marks)

c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor? (5 marks)

Question 4

Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also assume that on a single processor a program requires the execution of 2.56E9 arithmetic instructions, 1.28E9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency.

Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by 0.7 × p (where p is the number of processors) but the number of branch instructions per processor remains the same.

a. Find the total execution time for this program on 1, 2, 4, and 8 processors, and show the relative speedup of the 2, 4, and 8 processors result relative to the single processor result. (5 marks)

b. If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, 4, or 8 processors? (5 marks)

c. To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI values? (5 marks)

Question 5

a) Assume that A is an array of 100 doublewords and that the compiler has associated the variables g, h, and j with the registers x19, x20, and x21 respectively. Let's also assume that the starting address, or base address, of the array A is in x22.

Compile these C statements into RISC-V assembly language:

```
g = h + A[8];
A[10] = g – j;
```

(10 marks)

b) For the following C statement, write the corresponding RISC-V assembly code. Assume that the C variables f, g, and h have already been placed in registers x5, x6, and x7, respectively. Use a minimal number of RISC-V assembly instructions.

```
f = g + (h – 5)
```

(10 marks)

Question 6

For the following RISC-V assembly code, assume that the variables f, g, h, i, and j are assigned to registers x5, x6, x7, x28, and x29, respectively. Assume that the base address of the arrays A and B are in registers x10 and x11, respectively.

```
-----------------------------------
        addi x30, x10, 8
        addi x31, x10, 0
        sd x31, 0(x30)
        ld x30, 0(x30)
        add x5, x30, x31
-----------------------------------
```

Answer the following questions:

a. Write the equivalent C code for this RISC-V assembly code. (5 marks)

b. Translate the above assembly language instructions into RISC-V machine language instructions. (15 marks)