Habib University

EE-371/CS-330/CE-321 Computer Architecture – Spring 2023
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Time = 40 minutes **Quiz 01** **Max Points: 20**

SOLUTION

Instructions:

i. ***Smart watches, laptops, and similar electronics are strictly NOT allowed.***
ii. ***Answer sheets should contain all steps, working, explanations, and assumptions.***
iii. Attempt the quiz on clean papers with black/blue ink.
iv. Print your name and HU ID on all sheets.
v. Turn in your question paper along with your answer sheets.
vi. You are not allowed to ask/share your method or answer with your peers. The work submitted by you is solely your own work. Any violation of this will be the violation of HU Honor code and proper action will be taken as per university policy if found to be involved in such an activity.

CLO Assessment:

This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	***Explain*** the role of ISA in modern processors and instruction encodings and assembly language programming	✓
CLO 2	***Explain*** the architecture and working of a single cycle processor	
CLO 3	***Design*** the architecture to mitigate issues of a pipelined processor	
CLO 4	***Analyze the*** performance of cache operations	

Question 1 [6 points]:

You are on the design team for a new processor. The clock of the processor runs at 200 MHz. A program, Benchmark B, is being used to measure the performance of the processor. On the current implementation of the processor, the compilation of Benchmark B results in the following instruction mix: 30% load/store instructions, 50% arithmetic instructions, and 20% all other instructions. Also, the execution of "load/store", "arithmetic", and "other" instructions takes 6, 4, and 3 cycles, respectively.

A) [2 marks] Calculate the global CPI for Benchmark B

B) [4 marks] The CPU execution time on the benchmark is exactly 11 seconds. What is the count of its: (1) Total number of instructions? (2) Total number of "load/store", "arithmetic", and "other" instructions? (3) Total number of cycles used to execute the "load/store", "arithmetic", and "other" instructions? (4) Total number of cycles?

C) [2 marks] The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?

D) [2 marks] The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of loads and stores. What would be the new: (1) Total number of instructions? (2) Total number of cycles? (3) Global CPI (Cycles Per Instruction)?

E) [2 marks] How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

Answer:

A) Let I be the total number of instructions in Benchmark B. Then

The instruction count of:

load/store instructions $I_{LS} = 30\%\ I$

arithmetic instructions $I_A = 50\%\ I$

other instructions $I_O = 20\%\ I$

Also the cycles per instruction (CPI) for:

load/store instructions: $CPI_{LS} = 6$

arithmetic instructions: $CPI_A = 4$

other instructions: $CPI_O = 3$

So the total number of cycles taken by:

load/store instructions: $C_{LS} = I_{LS} \times CPI_{LS}$

arithmetic instructions: $C_A = I_A \times CPI_A$

other instructions: $C_O = I_O \times CPI_O$

And the total number of cycles

C = total number of cycles for load/store cycles +

total number of cycles for arithmetic instructions +

total number of cycles for other instructions

$$C = I_{LS} \times CPI_{LS} + I_A \times CPI_A + I_O \times CPI_O$$

Now Global CPI = $\frac{\text{total number of cycles}}{\text{total number of instructions}}$

$$= \frac{C}{\mathrm{I}}$$

$$= \frac{I_{LS} \times CPI_{LS} + I_A \times CPI_A + I_O \times CPI_O}{\mathrm{I}}$$

$$= \frac{30\%\mathrm{I} \times 6 + 50\%\mathrm{I} \times 4 + 20\% I \times 3}{\mathrm{I}}$$

$$= 4.4$$

B) (1)

$$CPU\ time = \frac{Instruction\ Count \times CPI}{Clock\ Rate}$$

So, $Instruction\ Count(I) = \frac{CPU\ time \times Clock\ Rate}{CPI}$

$$I = \frac{11 \times 200 \times 10^6}{4.4}$$

$$I = 5 \times 10^8 \text{instructions}$$

(2)

I_{LS} = 30% I = $0.3 \times 5 \times 10^8 = 1.5 \times 10^8$ instructions

I_A = 50% I = $0.5 \times 5 \times 10^8 = 2.5 \times 10^8$ instructions

I_O = 20% I = $0.2 \times 5 \times 10^8 = 1.0 \times 10^8$ instructions

(3)

Number of cycles taken by:

Load/store instructions: $C_{LS} = I_{LS} \times CPI_{LS} = 1.5 \times 10^8 \times 6 = 9 \times 10^8$ cycles

Arithmetic instructions: $C_A = I_A \times CPI_A = 2.5 \times 10^8 \times 4 = 10 \times 10^8$ cycles

Other instructions: $C_O = I_O \times CPI_O = 1.0 \times 10^8 \times 3 = 3 \times 10^8$ cycles

(4)

Total number of cycles C = $C_{LS} + C_A + C_O = (9 + 10 + 3) \times 10^8 = 22 \times 10^8$ cycles

C) Clock rate f_C = 200 MHz

So, current cycle time $t_C = \frac{1}{f_C} = \frac{1}{200 \times 10^6} = 5 \times 10^{-9} seconds$

If we double the number of registers, the new cycle time t'_C will be 20% more than t_C

$$t'_C = 1.2\ t_C = 1.2\ \times 5 \times 10^{-9} = 6 \times 10^{-9} seconds$$

So the new clock rate $f'_C = \frac{1}{t'_C} = \frac{1}{6 \times 10^{-9}} = 166.7\ MHz$

D) If we double the number of registers the new count of load/store instructions I'_{LS} is half the original number of load/store instructions I_{LS}

$$I'_{LS} = 0.5 I_{LS} = 0.5\ \times 1.5 \times 10^8 = 0.75 \times 10^8 \text{instructions}$$

(1)

New total number of instructions $I' = I'_{LS} + I_A + I_O = (0.75 + 2.5 + 1) \times 10^8$

$$I' = 4.25 \times 10^8 \text{instructions}$$

(2)

New total number of cycles taken by load/store instructions

$$C'_{LS} = I'_{LS} \times CPI_{LS} = 0.75 \times 10^8 \times 6 = 4.5 \times 10^8$$

So the new total number of cycles will be

$$C' = C'_{LS} + C_A + C_O = (4.5 + 10 + 3) \times 10^8 = 17.5 \times 10^8$$

(3)

The new CPI is

$$CPI' = \frac{\text{New total number of cycles}}{\text{New total number of instructions}} = \frac{C'}{I'} = \frac{17.5 \times 10^8}{4.25 \times 10^8} = 4.12$$

E) The new CPU time

$$t' = \text{New-Instruction-count}\ \times \text{New-CPI} \times \text{New-cycle-time}$$

$$t' = I' \times CPI' \times t'_C = 4.25 \times 10^8 \times 4.12 \times 6 \times 10^{-9} = 10.5 \text{ seconds}$$

Question 2 [8 points]:

Assume that x21 has base address of A, an array of doublewords, and x10 corresponds to constant k.

a) [4 marks] Compile the following C expression into RISC-V assembly language: A[15] = A[3] + k + 5

b) [4 marks] For each instruction: (1) identify whether it is encoded in R-format, I-format, or S-format. (2) Write down the numeric values of the fields (opcode, funct3, funct7, rs1, rs2, rd,

immediate etc.) ordered according to the respective machine code formats. You can choose any one of the decimal, binary, or hexadecimal representations to express these numbers.

Answer:

a)

ld x5, 24(x21) // Temporary reg x5 gets A[3]

add x5, x5, x21 // Temporary reg x5 gets A[3] + k

addi x5, x5, 5 // Temporary reg x5 gets A[3] + k + 5

sd x5, 120(x21) // Stores A[3] + k + 5 into A[15]

b)

ld x5, 24(x21) (I-type instruction)

Immediate	rs1	funct3	Rd	opcode
000001000000	10101	011	00101	0000011

add x5, x5, x10 (R-type instruction)

funct7	rs2	rs1	funct3	rd	opcode
0000000	01010	00101	000	00101	0110011

addi x5,x5,5 (I-type instruction)

Immediate	rs1	funct3	Rd	opcode
000000000101	00101	000	00101	0010011

sd x5, 120(x21) (S-type instruction)

Immediate [11:5]	rs2	rs1	funct3	Immediate [4:0]	opcode
0000011	00101	10101	011	11000	0100011