Habib University

EE-172/CS-130/CE-222 Digital Logic and Design - Fall 2021

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Time = 120 minutes	Midterm Exam	Max Points: 100

Instructions:

a) This is an open book, open notes quiz. Students are allowed to use any printed material for reference.
b) There are 06 questions in the question paper and all of the questions are mandatory.
c) Cell phones, laptops, smart watches, wireless headsets or any other electronic gadgets except scientific calculators are prohibited to use during the exam.
d) The question paper **must be returned** at the end of the exam along with the answer script.
e) Give proper reasoning to your questions where required. Ambiguous answers or untidy work will result in the deduction of your points.
f) Answer sheets should contain **all working and explanations** and assumptions.

CLO Assessment:

This assignment assesses students for the following course learning outcomes.

Course Learning Outcomes		CLO Assessed
CLO 1	Apply r-base (binary, octal, decimal, hexadecimal numbers systems) to digital systems and carry out arithmetic operations and conversions	✓
CLO 2	Apply principles of Boolean Algebra to represent and build equivalent realizations of digital logic (circuits)	✓
CLO 3	Design combinational logic circuits using logic gates	✓
CLO 4	Design sequential systems using finite state machine methodology	

Number Systems (CLO 01)

Question 1: (15 marks) [Expected time 15 mins]

Suppose that you are in a special task force team that is given a task to create a watch that tells you time in minutes 0-59 mins, but no one except your team should be able to read it. You are required to use all of the following characters only (no other characters are allowed):

Coded Symbols

@	#	$	%	+	&	<	>

(a) (05 marks) Fill in the following table and state your assumptions (4 marks)

Solution:

Actual	0	1	2	3	4	5	6	7	8	9	10	11	12
Coded	@	#	$	%	+	&	<	>	#@	##	#$	#%	#+

(b) (05 marks) Represent 43_{10} minutes in your coded notation (3 marks)

Solution:

Quotient	Remainder	Code	
43			
43/8 = 5	3	%	least significant
5/8 = 0	5	&	most significant

$(43)_{10} = (\&\%)_{coded}$

(c) (05 marks) In your number system what does ($@#) represents in decimal?

Solution:

$ = 2 , @ = 0 , # = 1

$(x)_{10} = (8^2)(2) + (8^1)(0) + (8^0)(1)$

$(x)_{10} = 128 + 0 + 1$

$(x)_{10} = (129)_{10}$

Question 2: (15 marks) [Expected time 15 mins]

Do the following arithmetic operation in binary. Determine if the result is correct or not and indicate if there is overflow in the result. Use 2's complement format where required.

(a) (3 marks) 8-bit unsigned operation: (91) + (57)

Solution:

		1	1	1	1		1	1	
91		0	1	0	1	1	0	1	1	91
+ 57	+	0	0	1	1	1	0	0	1	57
+ 148		1	0	0	1	0	1	0	0	unsigned number 148

No overflow has occurred.

(b) (3 marks) 8-bit signed operation: (91) + (57)

Solution:

		1	1	1	1		1	1	
91		0	1	0	1	1	0	1	1	91
+ 57	+	0	0	1	1	1	0	0	1	57
+ 148		1	0	0	1	0	1	0	0	MSB=1 indicated that this is a negative number

2's comp (10010100) = (01101100) = 108

Overflow has occurred.

(c) (3 marks) 8-bit signed operation: (19) - (75)

Solution:

A

			1	1		1	1	1	
19		0	0	0	1	0	0	1	1	19
– 75	+	1	0	1	1	0	1	0	1	2's comp of 75
– 56		1	1	0	0	1	0	0	0	MSB=1 indicated that this is a negative number

2's comp (11001000) = (00111000) = 56

No overflow has occurred.

(d) (3 marks) 8-bit BCD addition: (19) + (75)

Solution:

					carry						
		1	1	1	1 =1				1		
19		0	0	0	1		1	0	0	1	
+ 75	+	0	1	1	1		0	1	0	1	
+ 94		1	0	0	1		1^1	1^1	1	0	
							+	1	1	0	
		1	0	0	1		0	1	0	0	$(94)_{BCD}$

(e) (3 marks) 8-bit BCD subtraction: (19) - (75)

Solution:

Since BCD numbers are decimal numbers:

19 -75 can be solved by adding 19 to 10's complement of 75

10's complement of 75 = 25 = 0010 0101

									1		
19		0	0	0	1		1	0	0	1	
– 75	+	0	0	1	0		0	1	0	1	(2's Comp of 7 and 5)
– 56		0	0	1	1		1	1	1	0	
							0	1	1	0	
		0	1	0	0		0	1	0	0	$(44)_{BCD}$

10's complement of 44 = 56

Since there is no carry in output

Result = - 10's complement of 44 = -56

Note: You can skip comment on overflow in part (d) &(e).

Question 3: (15 marks) [Expected time 15 mins]

Obtain the 2-level NOR implementation and draw the circuit diagram for the following function:

F = [(A+B'+C)(AB+C')]'

Note: You have both complemented and uncomplemented types of inputs available.

Solution:

$F' = (A + B' + C)(AB + C') = AB + ABC + AC' + B'C'$

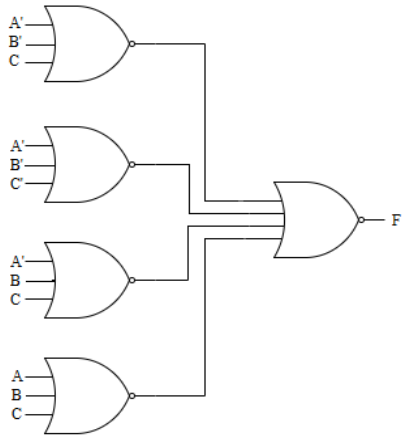
$F' = ABC' + ABC + AB'C' + A'B'C'$

$F = (ABC' + ABC + AB'C' + A'B'C')'$

$F = (ABC')'(ABC)'(AB'C')'(A'B'C')'$

$F = (A' + B' + C)(A' + B' + C')(A' + B + C)(A + B + C)$

$F = \prod(0,4,6,7)$



Question 4:(25 marks) [Expected time 20 mins]

A 2-bit-wide shifter takes two input signals, i_0 and i_1, and shifts them to two outputs, o_0 and o_1, under the control of a shift signal *S*. If *S* is false, then the outputs are equal to their corresponding inputs. If S is true, then o_1 is equal to i_0 and o_0 is set to 0.

a) (10 marks) Complete the following truth table

Solution:

S	i_0	i_1	o_0	o_1
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	0	1

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b) (05 marks) Write down the *Canonical POS* expression for the above outputs.

Solution:

Product of Maxterms:

$o_0 = (S+i_0+i_1)(S+i_0+i_1')(S'+i_0+i_1)(S'+i_0+i_1')(S'+i_0'+i_1)(S'+i_0'+i_1') = \prod(0,1,4,5,6,7)$

$o_1 = (S+i_0+i_1)(S+i_0'+i_1)(S'+i_0+i_1)(S'+i_0+i_1') = \prod(0,2,4,5)$

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c) (10 marks) Use k-maps to find the most simplified PoS expression for both outputs.

Solution:

For o_0:

S \ $i_0\ i_1$	00	01	11	10
0	0	0	1	1
1	0	0	0	0

$$PoS = o_0' = i_0' + S$$

$$o_0 = (i_0' + S)' = i_0.S'$$

For o_1:

S \ $i_0\ i_1$	00	01	11	10
0	0	1	1	0
1	0	0	1	1

$$PoS = o_1' = S'.i_1' + S.i_0'$$

$$o_1 = (S'.i_1' + S.i_0')'$$
$$o_1 = (S'.i_1')'.(S.i_0')'$$
$$o_1 = (S + i_1).(S' + i_0')$$

Combinational Logic Circuits (CLO 03)

Question 5: (30 marks) [Expected time 30 mins]

A student team arranges a limited inventory by pooling the funds. They are required to develop **two** *different* circuits of a 2-bit Magnitude differentiator (defined below), to be used in different parts of the robotic limbs of their prototype. Inventory parts, their quantity and cost is given as under.

A magnitude differentiator is a system which provides output D as the magnitude of difference between two numbers (A and B) i.e.

$$D = |A - B|$$

Inventory of Items

Type of part	Quantity available	Price per part
16 x 1 MUX	2	Rs. 100
8 x 1 MUX	4	Rs. 40
4 x 1 MUX	8	Rs. 12
AND/OR/NOT gates	5 DIP ICs (20 gates) for each type	Rs. 12 per IC (4 gates per IC)
3 x 8 Decoder	2	Rs. 30
Full Adders	2	Rs. 50
XOR gates	1 DIP IC (4 gates)	Rs. 20 per IC

a) (05 marks) Complete the following truth table.

Solution:

A		B		D	
A1	A0	B1	B0	D1	D0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	0	0

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b) (05 marks) Write down the Boolean function to describe the function D.

Solution:

For *D1*:

$A_1\,A_0$ \ $B_1\,B_0$	00	01	11	10
00			1	1
01			1	
11	1	1		
10	1			

$Canonical\ SoP\ = \sum(2,3,7,8,12,13)$

$D_1 = A_1B_1'B_0' + A_1A_0B_1' + A_1'A_0'B_1 + A_1'B_1B_0$

For *D0*:

$A_1\,A_0$ \ $B_1\,B_0$	00	01	11	10
00		1	1	
01	1			1
11	1			1
10		1	1	

$Canonical\ SoP\ = \sum(1,3,4,6,9,11,12,14)$

$D_0 = A_0B_0' + A_0'B_0 = A_0 \oplus B_0$

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c) (05 marks) List down at least 04 possible different implementations of the logic regardless of cost.

Solution:

Approach 1: using 16x1 MUX

Approach 2: using 8x1 MUX and few gates

Approach 3: using decoder

Approach 4: using gates

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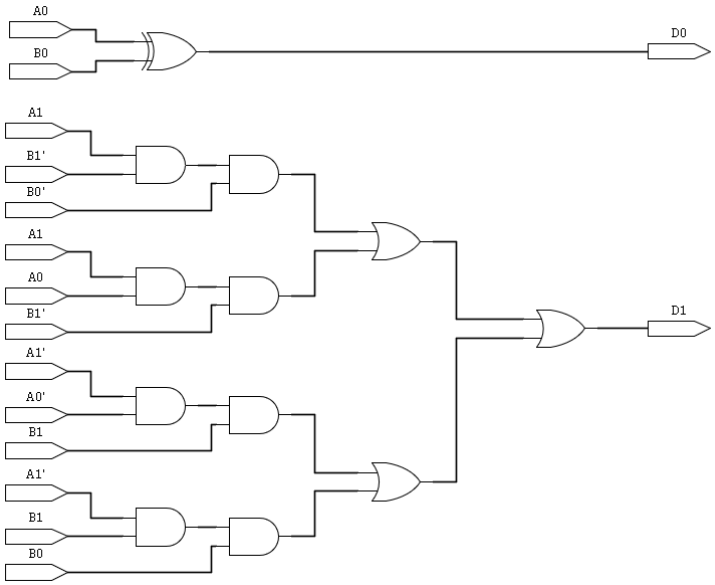
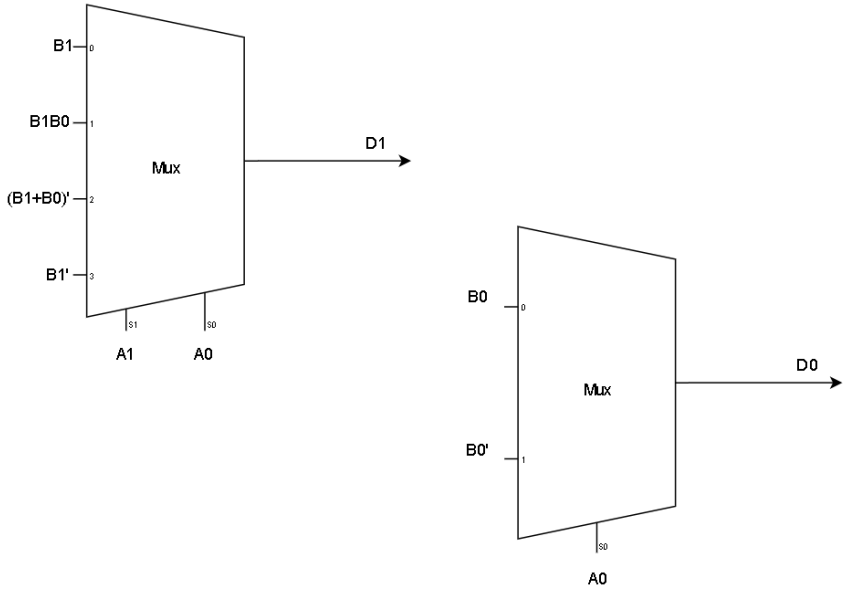
d) (10 marks) Pick the items from given inventory and rearrange the expression or use simplification methods to show two different implementations of the logic.

Solution: there can be multiple and wide variety of solutions in this. Two solutions should be different and correct implementations of expressions obtained for D0 and D1. Given are two sample implementations.

Implementation 1:



Implementation 2:



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e) (05 marks) Comment on approach to get least possible expense and least possible gate delay.

Solution:

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