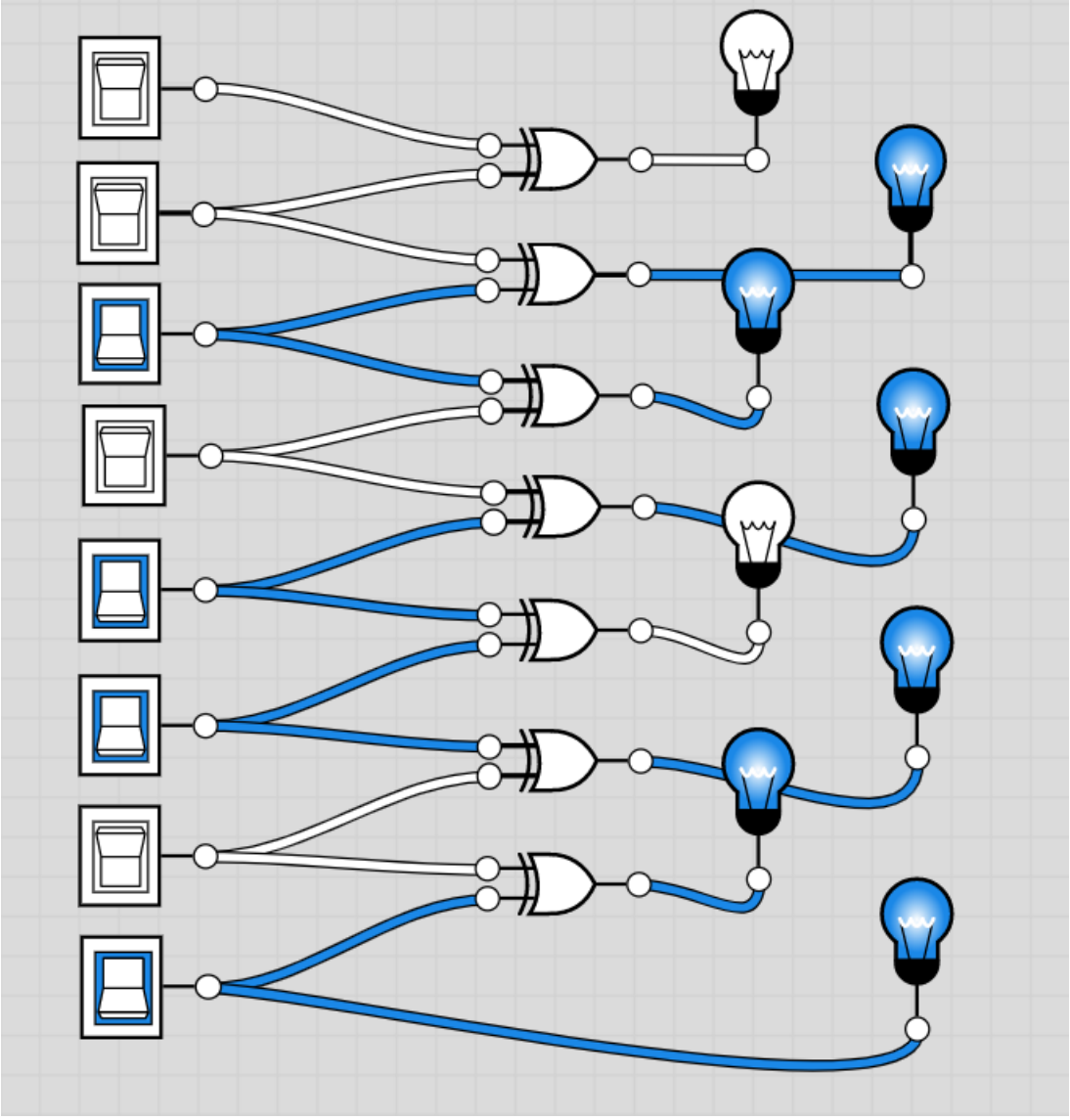
Digital Logic and Design – Fall 2022

Homework # 2 – K-maps and Boolean circuit Solutions

Q.1 Think of a logic circuit that converts an 8-bit binary number to its equivalent gray code. Simulate that circuit on logic.ly and add the screenshot that shows the conversion of 10110100 to its equivalent gray code.

Note: The switches go from LSB -> MSB.



Q.2 Perform the following operations:

a.) Find the complement of F = wx + yz, then show that FF' = 0 and F + F = 1

$$F' = (wx + yz)' = (wx)'(yz)' = (w' + x')(y' + z')$$

$$FF' = wx(w' + x')(y' + z') + yz(w' + x')(y' + z') = 0$$
$$F + F' = wx + yz + (wx + yz)' = A + A' = 1 \text{ with } A = wx + yz$$

b.) **Simplify the following expression using boolean algebra**

i.) (x + y)(x + y ')(xz')'

(c) $(x+y)(x+y')(xz')'$

$= (x+y)(x+y')(x'+z)$

$= (x + xy' + xy)(x'+z)$

$= xz + xy'z + xyz$

$= xz(1 + y' + y) = xz$

ii.) w' (wxyz)'

(b) $w' \cdot (wxyz)' = w' \cdot (w' + x' + y' + z')$

$= w'w' + w'x' + w'y' + w'z'$

$= w' + w'x' + w'y' + w'z'$

$= w'(1 + x' + y' + z')$

$= w'$

iii.) (ab + c')' + ac'b + b

$(a' + b')c + abc' + b$

$(a' + b')c + b(1 + ac')$

$(a' + b')c + b$

$a'c + c + b$

$c(1 + a'_ + b$

$c + b$

c.) **We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called bitwise operation). Given two eight-bit strings A = 10110001 and B = 10101100, evaluate the eight-bit result after the following logical operations:**

i.) **A OR B** = 1011 1101
ii.) **A XOR B** = 0001 1101
iii.) **NOT B** = 0101 0011

Q3. Simplify the following expressions using Boolean algebra postulates and theorems. Indicate all postulates or theorems used to prove the statements.

a) **(x + x ')'**
(x'x) ; (Demorgans Theorem)
0 ; (AA' = 0)

b) **w'·(wxyz)'**
Q2b repeated(ii)

c) **(x + y) · (x + y ') · (xz')**
Q2b repeated(iii)

Q4. A bank vault has three locks with a different key for each lock. Each key is owned by a different person. In other to open the door, at least two people must insert their keys into the assigned locks. The signal lines A, B, and C are 1 if there is a key inserted into lock 1, 2, or 3, respectively.

a) **Make a truth table for the given scenario for a variable Z which is 1 if the door should open.**

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

b) Write Minterms and Maxterms associated with the function and express Boolean function for Z in both canonical forms

Minterms: A'BC+AB'C+ABC'+ABC

Maxterms: (A+B+C) (A+B+C') (A+B'+C) (A'+B+C)

SOP: $Z = \sum(3, 5, 6, 7)$

POS $Z = \Pi(0, 1, 2, 4)$

Q.5 Using De Morgan's theorems, find the complement of the following:

i. $(a' + cd')(abc' + bd)(ad' + b + c')$

$$(a + cd')' + (abc' + bd)' + (ad' + b + c')'$$

$$a(c' + d) + (a' + b' + c)(b' + d') + (a' + d)(b'c)$$

ii. $(xyz' + x'z + yz')(xy)$

$$(xyz' + x'z + yz')' + (xy)'$$

$$(xyz')'(x'z)'(yz')' + (x' + y')$$

$$(x' + y' + z)(x + z')(y' + z) + (x' + y')$$

Q6. Write the Canonical POS form for the following expressions.

$$Y = \big((AB + A'B')(CD' + C'D)\big)'$$

$$(ABCD' + ABC'D + A'B'CD' + A'B'C'D)'$$

$$(A' + B' + C' + D)(A' + B' + C + D')(A + B + C' + D)(A + B + C + D')$$

$$F = \Pi m(1, 2, 13, 14)$$

Q7. For the Boolean function:

$$F = xy'z + x'y'z + w'xy + wx'y + wxy$$

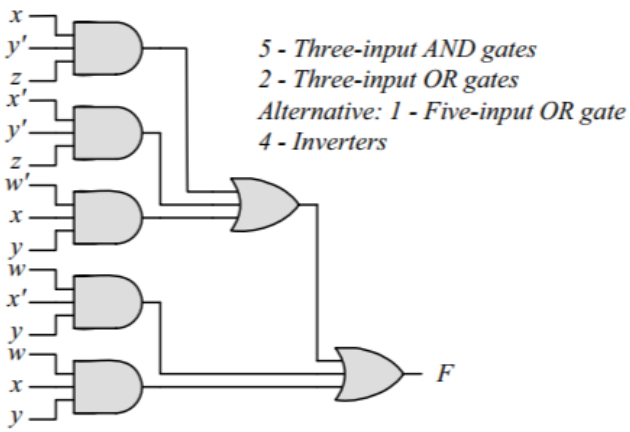
(a) Obtain the truth table of F.

$F = xy'z + x'y'z + w'xy + wx'y + wxy$

$F = \Sigma(1, 5, 6, 7, 9, 10\ 11, 13, 14, 15)$

wx y z	F
00 0 0	0
00 0 1	1
00 1 0	0
00 1 1	0
01 0 0	0
01 0 1	1
01 1 0	1
01 1 1	1
10 0 0	0
10 0 1	1
10 1 0	1
10 1 1	1
11 0 0	0
11 0 1	1
11 1 0	1
11 1 1	1

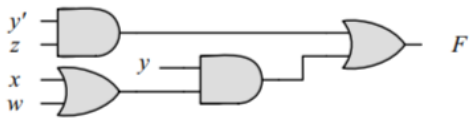
(b) Draw the logic diagram, using the original Boolean expression.



(c) Use Boolean algebra to simplify the function to a minimum number of literals.

$$F = xy'z + x'y'z + w'xy + wx'y + wxy$$
$$F = y'z + xy + wy$$
$$F = y'z + y(w + x)$$

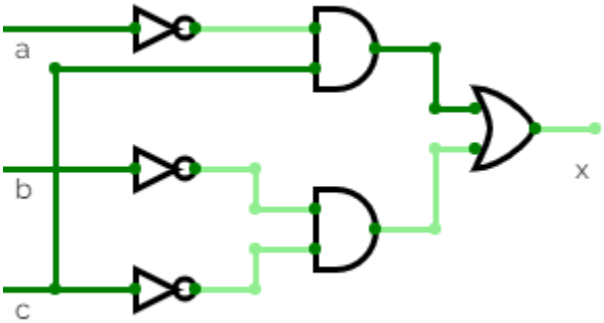
(d) Draw the logic diagram from the simplified expression, and compare the total number of gates with the diagram of part (b).



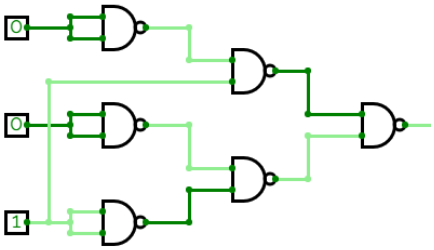
1 – Inverter, 2 – Two-input AND gates, 2 – Two-input OR gates

Q8. Using the given logic circuits,

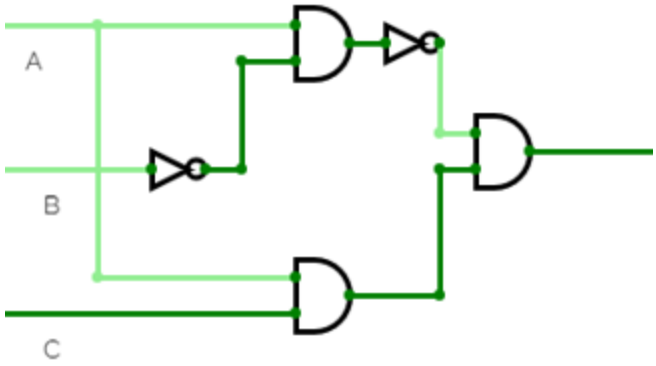
a) Sketch NAND logic implementation:



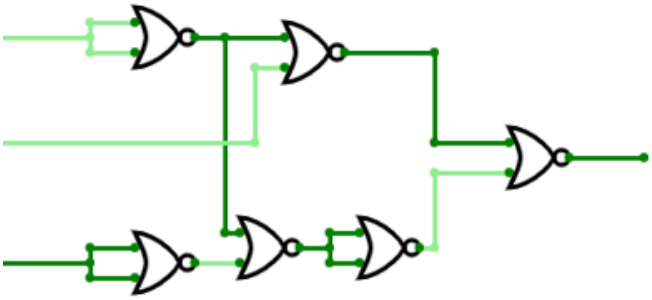
Solution:



b) Sketch NOR logic implementation:



Solution



Q9. Perform following by using only Boolean algebra postulates and theorems

a.) F(a,b,c,d) = (a + cd) (d + a'b) into a product of maxterms form

F = (a + cd) (d + a'b)
F = (a + c) (a + d) (a' + d) (b + d)
F = (a + bb' + c + dd') (a + bb' + cc' + d) (a' + bb' + cc' + d) (aa' + b + cc' + d)
F = (a + b + c + d) (a + b + c + d') (a + b' + c + d) (a + b' + c + d') (a + b + c' + d) (a + b' + c' + d) (a' + b + c + d) (a' + b + c' + d) (a' + b' + c + d) (a' + b' + c' + d)

F = Πm(0,1,2,4,5,6,8,10,12,14)

b.) F(w,x,y,z) = (w'z + x) (y' + wy'x) (xz' + w) into a sum of minterms form

F = (w'z + x) (y' + wy'x) (xz' + w)
F = (w'y'z + ww'xy'z + xy' + wxy') (xz' + w)
F = w'xy'zz' + ww'y'z + xy'z' + wxy' + wxy' + wxy'z
F = xy'z' + wxy' + wxy'z
F = (w + w')xy'z' + (z + z')wxy' + wxy'z
F = w'xy'z' + wxy'z' + wxy'z

F = ∑m(4,12,13)

c.) F(i,j,k,l) = ij'l + j'kl' + i'j'k' into a sum of minterms form

F = ij'l + j'kl' + i'j'k'
F = ij'l (k + k') + j'kl' (i + i') + i'j'k' (l + l')
F = ij'kl + ij'k'l + ij'kl' + i'j'kl' + i'j'k'l + i'j'k'l'
F = ∑m(0,1,2,9,10,11)

d.) F'(p, q, r, s) = p'q'r + p'rs' + pq'r's into a product of maxterm form

F' = p'q'r + p'rs' + pq'r's
F = (p'q'r + p'rs' + pq'r's)'
F = (p'q'r)' (p'rs')' (pq'r's)'
F = (p + q + r') (p + r' + s) (p' + q + r + s')
F = (p + q + r' + ss') (p + qq' + r' + s) (p' + q + r + s')
F = (p + q + r' + s) (p + q + r' + s') (p + q' + r' + s) (p' + q + r + s')
F = Πm(2,3,6,9)

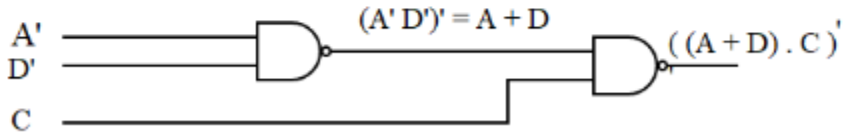
e.) Simplify the following function, and implement it with two-level NAND gate circuit.

i) F(A, B, C) = (A' + C' + D')(A' + C') (C' + D')

F = (A C D)' (A C)' (C D)' (De Morgan's law)
F = (A C D)' (A C)' (C D)'
F = (A C D + A C + C D)'
F = (AC (1 + D) + C D)'
F = (A C + C D)'
F = (C (A + D))'

F = C' + A'D'

We will implement it using two-level NAND gates as follows:



Q10. Use Karnaugh maps to convert the following POS expressions to minimum SOP expressions: [3 + 4]

a. $(A + B')(A + C')(A' + B' + C)$

AB/C	0	1
00	1	0
01	0	0
11	0	1
10	1	1

$$SOP: B'C' + AC$$

b. $(A' + B)(A' + B' + C')(B + C' + D)(A + B' + C + D')$

AB/CD	00	01	11	10
00	1	1	1	0
01	1	0	1	1
11	1	1	0	0
10	0	0	0	0

$$SOP: A'C'D' + A'B'D + A'BC + ABC'$$

Q11. A system responds to a different combination of superimposed sinusoids with different frequencies. You take the Fourier transform of these signals and find that there are at most 4 frequencies present in them. The frequencies are mapped to variables in the following manner:

A = 300 Hz

B = 550 Hz

C = 800 Hz

D = 1100 Hz

a) Find out the simplified Boolean expressions using k-maps for the outputs X and Y if the system responds as:[5]
X(A,B,C,D) = $\Sigma_m(1,3,7,9,11,13,15)$
Y(A,B,C,D) = $\Pi_m(0,1,3,15,11)$

For X(A,B,C,D):

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	0	1	1	0
$\overline{A}B$	0	0	1	0
AB	0	1	1	0
$A\overline{B}$	0	1	1	0

X = B'D + CD + AD

For Y(A,B,C,D):

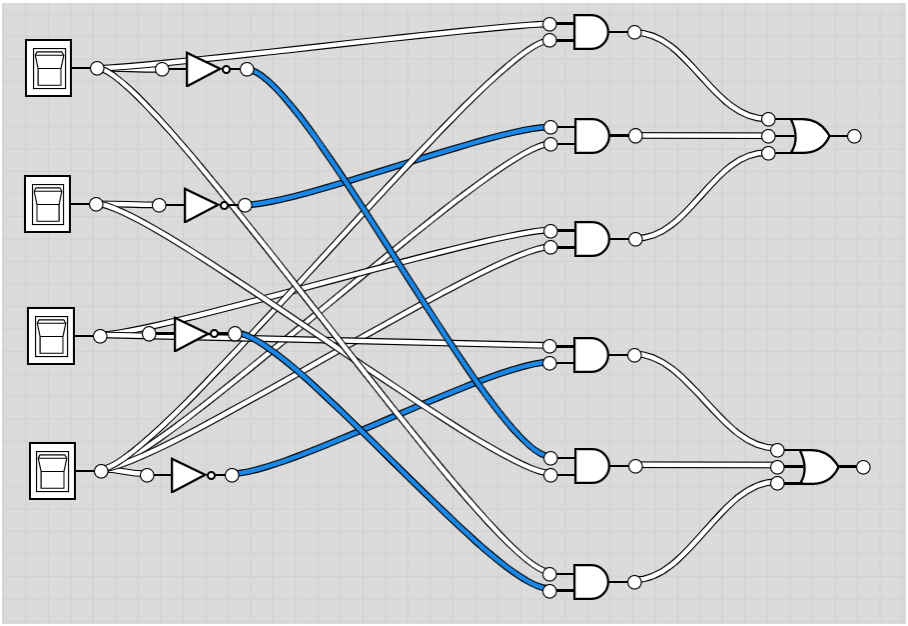
	$\overline{C}.\overline{D}$	$\overline{C}.D$	$C.D$	$C.\overline{D}$
$\overline{A}.\overline{B}$	0	0	0	1
$\overline{A}.B$	1	1	1	1
$A.B$	1	1	0	1
$A.\overline{B}$	1	1	0	1

Y = CD' + A'B + AC'

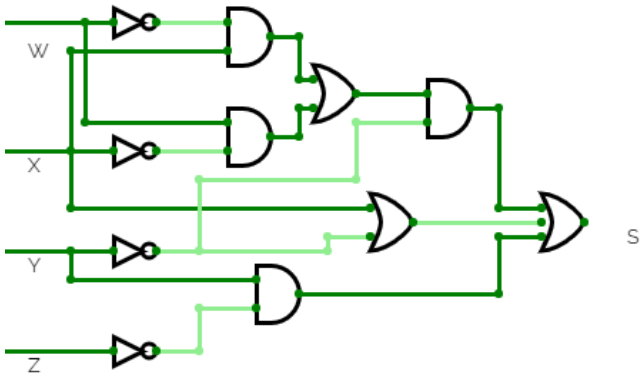
b) You are now asked to replace the system with a Logic circuit that responds to the inputs in the same way as the system does. Assume that the inputs are now 4 discrete variables, each corresponding to a frequency present in the sinusoids. Draw this circuit on logic.ly and attach a properly labelled screen shot.

Input sequence: A->B-C->D

Output sequence: X->Y



Q12. You have been hired as a lab designer in the DLD lab. Your instructor has decided to ask the students to implement the following logic circuit on a breadboard using ICs.



The problem is that the ICs in the lab are not sufficient for all the students to use. So, you decide to simplify the circuit and reduce the number of gates used.

a. **To proceed, use Boolean algebra techniques to get the simplified expression of the given circuit.**

$$(w'x + wx')y' + (x + y') + yz'$$

$$w'xy' + wx'y' + x + y' + yz'$$

$$y'(w'x + wx' + 1) + x + yz'$$

$$y' + x + yz'$$

$$x + y' + z'$$

b. **You are skeptical in your simplification and want to verify if the obtained expression is correct. For that, you make the truth table of the circuit above.**

W	X	Y	Z	S
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1

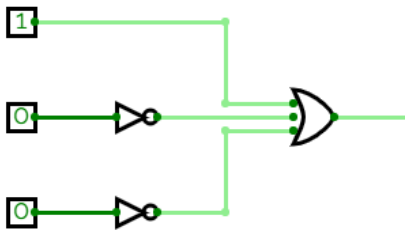
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

c. Using the truth table, simplify the circuit using K-maps.

wx \ yz	00	01	11	10
00	1	1	0	1
01	1	1	1	1
11	1	1	1	1
10	1	1	0	1

The given k map gives the expression: x+y'+z'

d. Verify that the simplified expression obtained is the same as the one obtained in part a by drawing the simplified circuit. Is the number of gates used after simplification the same as the one used originally?



Q13. You work in a company that optimizes electrical solutions for different clients in terms of either cost, no. of components and/or types of components.

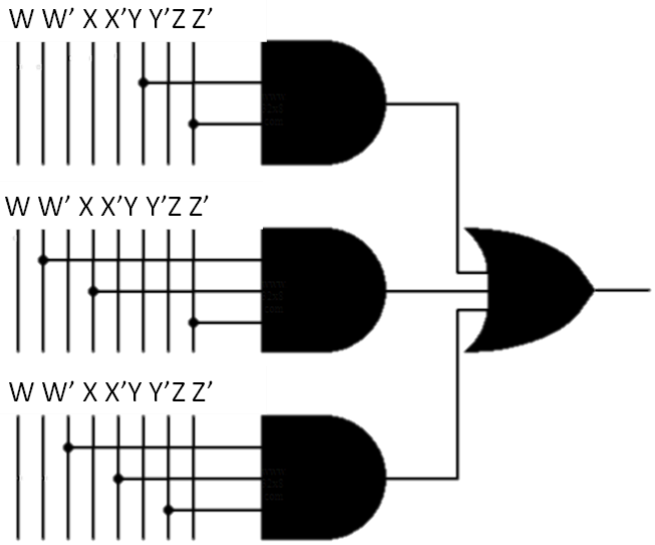
a) The client you are working with right now wants to reduce the cost and number of components in their circuit design. Assuming that all of the components cost the same, minimize the following SOP representation of their circuit design using K-map reduction.

F(W, X, Y, Z) = ∑(0, 2, 8, 12, 15)
d(W, X, Y, Z) = ∑ (3, 4, 7, 14) (don't care conditions)

	00	01	11	10
00	1		x	1
01	x		x	
11	1		1	x
10	1			

F = Y'Z' + W'X'Z' + XYZ

b) Draw a circuit diagram for the reduction you have performed in (a)



c) To complete the solution, you are required to also list down the number of terms and no of literals in each term in the original design as well as the reduced one. Hence, please list those:

Original:
Terms: 5
Literals: 5 for all

Reduced:
Terms: 3
Literals: 2, 3 and 3 respectively

d) Good work! Your client was satisfied with the result! However, before the 1-year contract ends, this client has returned to the office and now they want to reduce the types of components in their solution.

Since NOR gates are universal gates, you can replace all the different gates in your circuit in (b) with a combination of NOR gates. Hence, draw a NOR representation of your circuit.