

### Logic Course Assignment #5

- 1- Construct a 5 to 32 decoder using four 3 to 8 decoders with enables, and a 2 to 4 decoder.
- 2- Design a 4-input priority encoder.
- 3- Design a 4 to 16 decoder using logic gates. The inputs are A, B, C, D and the outputs are active low  $/y_0, /y_1, \dots, /y_{15}$ . The decoder should have one active high enable line, E.
- 4- Design a 5 to 32 decoder using only 3 to 8 decoder modules. Assume that each 3 to 8 decoder has one active-low enable input  $/E_1$ , and one active-high enable input,  $E_2$ .
- 5- Design a 32 to 1 multiplexer using:
  - a) only 74151 modules (check the books and data sheets for specifications),
  - b) two 74150 modules and one 4 to 1 multiplexer,
  - c) two 74150 modules and one NAND gate.
- 6- Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.
- 7- Realize the following functions using a 4 to 1 multiplexer module:
  - (a)  $f_1(a, b, c) = \sum m(2, 4, 5, 7)$
  - (b)  $f_2(a, b, c) = \prod M(0, 6, 7)$
  - (c)  $f_3(a, b, c) = (a + b')(b' + c)$
- 8- Given the following circuit, with the decoder having active-low outputs as shown, find the expression for  $f(w, x, y, z)$  in SOP form.

