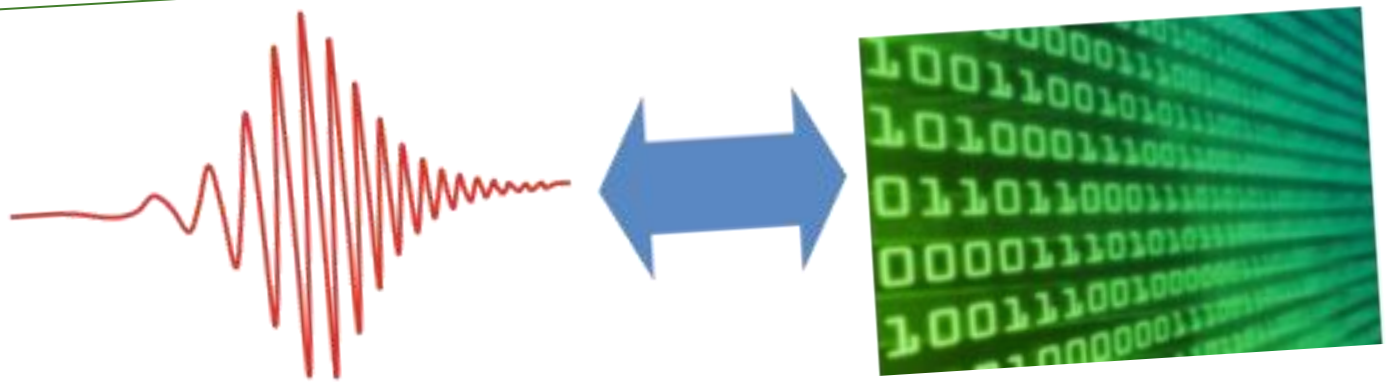
Level-Crossing Analog to Digital Converter
LC-ADC



Analog to Digital Conversion [1]

1928
K. N. Toosi University
of Technology

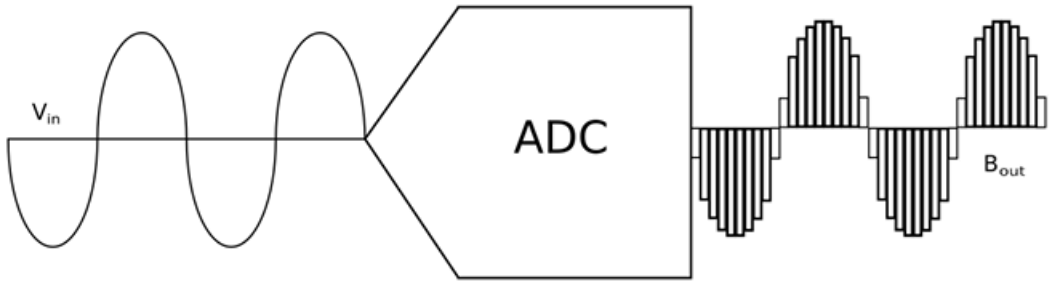
Presenter: Ali Qorbani Fard

Supervisor: Dr. Hossein Shamsi

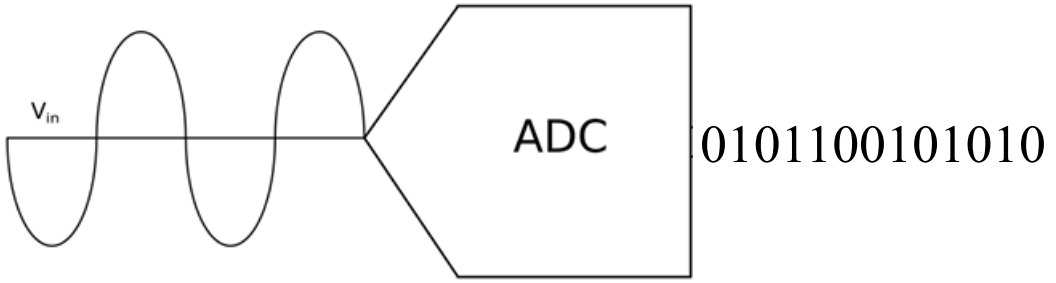
[1] Marcel J.M Pelgrom, “Analog-to Digital Conversion”, 4th ed. Stiphout, the Netherlands: Springer, 2021.

TABLE Of Contents

INTRODUCTION

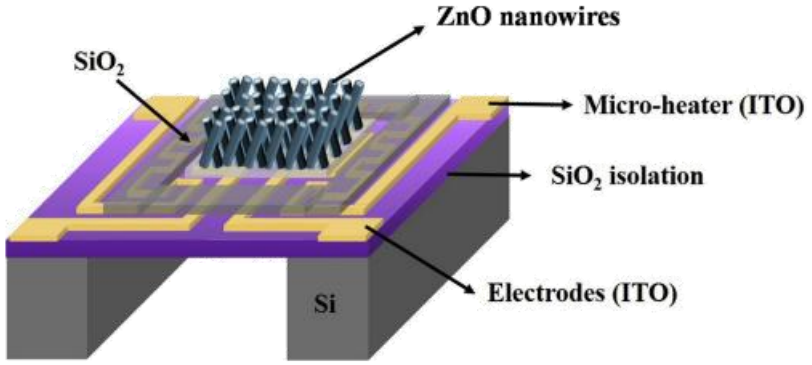


Simplified diagram of ADC [2]



Analog to Digital Converter
Modified Version of [2]

- What is ADC?
- Quantization
- ADC Application
- ADC & Sensors



Gas sensor [3]

[2] Anthony Troxell , “DESIGN AND LAYOUT OF A FIXED WINDOW 6-BIT LEVEL CROSSING ANALOG-TO-DIGITAL CONVERTER,”,M.S thesis, Dept. of Electrical Eng., California State University, Spring 2023.
[3] Ting-Jen Hsueha, Chien-Hua Pengb, Wei-Shou Chenc, "A transparent ZnO nanowire MEMS gas sensor prepared by an ITO micro-heater," Elsevier , October. 2019.

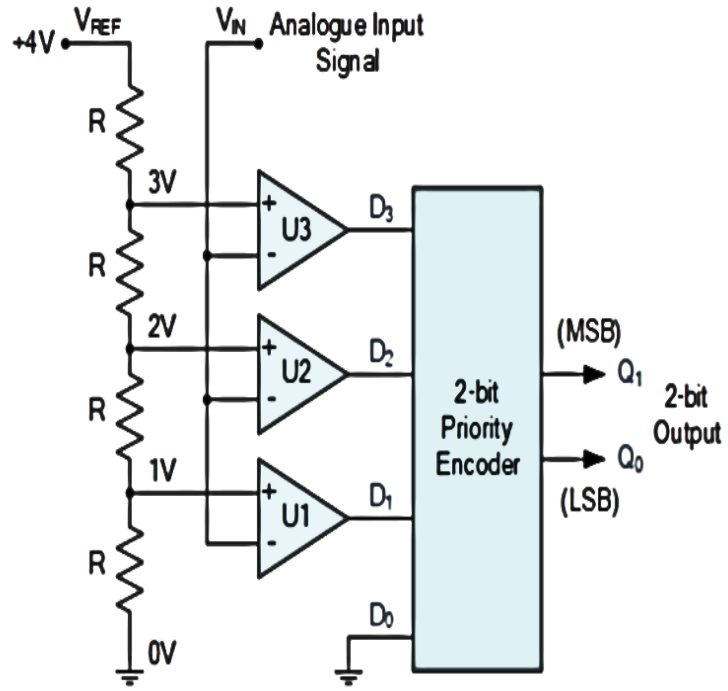
OVERVIEW OF ADC ARCHITECTURES / Flash

Pros:

- ✓ Extremely Fast Conversion
- ✓ Simple Architecture (for Low Bit-Depth)

Cons:

- ❑ Exponential Hardware Need
- ❑ High Power Consumption
- ❑ Large Chip Area
- ❑ Thermal and Process Sensitivity



Flash ADC, modified Version of [1]
V_{in} = 2.3 V

[1] Marcel J.M Pelgrom, "Analog-to Digital Conversion", 4th ed. Stiphout, the Netherlands: Springer, 2021.

OVERVIEW OF ADC ARCHITECTURES / SAR

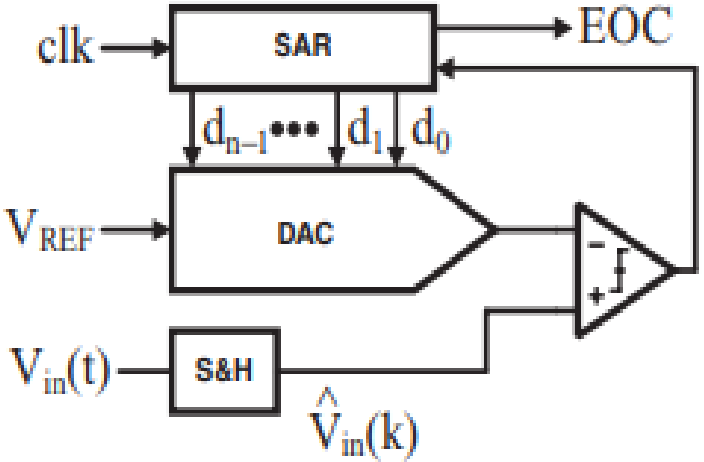
Pros:

- ✓ Cost effective
- ✓ smaller area
- ✓ higher resolution is available

Cons:

- ❑ Slower conversion speed
- ❑ Requires DAC

Successive approximation ADC



SAR ADC [4]

[4] Gabriele Manganaro, "Advanced Data Converters", 1st ed. Cambridge: Cambridge University press, 2012.

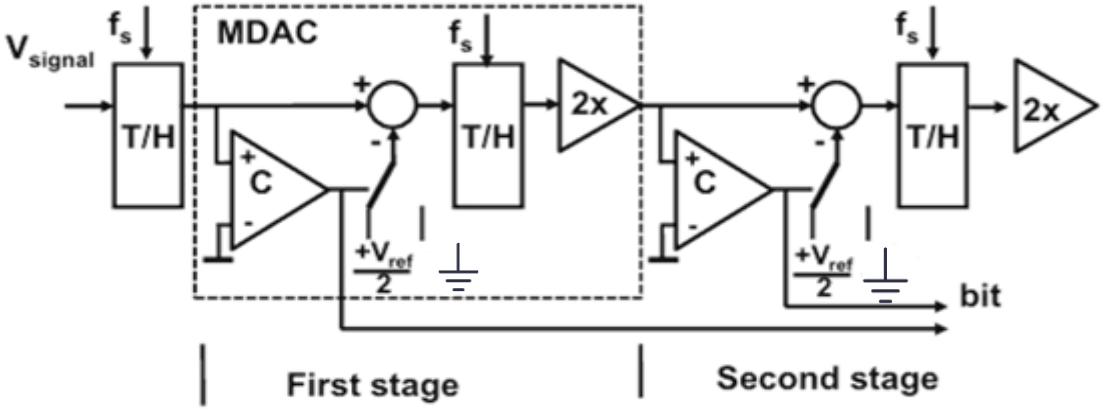
OVERVIEW OF ADC ARCHITECTURES / Pipeline

Pros:

- ✓ Speed–Resolution Trade-off
- ✓ Efficient Hardware
- ✓ Scalable Architecture

Cons:

- ❑ Latency
- ❑ Power Consumption

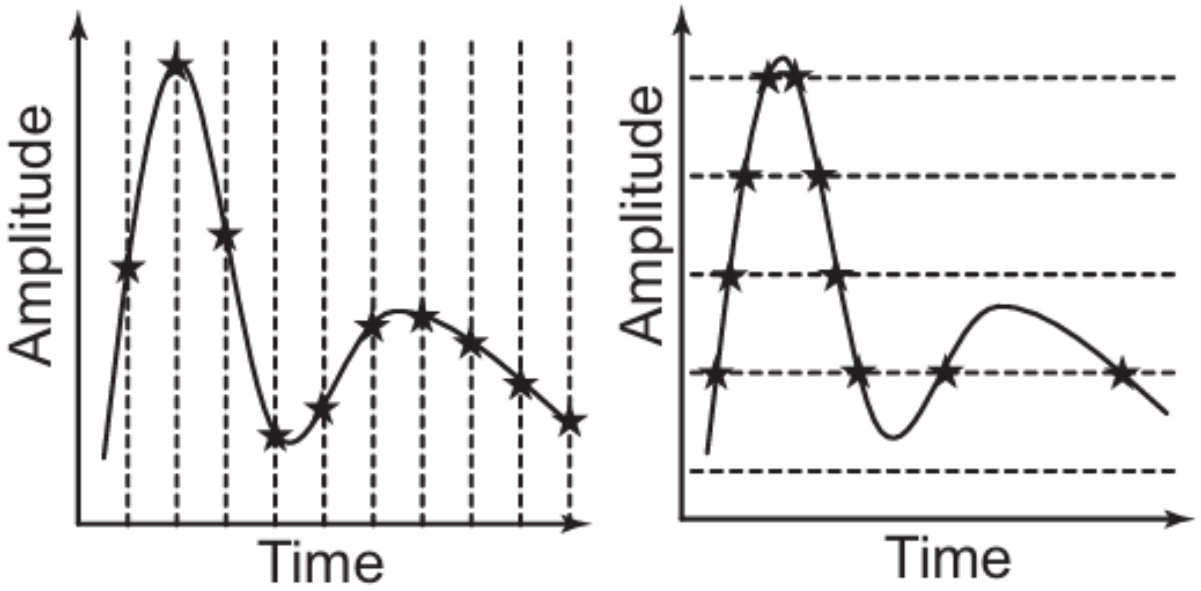


Pipeline ADC, Modified Version of [1]

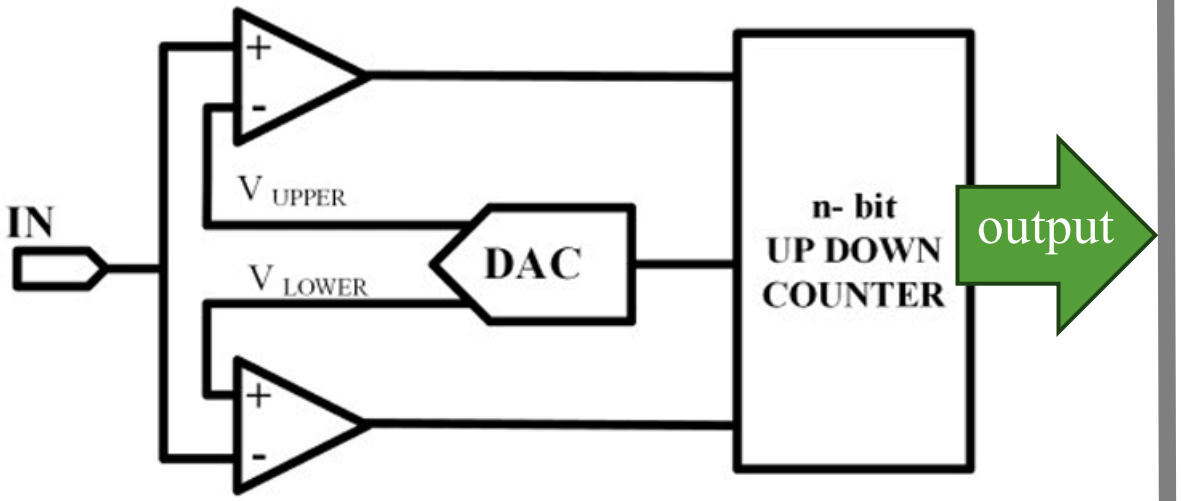
SAR ← Pipeline → Flash

[1] Marcel J.M Pelgrom, "Analog-to Digital Conversion", 4th ed. Stiphout, the Netherlands: Springer, 2021.

Synchronous VS Asynchronous ADC



Synchronous VS Asynchronous ADC [5]

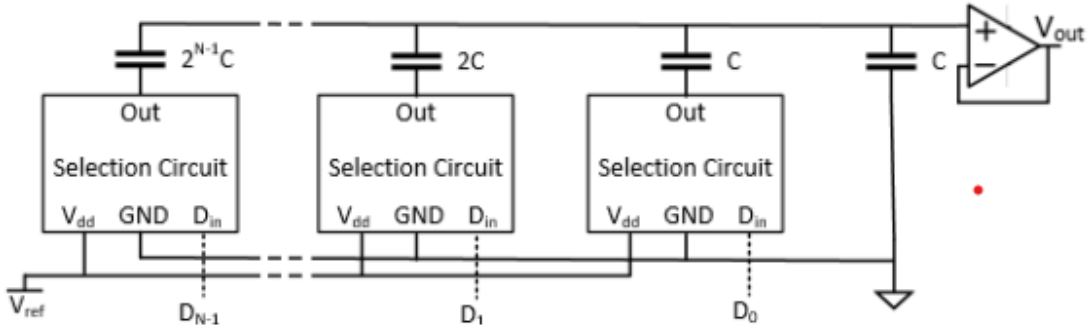


Basic architecture of Level Crossing ADC (Asynchronous) [6]

[5] Mario Renteria-Pinon, Xiaochen Tang, Jaime Ramirez-Angulo, and WEI TANG, "Fully Digital Second-order Level-crossing Sampling ADC for Data Saving in Sensing Sparse Signals," in "arXiv.", New York, USA, 2023.
[6] Sreenivasulu polineni, Anil Kumar Gupta, "8-bit Nano Watt Level Crossing ADC for Bio-Medical Application Medical Application " in "IEEE International Conference on Computer, Communication and Control", Kurukshetra, India , 2015.

Digital to Analog Converter - DAC

- High matching accuracy due to capacitor ratios
- Common in **SAR ADCs**
- Fast, low-power
- Needs precise capacitor layout (unit capacitor arrays)

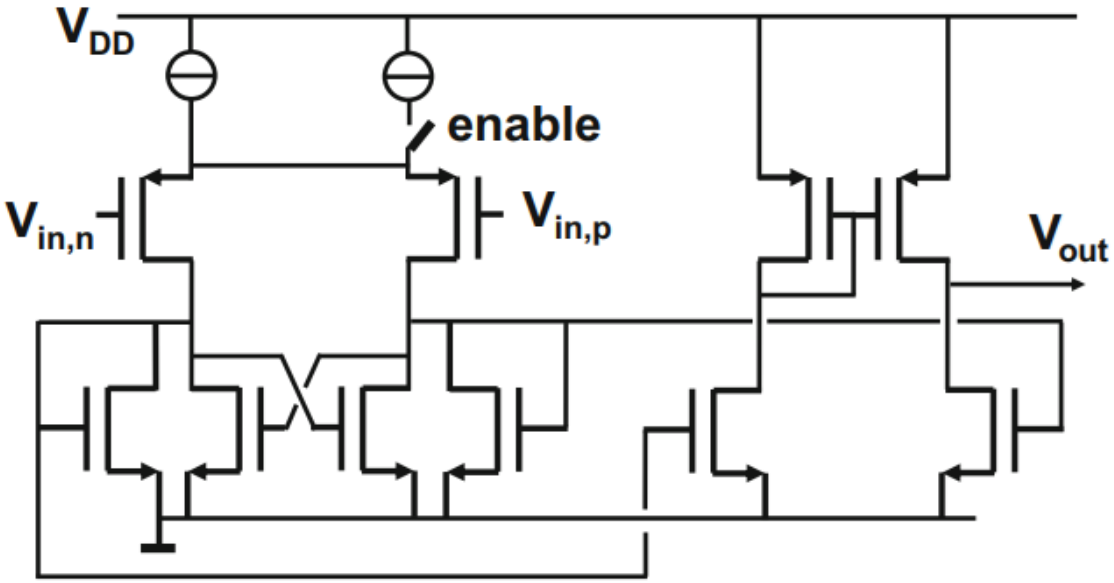


DAC Block Diagram [7]

[7] Kieren Pa, "SYNCHRONOUS LEVEL CROSSING ADC FOR BIOMEDICAL RECORDING APPLICATIONS," M.S. thesis, Department of Electrical Engineering, University of North Texas, Texas, USA, 2021.

Comparator

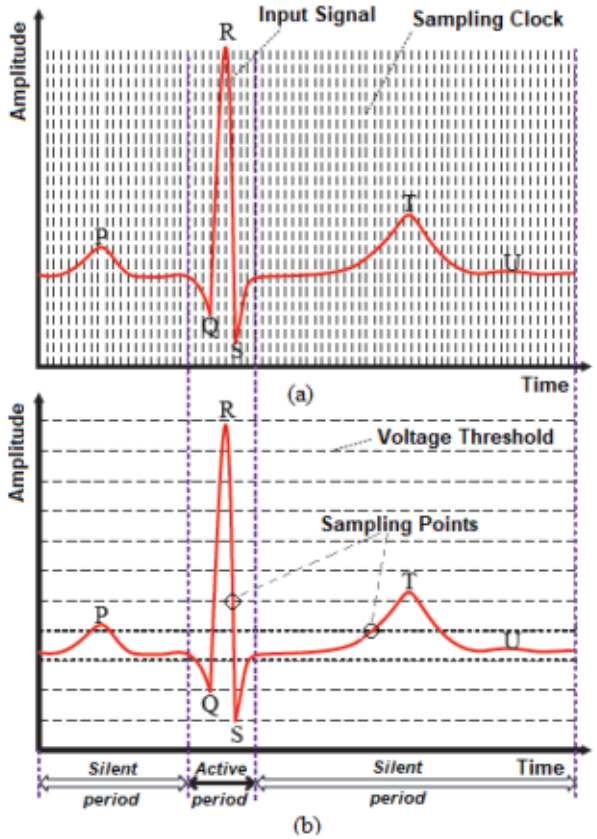
- Vin,p > Vin,n → Vout = VDD
- Vin,p < Vin,n → Vout = VSS
- Parallel NMOS → discharge & speed increase



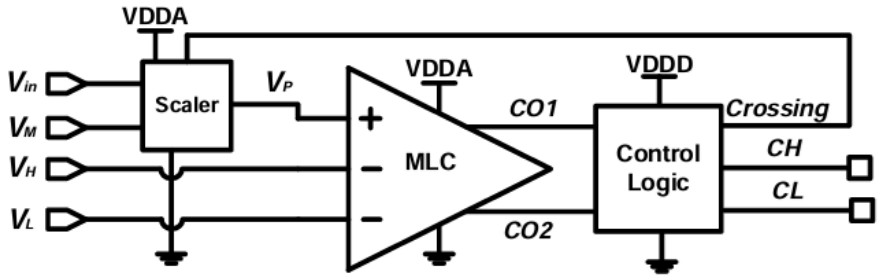
Comparator [1]

[1] Marcel J.M Pelgrom, “Analog-to Digital Conversion”, 4th ed. Stiphout, the Netherlands: Springer, 2021.

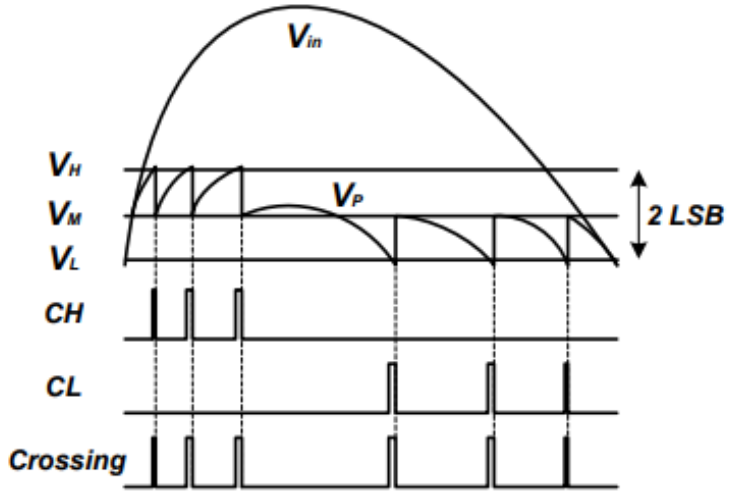
Article 1/2 [8]



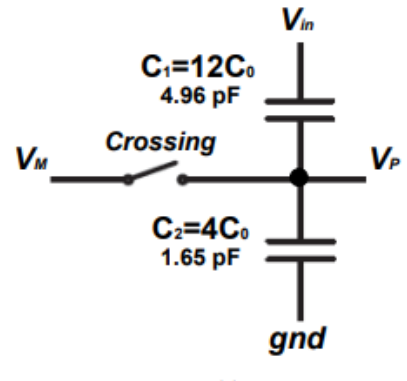
(a) Nyquist sampling
(b) Level crossing sampling.



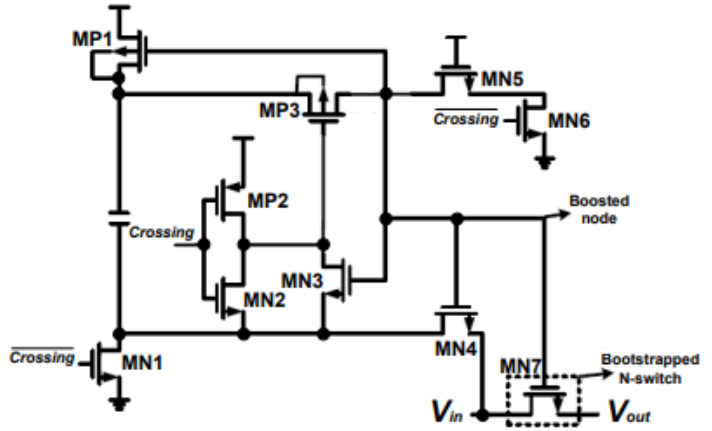
Block diagram of the proposed LC-ADC



Example waveforms.



(a)

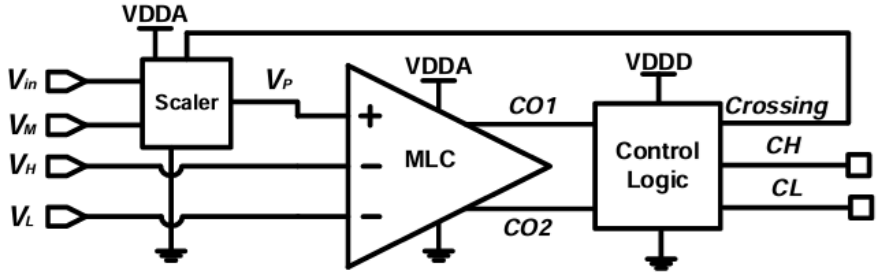


(b)

(a) The Scaler
(b) The schematic of bootstrapped switch

[8] Yuting Hou, Khalil Yousef, Mohamed Atef, Guoxing Wang, Yong Lian,"A 1-to-1-kHz, 4.2-to-544-nW, Multi-Level Comparator Based Level-Crossing ADC for IoT Applications," IEEE Transactions on Circuits and Systems II: Express Briefs Volume: 65, Issue: 10, October 2018, pp. 1390 - 1394.

Article 1/2 [8]



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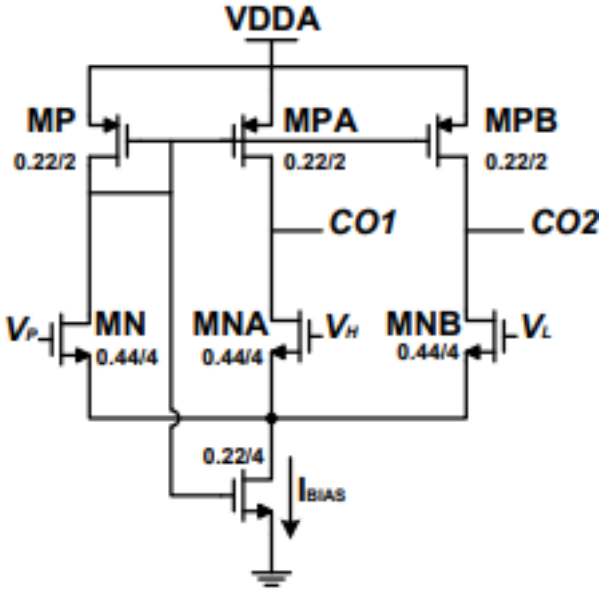
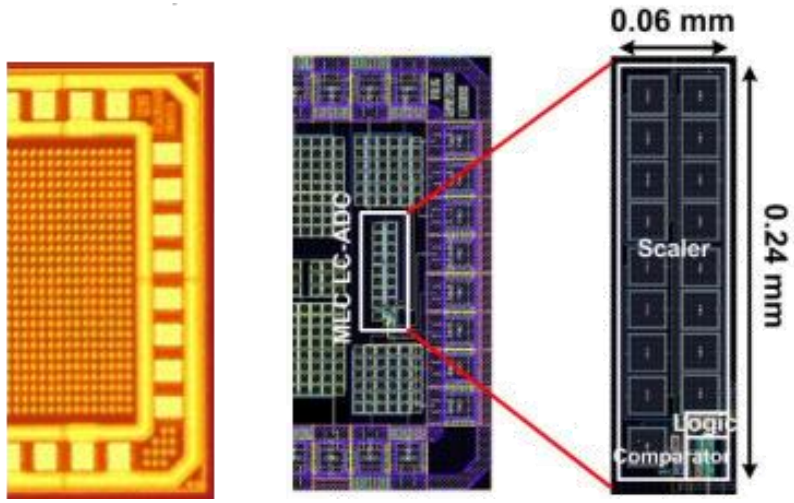


The schematic of self-biased multi-level comparator

TABLE I
MLC WORKING FUNCTION

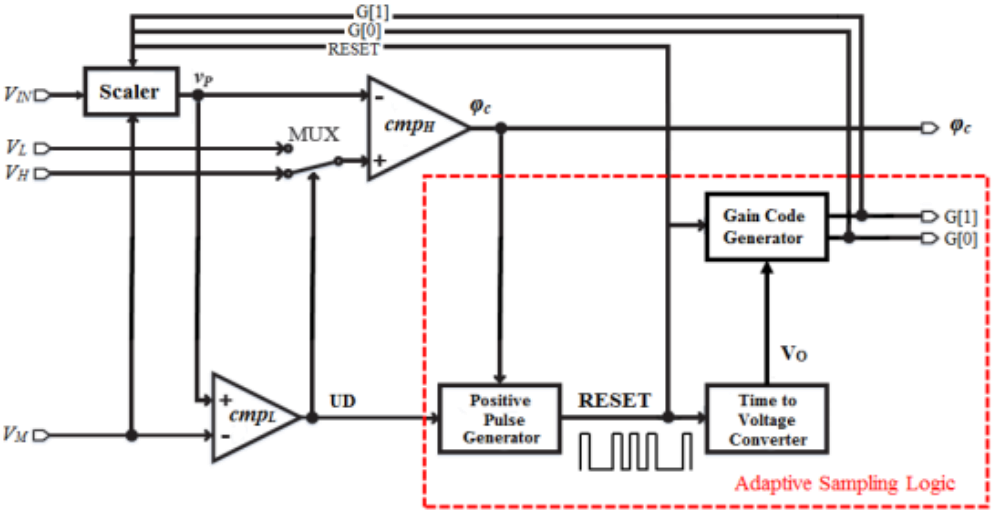
	CO1	*CO2*
$V_P > V_H$	High	High
$V_L < V_P < V_H$	Low	High
$V_P < V_L$	Low	Low



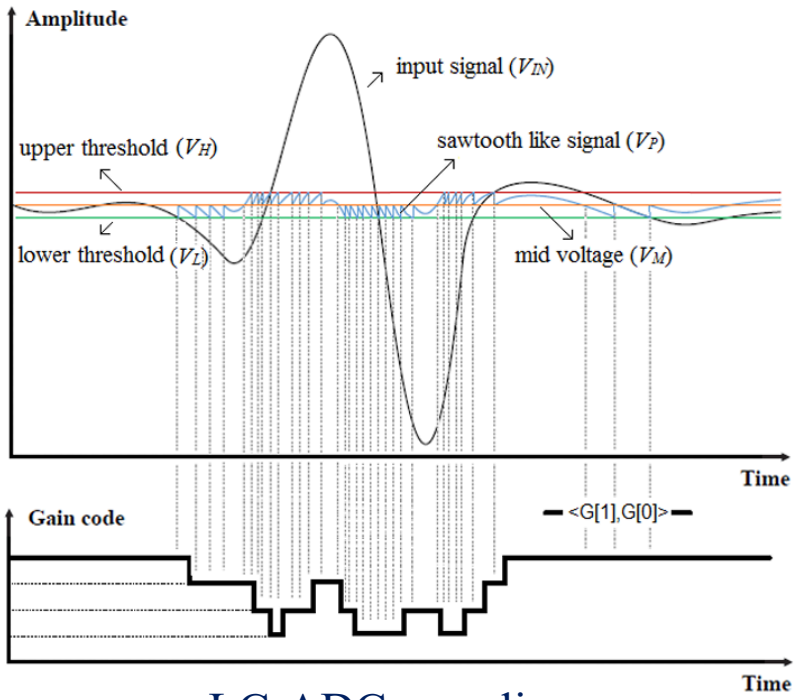
The die and layout of proposed LC-ADC (the top layer of the die is full of dummy pattern)

[8] Yuting Hou, Khalil Yousef, Mohamed Atef, Guoxing Wang, Yong Lian,"A 1-to-1-kHz, 4.2-to-544-nW, Multi-Level Comparator Based Level-Crossing ADC for IoT Applications," IEEE Transactions on Circuits and Systems II: Express Briefs (Volume: 65, Issue: 10, October 2018) , pp. 1390 - 1394.

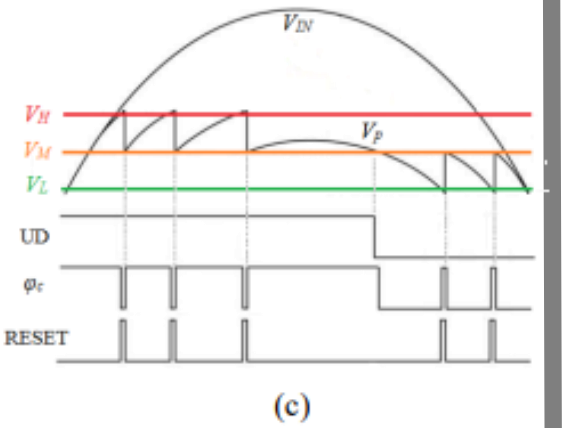
Article 2/2 [9]



Block diagram of the proposed LC-ADC



LC-ADC sampling
process and generated gain code



(c)

UD, output sampling
and RESET signals

[9] Yuting Hou, Jiali Qu, Zhenzhen Tian, Mohamed Atef, Khalil Yousef, Yong Lian, " A 61-nW Level-Crossing ADC With Adaptive Sampling for Biomedical Applications," IEEE Transactions on Circuits and Systems II: Express Briefs Volume: 66, Issue: 1, January ,2019, pp. 56 - 60.

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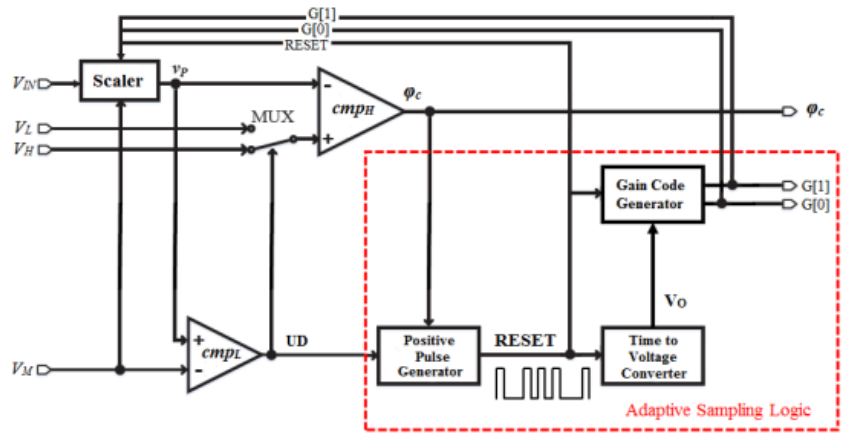
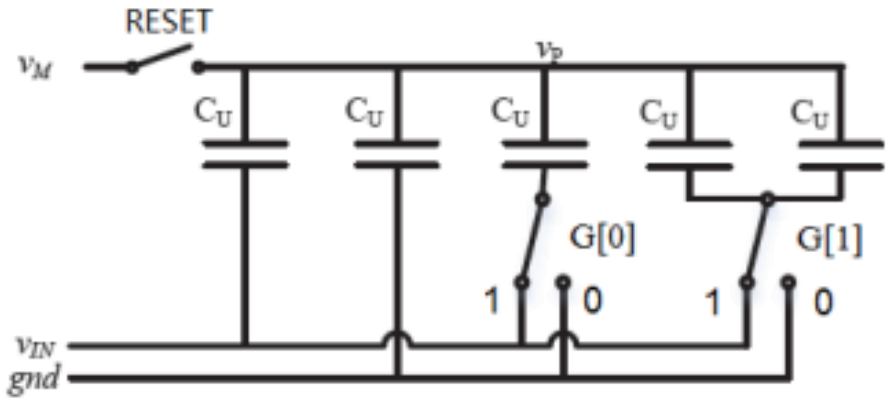
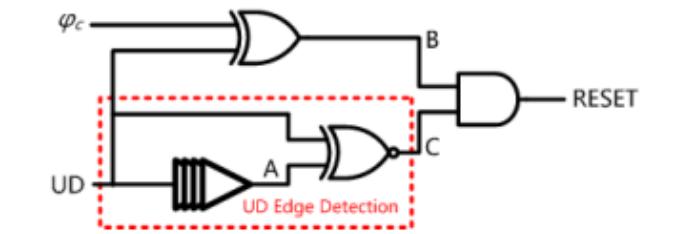
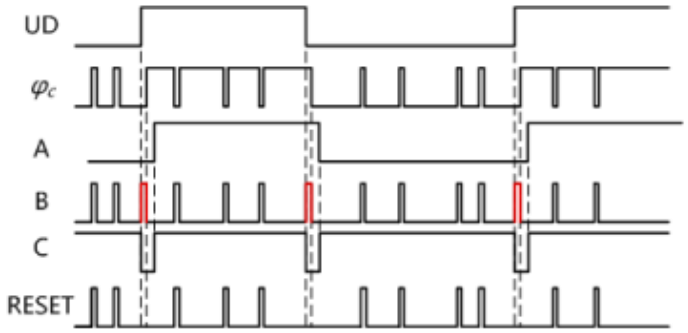




The structure of Scaler

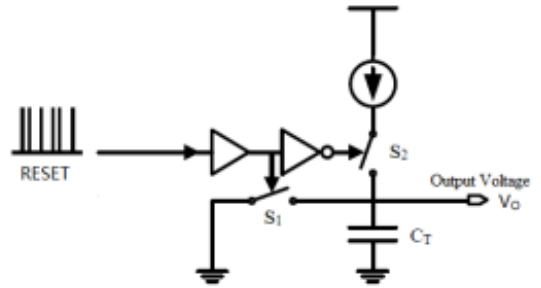


(a)



(b)

Positive Pulse Generator
(a) block diagram;
(b) transient waveforms



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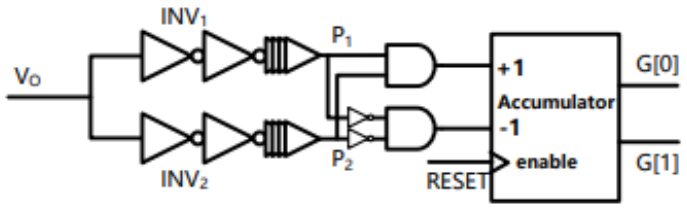
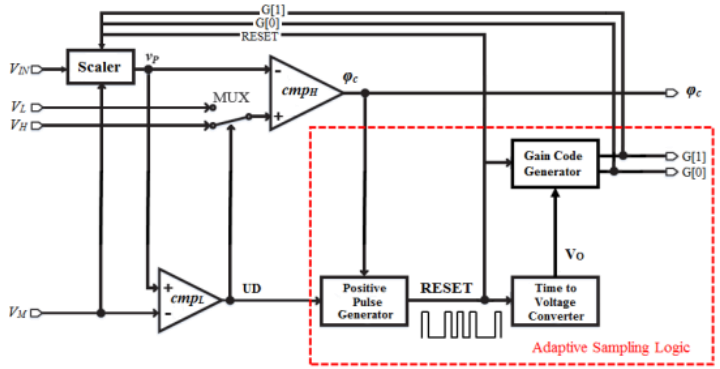


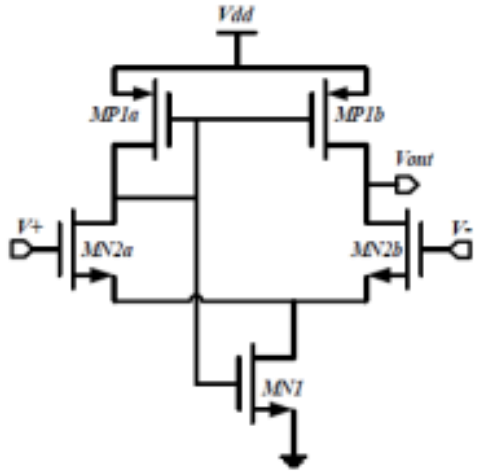
(b)

(a)The block diagram of Time to Voltage Converter;
(b) Block diagram of Gain Code Generator;

[9] Yuting Hou, Jiali Qu, Zhenzhen Tian, Mohamed Atef, Khalil Yousef, Yong Lian“ A 61-nW Level-Crossing ADC With Adaptive Sampling for Biomedical Applications," IEEE Transactions on Circuits and Systems II: Express Briefs Volume: 66, Issue: 1, January ,2019, pp. 56 - 60.

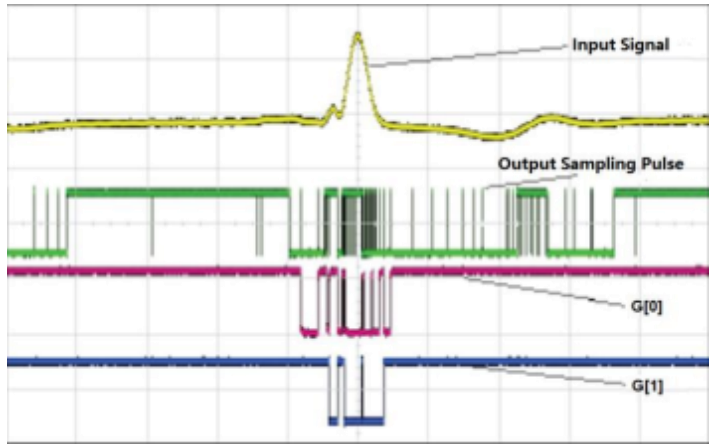
Article 2/2 [9]





The schematic of sampling window comparator

LC-ADC chip micrograph



The measured adaptive sampling method

[9] Yuting Hou, Jiali Qu, Zhenzhen Tian, Mohamed Atef, Khalil Yousef, Yong Lian“ A 61-nW Level-Crossing ADC With Adaptive Sampling for Biomedical Applications," IEEE Transactions on Circuits and Systems II: Express Briefs Volume: 66, Issue: 1, January ,2019, pp. 56 - 60.

Future Works

- Design optimized low-power comparators
- Optimize DAC circuit
- System-level validation with real signals
- Investigate ultra-low power techniques

REFERENCES

[1] Marcel J.M Pelgrom, “Analog-to Digital Conversion”, 4th ed. Stiphout, the Netherlands: Springer, 2021.

[2] Anthony Troxell , “DESIGN AND LAYOUT OF A FIXED WINDOW 6-BIT LEVEL CROSSING ANALOG-TO-DIGITAL CONVERTER,”,M.S thesis, Dept. of Electrical Eng., California State University, Spring 2023.

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Thank You For Your Attention