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Digital Logics Lab 2 due 10.30.18

3.1
BCD Digit 1: 2
BCD Digit 2: 7
T_f = 1 second

3.2

Binary Input to 7 Segment Display

Hex[0]	*Hex[1]*	*Hex[2]*	*Hex[3]*	*Hex[4]*	*Hex[5]*	*Hex[6]*	**Hexadecimal Representation of Inputs**	**Value Displayed on 7-Segment Display**
0	0	0	0	0	0	1	01	0
1	0	0	1	1	1	1	4F	1
0	0	1	0	0	1	0	12	2
0	0	0	0	1	1	0	06	3
1	0	0	1	1	0	0	4C	4
0	1	0	0	1	0	0	24	5
1	1	0	0	0	0	0	60	6
0	0	0	1	1	1	1	0F	7
0	0	0	0	0	0	0	00	8
0	0	0	1	1	0	0	0C	9
1	1	1	1	1	1	1	7F	OFF

When the BIN is set to LOW, all the outputs of the 7447 Decoder in binary will be 1, thereby resulting in the display turning OFF.

3.3
The bit size for my specific T_f value of 1 second is: 26 bits
Log_2 of 50,000,000 = 25.575 = 26 bits

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BCD-1 and BCD-2 Activation Circuit Truth Table:

D	C	B	A	Q
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

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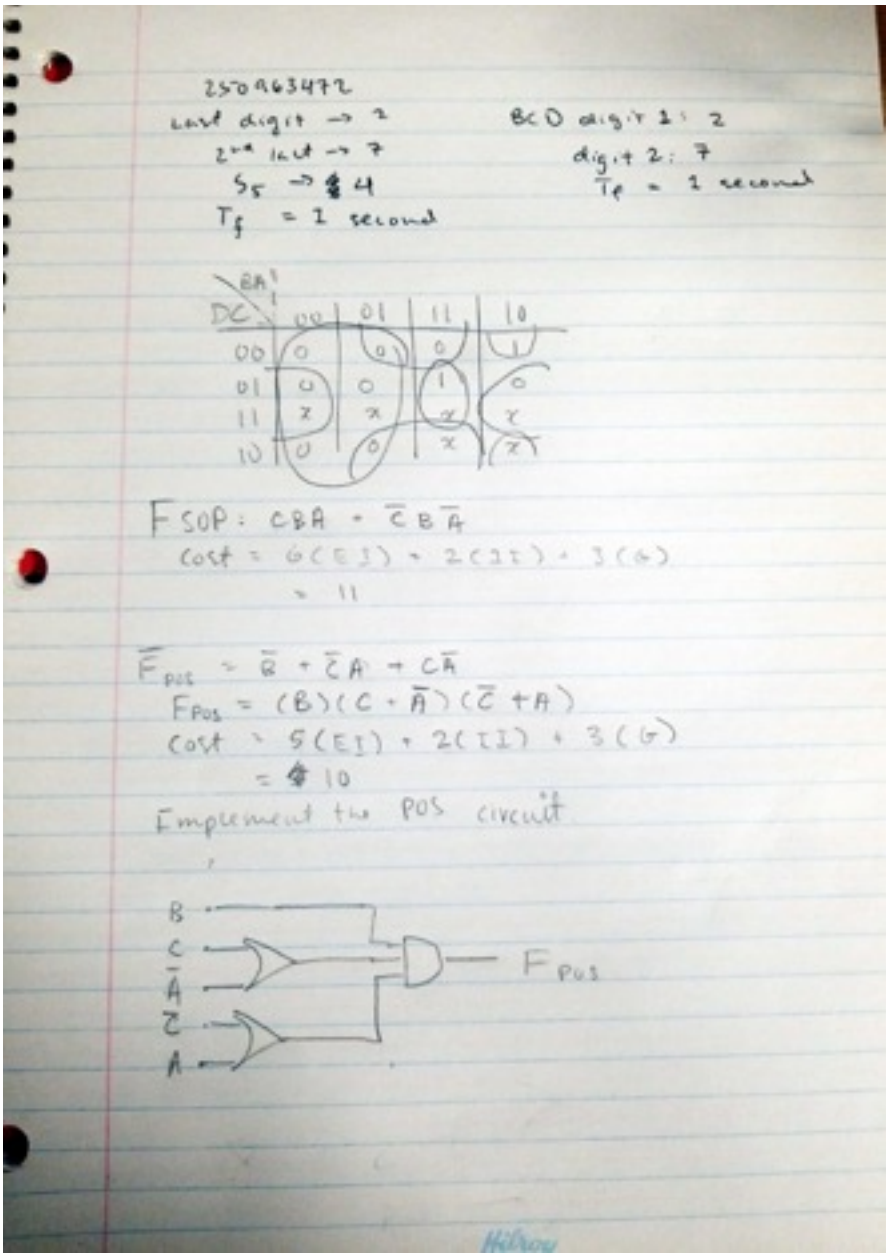
3.4

Design and calculations for BCD Activation circuit:



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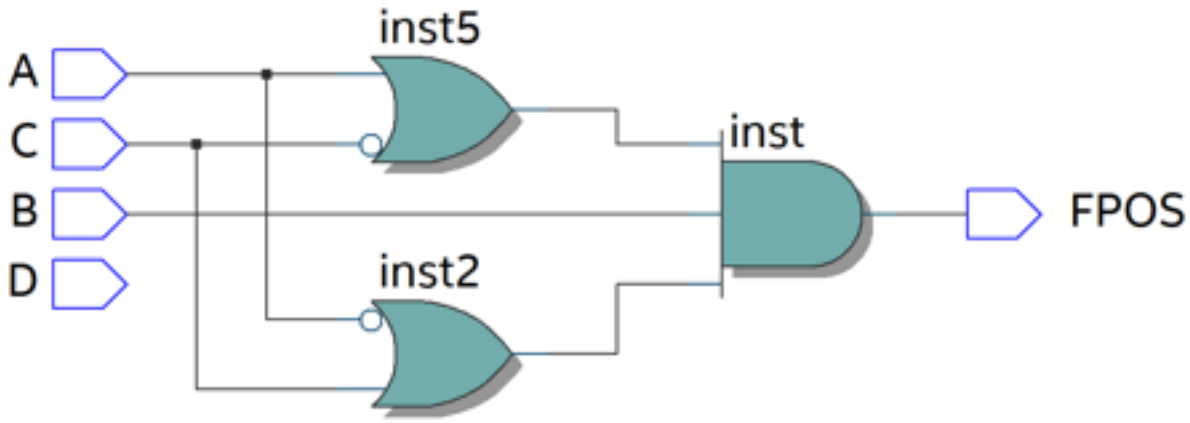
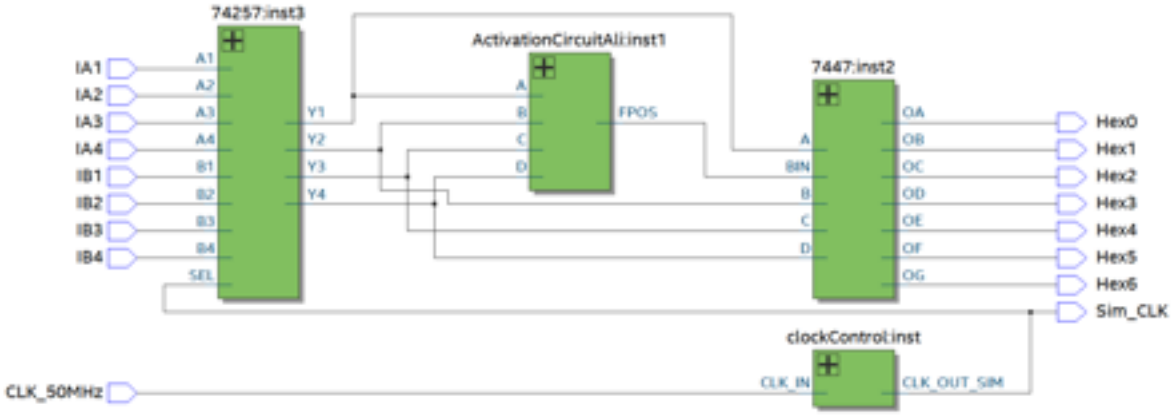
3.5 RTL Viewer:

Activation Circuit:



Full Circuit:



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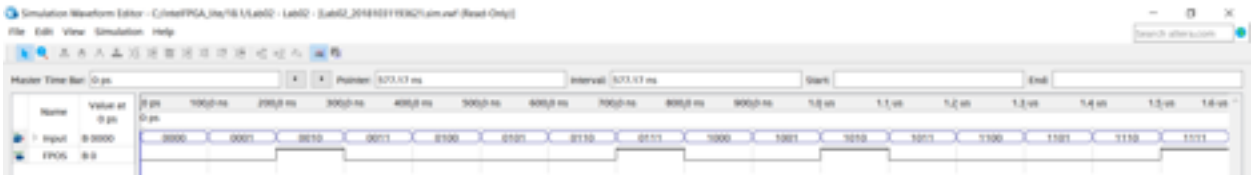
Output Simulation Results:

Activation Circuit:



The results 1010 (10) and 1111 (15) can be ignored because they are not BCD. Otherwise, 0010 (BCD: 2) and 0111 (BCD: 7) produce an output, which are the two given BCD numbers.

Final Simulation

B Constant

A Constant

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Additional Design Problem

Please note that Problem 1 and 2 have the same truth table so I combined them together. In the case of Q1, the table cuts off after 1001 because it's based off of BCD, reaching a maximum of 9. If the Q value is 0, that means the BCD value inside has an EVEN value of 1s. If the value is 1, the BCD value inside has an ODD value of 1s.

Even Parity Bit
Remember: If ABCD=0, BCD value contained is an EVEN value of 1.

A	B	C	D	Q (Q1/Q2)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X/0
1	0	1	1	X/1
1	1	0	0	X/0
1	1	0	1	X/1
1	1	1	0	X/1
1	1	1	1	X/0

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Odd Parity Bit:

A	B	C	D	Q (Q1/Q2)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

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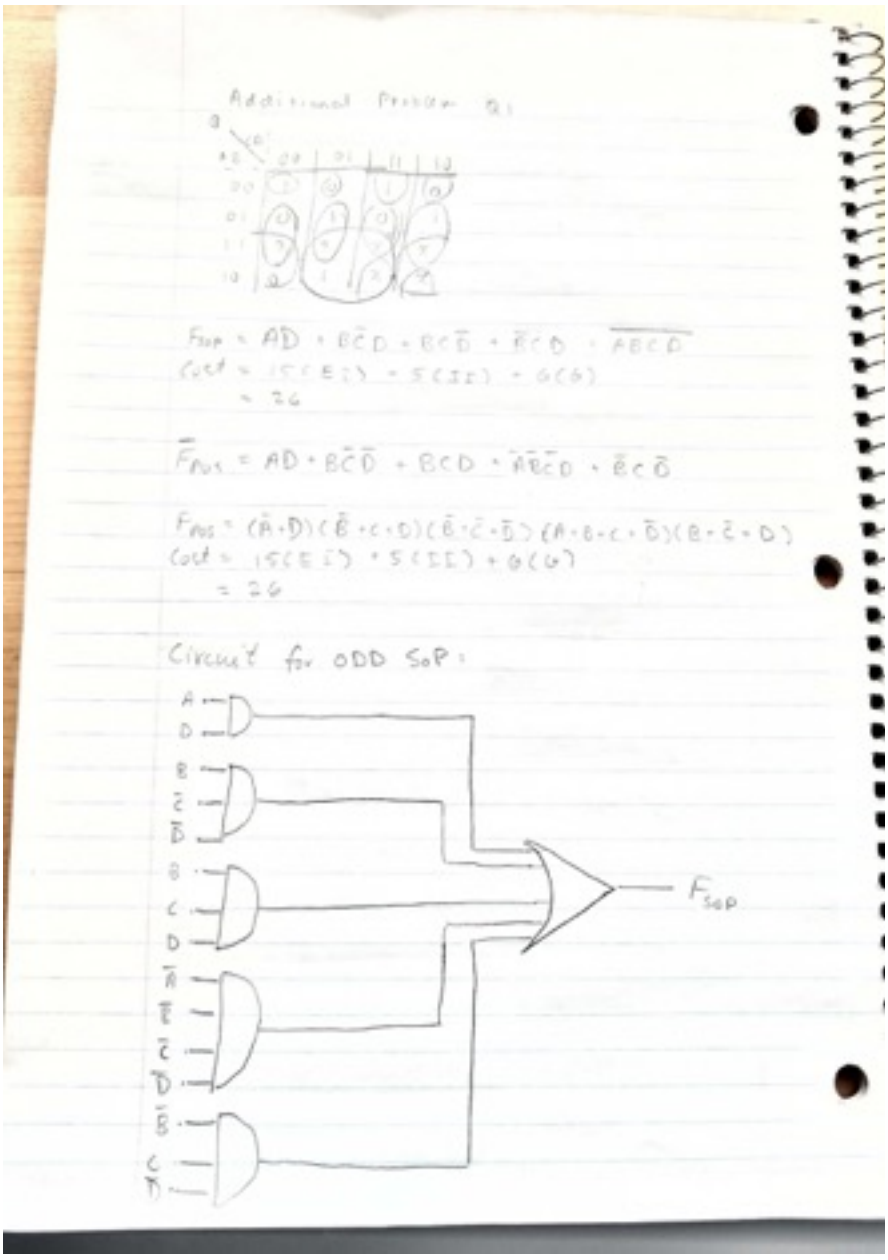
Problem 1 K-Map and Circuit:



The even and odd parity bit generators are complements of each other, meaning you only have to find one K-Map to find the costs of both. The cost will be the same for all 4 options (even SOP, odd POS, etc.), so we can choose any to implement.

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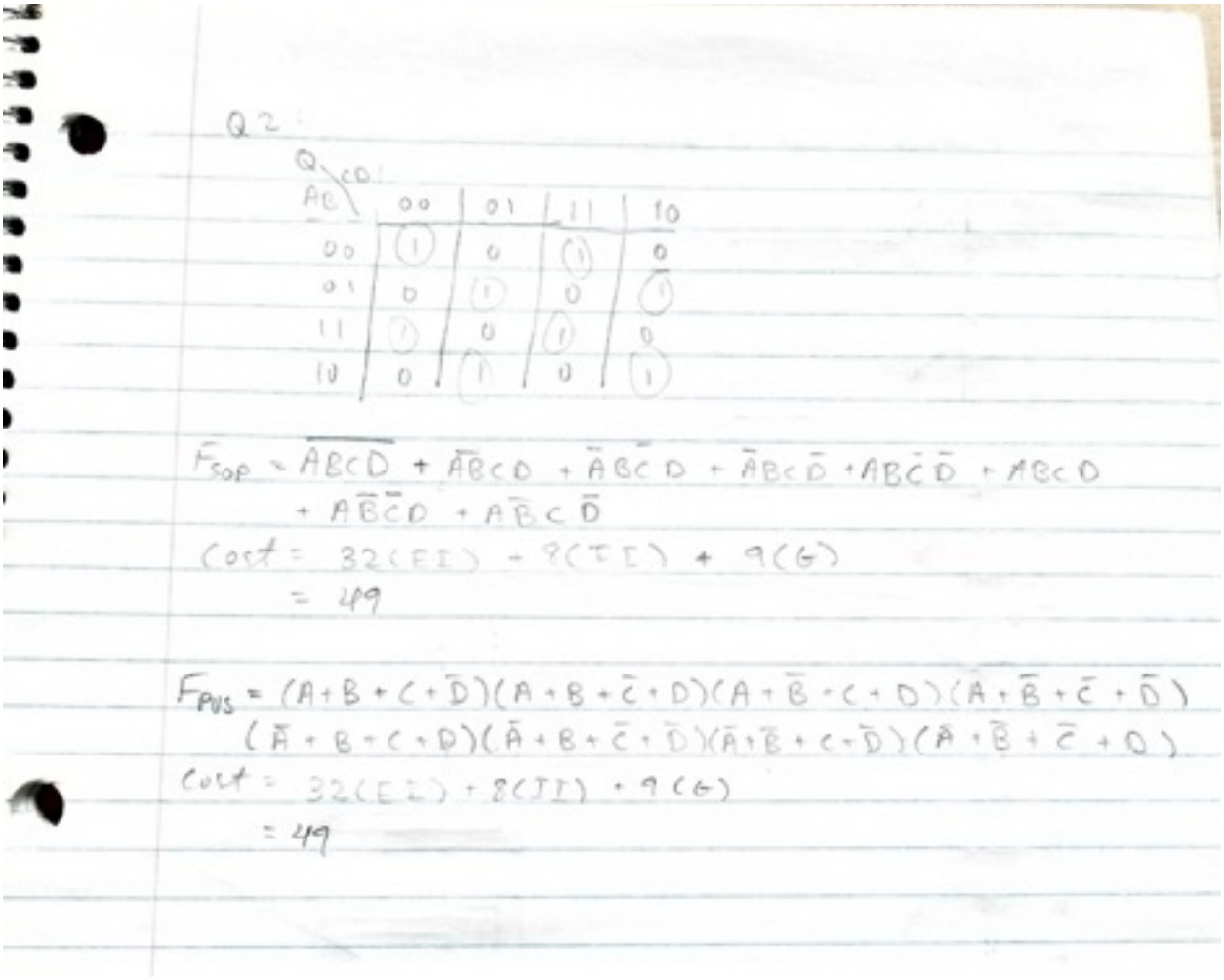
Problem 2 K-Map:



Again, the cost will be the same no matter what implementation you pick. In this case, I have chosen to implement the ODD SoP.

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Problem 2 Circuit Implementation (ODD SoP):