dnnweaver-v2.0 - [/home/hardik/workspace/vivado_projects/dnnweaver-v2.0/dnnweaver-v2.0.xpr] - Vivado 2018.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

BLOCK DESIGN - ku115 *

Sources | Design | Signals | Board

Kintex UltraScale KCU1500 Acceleration Development Bc
- External Memory (1 out of 4 connected)
  - DDR4 SDRAM C0
  - DDR4 SDRAM C1
  - DDR4 SDRAM C2
  - DDR4 SDRAM C3
- General Purpose Input or Output (0 out of 2 connect
  - DIP switches
  - User LEDs
- Miscellaneous (1 out of 3 connected)
  - IIC
  - PCI Express
  - UART

Block Interface Properties

cl_ddr0

Name: cl_ddr0

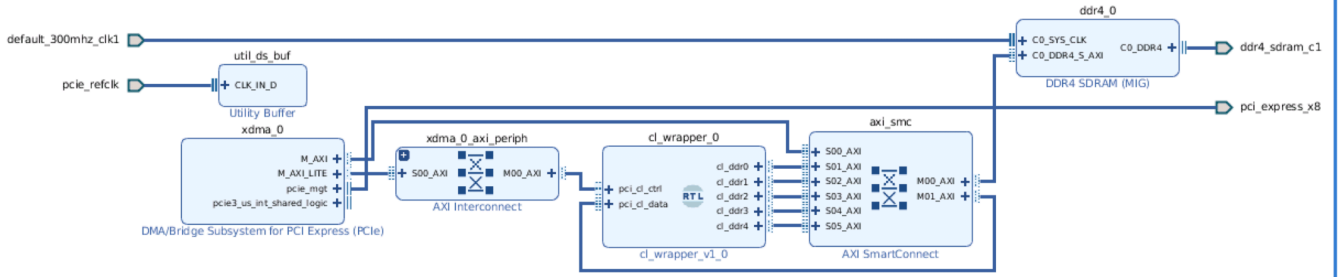
Mode: MASTER

Connection: cl_wrapper_0_cl_ddr0

Associated clock: clk

General | Properties

Diagram | Address Editor



Tcl Console | Messages | Log | Reports | Design Runs

```
apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config { Clk_master {/ddr4_0/addn_ui_clkout1 (150 MHz)} Clk_slave {/ddr4_0/c0_ddr4_ui_clk (300 MHz)} Clk_xbar {/ddr4_0/c0_ddr4_ui_clk (300 MHz)} Master {/cl_wrapper_0/cl_dd
</ddr4_0/C0_DDR4_MEMORY_MAP/C0_DDR4_ADDRESS_BLOCK> is being mapped into </cl_wrapper_0/cl_ddr3> at <0x000000000 [ 4G ]>
</cl_wrapper_0/pci_cl_data/reg0> is being mapped into </cl_wrapper_0/cl_ddr3> at <0x100000000 [ 4G ]>
apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config { Clk_master {/ddr4_0/addn_ui_clkout1 (150 MHz)} Clk_slave {/ddr4_0/c0_ddr4_ui_clk (300 MHz)} Clk_xbar {/ddr4_0/c0_ddr4_ui_clk (300 MHz)} Master {/cl_wrapper_0/cl_dd
</ddr4_0/C0_DDR4_MEMORY_MAP/C0_DDR4_ADDRESS_BLOCK> is being mapped into </cl_wrapper_0/cl_ddr4> at <0x000000000 [ 4G ]>
</cl_wrapper_0/pci_cl_data/reg0> is being mapped into </cl_wrapper_0/cl_ddr4> at <0x100000000 [ 4G ]>
endgroup
regenerate_bd_layout
regenerate_bd_layout -routing
```

Type a Tcl command here