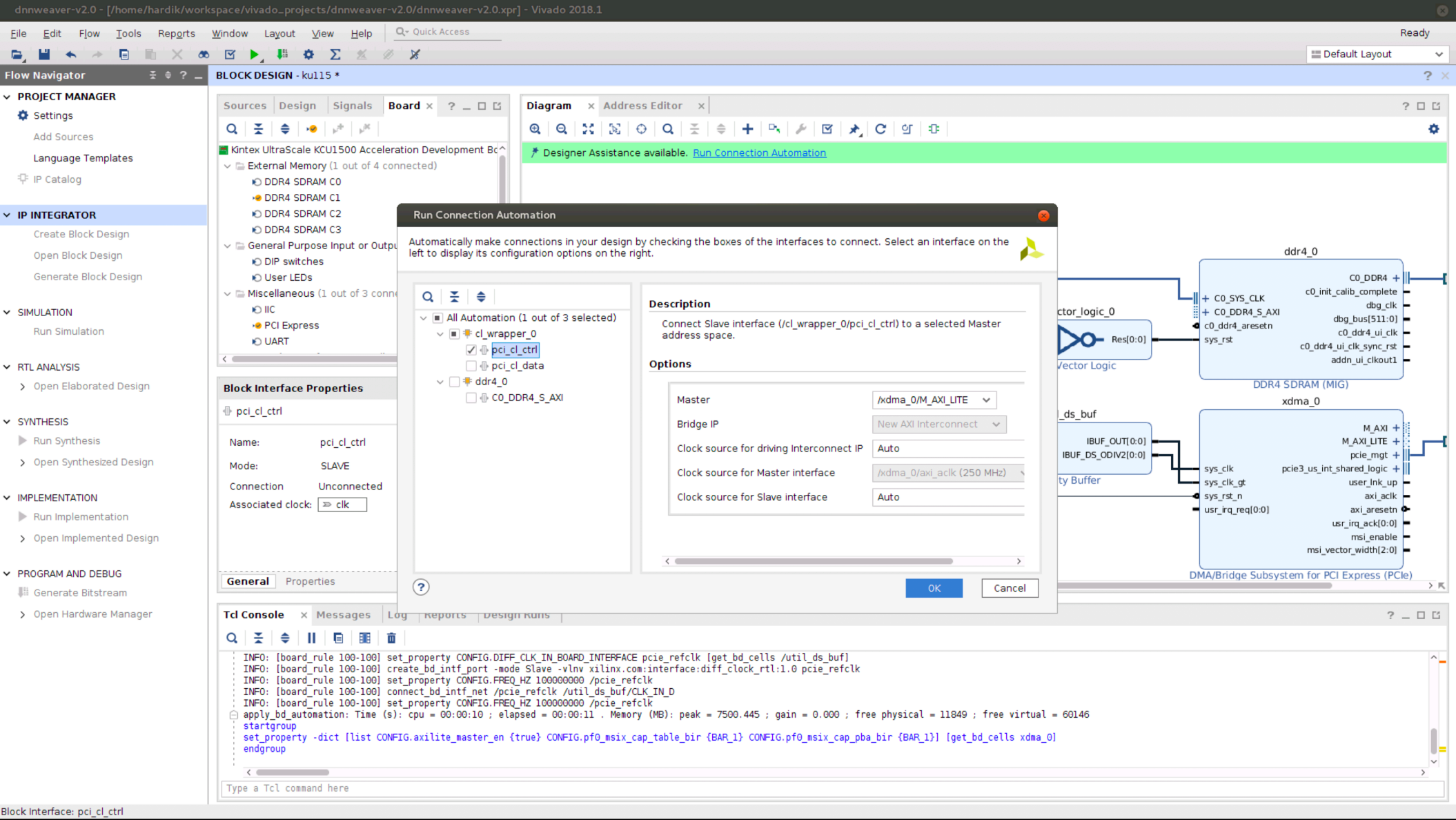
dnnweaver-v2.0 - [/home/hardik/workspace/vivado_projects/dnnweaver-v2.0/dnnweaver-v2.0.xpr] - Vivado 2018.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - ku115 *
Sources Design Signals Board
Kintex UltraScale KCU1500 Acceleration Development Bc
External Memory (1 out of 4 connected)
DDR4 SDRAM C0
DDR4 SDRAM C1
DDR4 SDRAM C2
DDR4 SDRAM C3
General Purpose Input or Outpu
DIP switches
User LEDs
Miscellaneous (1 out of 3 conne
IIC
PCI Express
UART
Block Interface Properties
pci_cl_ctrl
Name: pci_cl_ctrl
Mode: SLAVE
Connection Unconnected
Associated clock: clk
General Properties
Diagram Address Editor
Designer Assistance available. Run Connection Automation
Run Connection Automation
Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.
All Automation (1 out of 3 selected)
cl_wrapper_0
pci_cl_ctrl
pci_cl_data
ddr4_0
C0_DDR4_S_AXI
Description
Connect Slave interface (/cl_wrapper_0/pci_cl_ctrl) to a selected Master address space.
Options
Master /xdma_0/M_AXI_LITE
Bridge IP New AXI Interconnect
Clock source for driving Interconnect IP Auto
Clock source for Master interface /xdma_0/axi_aclk (250 MHz)
Clock source for Slave interface Auto
OK
Cancel
ddr4_0
C0_DDR4
c0_init_calib_complete
dbg_clk
dbg_bus[511:0]
c0_ddr4_ui_clk
c0_ddr4_ui_clk_sync_rst
addn_ui_clkout1
C0_SYS_CLK
C0_DDR4_S_AXI
c0_ddr4_aresetn
sys_rst
DDR4 SDRAM (MIG)
ctor_logic_0
Res[0:0]
Vector Logic
xdma_0
M_AXI
M_AXI_LITE
pcie_mgt
pcie3_us_int_shared_logic
user_lnk_up
axi_aclk
axi_aresetn
usr_irq_ack[0:0]
msi_enable
msi_vector_width[2:0]
sys_clk
sys_clk_gt
sys_rst_n
usr_irq_req[0:0]
DMA/Bridge Subsystem for PCI Express (PCIe)
_ds_buf
IBUF_OUT[0:0]
IBUF_DS_ODIV2[0:0]
ty Buffer
Tcl Console Messages Log Reports Design Runs
INFO: [board_rule 100-100] set_property CONFIG.DIFF_CLK_IN_BOARD_INTERFACE pcie_refclk [get_bd_cells /util_ds_buf]
INFO: [board_rule 100-100] create_bd_intf_port -mode Slave -vlnv xilinx.com:interface:diff_clock_rtl:1.0 pcie_refclk
INFO: [board_rule 100-100] set_property CONFIG.FREQ_HZ 100000000 /pcie_refclk
INFO: [board_rule 100-100] connect_bd_intf_net /pcie_refclk /util_ds_buf/CLK_IN_D
INFO: [board_rule 100-100] set_property CONFIG.FREQ_HZ 100000000 /pcie_refclk
apply_bd_automation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:11 . Memory (MB): peak = 7500.445 ; gain = 0.000 ; free physical = 11849 ; free virtual = 60146
startgroup
set_property -dict [list CONFIG.axilite_master_en {true} CONFIG.pf0_msix_cap_table_bir {BAR_1} CONFIG.pf0_msix_cap_pba_bir {BAR_1}] [get_bd_cells xdma_0]
endgroup
Type a Tcl command here
Block Interface: pci_cl_ctrl