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Sources | **Design** | **Signals** | **Board**

Kintex UltraScale KCU1500 Acceleration Development Board

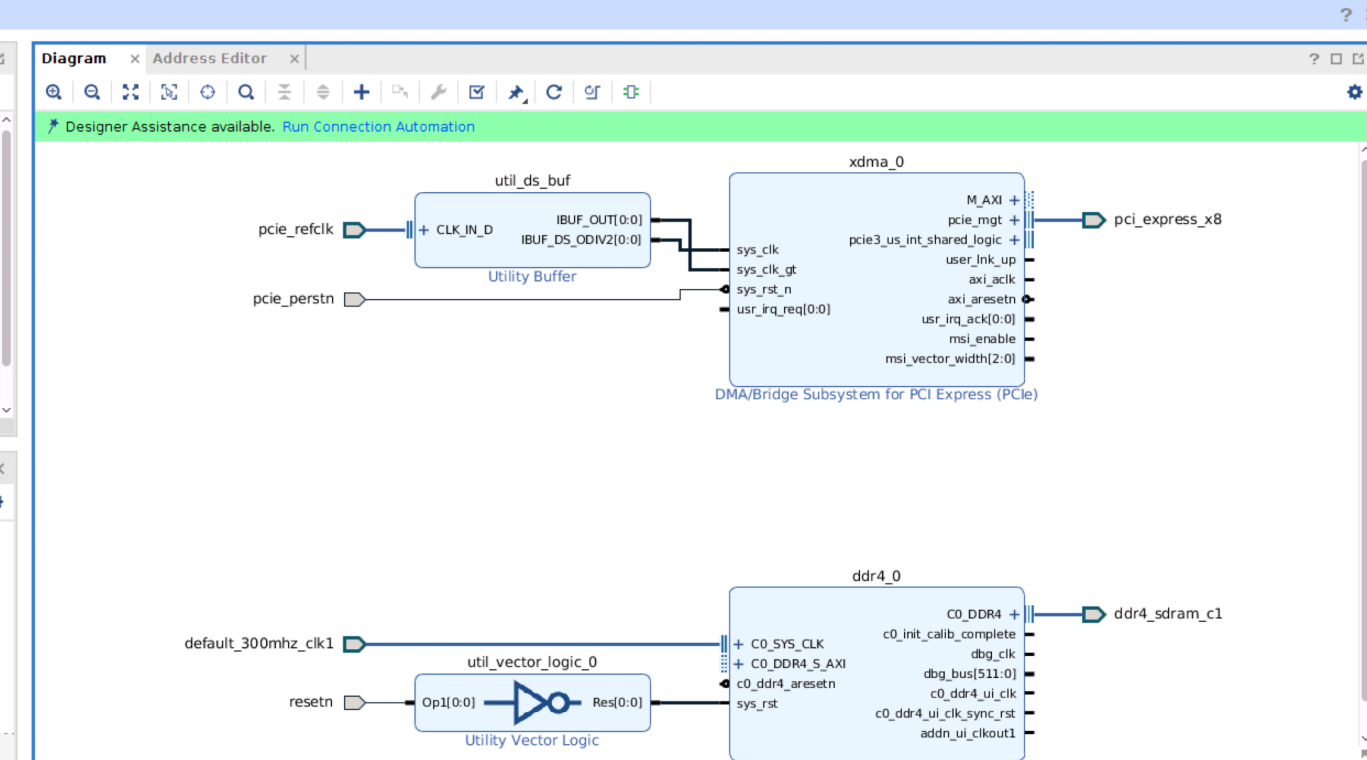
- External Memory (1 out of 4 connected)
 - DDR4 SDRAM C0
 - DDR4 SDRAM C1
 - DDR4 SDRAM C2
 - DDR4 SDRAM C3
- General Purpose Input or Output (0 out of 2 connected)
 - DIP switches
 - User LEDs
- Miscellaneous (1 out of 3 connected)
 - IIC
 - PCI Express
 - UART

Block Properties

Name: xdma_0

Parent name: ku115

General | Properties | IP



Tcl Console | Messages | Log | Reports | Design Runs

```

endgroup
apply_bd_automation -rule xilinx.com:bd_rule:xdma -config {auto_level "IP Level" lane_width "X8" link_speed "8.0 GT/s (PCIe Gen 3)" axi_clk "Maximum Data Width" axi_intf "AXI Memory Mapped" bar_size "Disable" bypass_size "C
INFO: [board_rule 100-100] set_property CONFIG.USE_BOARD_FLOW true [get_bd_cells /util_ds_buf]
INFO: [board_rule 100-100] set_property CONFIG.DIFF_CLK_IN_BOARD_INTERFACE pcie_refclk [get_bd_cells /util_ds_buf]
INFO: [board_rule 100-100] create_bd_intf_port -mode Slave -vlnv xilinx.com:interface:diff_clock_rtl:1.0 pcie_refclk
INFO: [board_rule 100-100] set_property CONFIG.FREQ_HZ 1000000000 /pcie_refclk
INFO: [board_rule 100-100] connect_bd_intf_net /pcie_refclk /util_ds_buf/CLK_IN_D
INFO: [board_rule 100-100] set_property CONFIG.FREQ_HZ 1000000000 /pcie_refclk
apply_bd_automation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 8000.602 ; gain = 0.000 ; free physical = 11577 ; free virtual = 59869
    
```

Type a Tcl command here