dnnweaver-v2.0 - [/home/hardik/workspace/vivado_projects/dnnweaver-v2.0/dnnweaver-v2.0.xpr] - Vivado 2018.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

BLOCK DESIGN - ku115 *

Sources Design Signals Board

Kintex UltraScale KCU1500 Acceleration Development Bc
- External Memory (1 out of 4 connected)
  - DDR4 SDRAM C0
  - DDR4 SDRAM C1
  - DDR4 SDRAM C2
  - DDR4 SDRAM C3
- General Purpose Input or Output (0 out of 2 connect
  - DIP switches
  - User LEDs
- Miscellaneous (0 out of 3 connected)
  - IIC
  - PCI Express
  - UART

System Net Properties

util_vector_logic_0_Res

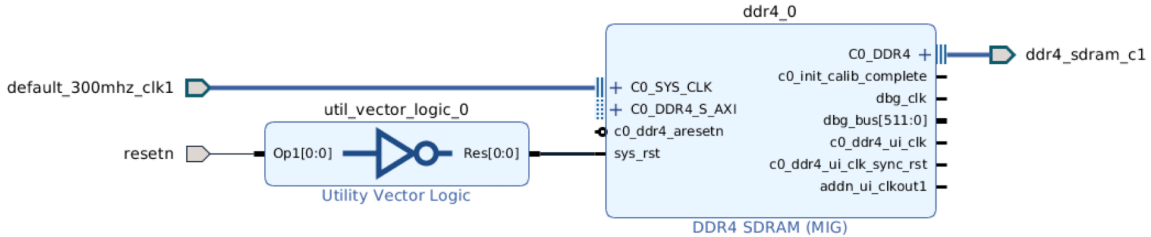
Name: l_vector_logic_0_Res

Parent name: ku115

Driver: util_vector_logic_0/Res

General Properties Pins

Diagram



Tcl Console Messages Log Reports Design Runs

```
INFO: [board_interface 100-100] connect_bd_net /resetn /ddr4_0/sys_rst
INFO: [board_interface 100-100] set_property CONFIG.POLARITY ACTIVE_LOW /resetn
delete_bd_objs [get_bd_nets resetn_1]
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:util_vector_logic:2.0 util_vector_logic_0
endgroup
set_property -dict [list CONFIG.C_SIZE {1} CONFIG.C_OPERATION {not} CONFIG.LOGO_FILE {data/sym_notgate.png}] [get_bd_cells util_vector_logic_0]
connect_bd_net [get_bd_ports resetn] [get_bd_pins util_vector_logic_0/Op1]
connect_bd_net [get_bd_pins util_vector_logic_0/Res] [get_bd_pins ddr4_0/sys_rst]
```

Type a Tcl command here