

## Flow Navigator

## PROJECT MANAGER



Add Sources

Language Templates



IP Catalog

## IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

## SIMULATION

Run Simulation

## RTL ANALYSIS

&gt; Open Elaborated Design

## SYNTHESIS

▶ Run Synthesis

&gt; Open Synthesized Design

## IMPLEMENTATION

▶ Run Implementation

&gt; Open Implemented Design

## PROGRAM AND DEBUG

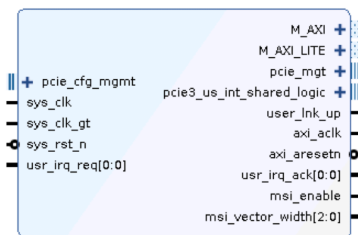
▶ Generate Bitstream

&gt; Open Hardware Manager

## Re-customize IP

## DMA/Bridge Subsystem for PCI Express (PCIe) (4.1)

Documentation IP Location

☐ Show disabled ports

Component Name xdma\_0

Board Basic PCIe ID PCIe : BARs PCIe : MISC PCIe : DMA

☒ PCIe to AXI Lite Master Interface☐ 64bit Enable☐ Prefetchable

Size 4

Scale Kilobytes

Value FFFFFFF00

PCIe to AXI Translation 0x00000000

☒ PCIe to DMA Interface☐ 64bit Enable☐ Prefetchable☐ PCIe to DMA Bypass Interface☐ 64bit Enable☐ Prefetchable

Size 1

Scale Megaby...

Value FFF00000

PCIe to AXI Translation 0x0000000000000000

OK

Cancel

Type a Tcl command here

Ready

Default Layout

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