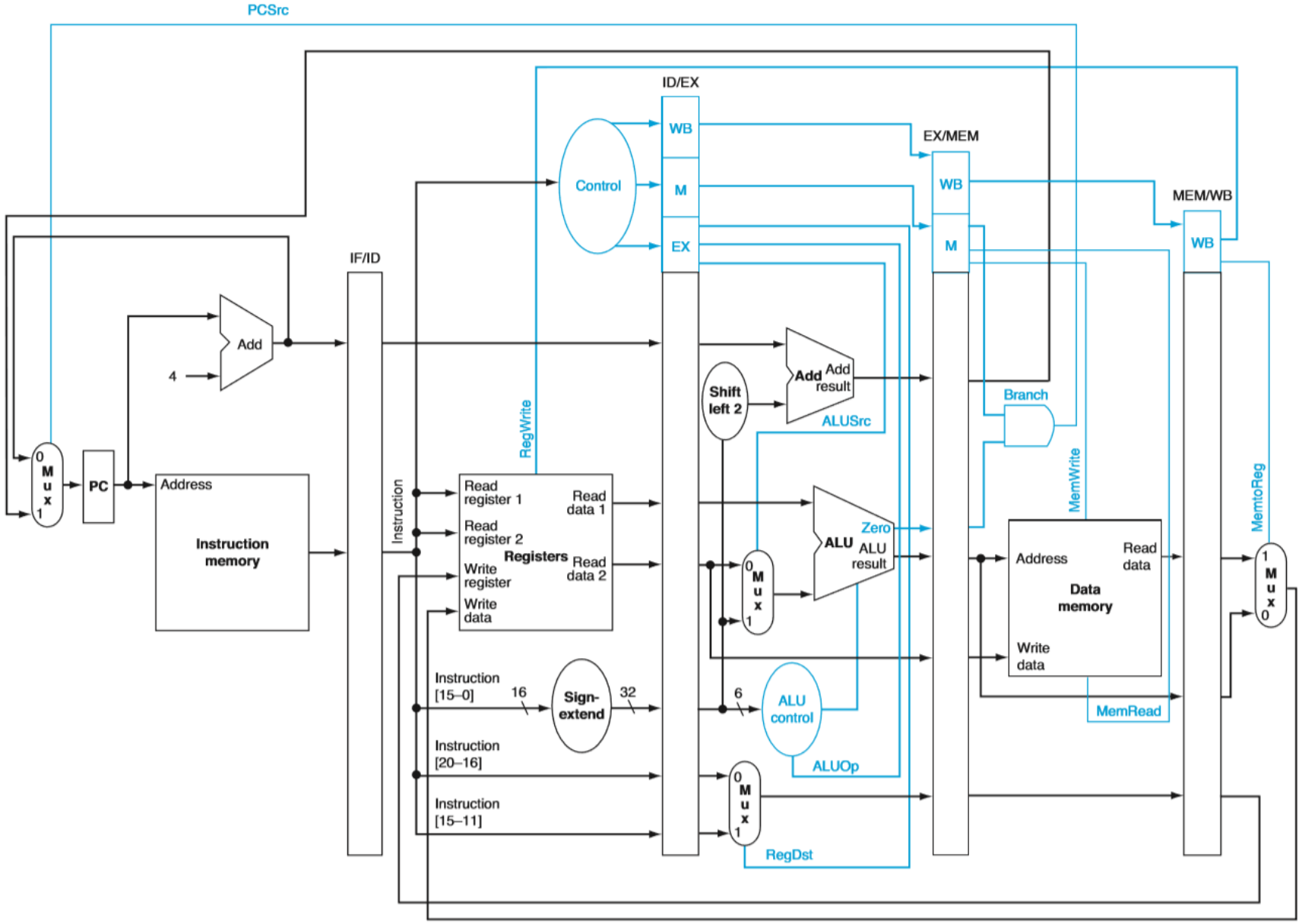
IN THE NAME OF GOD

Architecture Lab Description, Session #6

Session Abstract

- Implementing Control Unit Stage
- Assembling CPU
  - Use instantiation and wiring
- Creating test bench and testing it

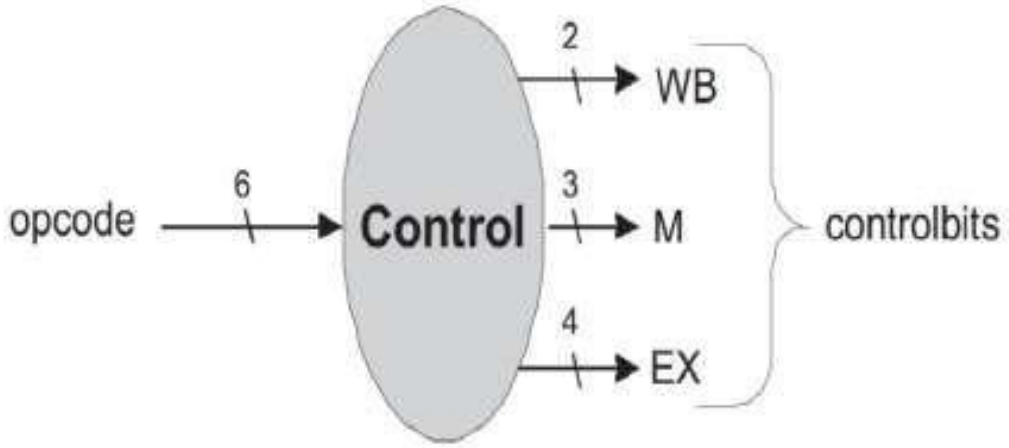
MIPS Data Path



Control Unit I/O

- Inputs:
  - Instruction
- Outputs
  - 2-bit for WriteBack module(MemToReg and RegWrite)
  - 3-bit for Memory module(Branch, MemRead and MemWrite)
  - 4-bit for Execute module(ALU source, RegDest and 2-bit ALUop)

Control Unit Stage



Implement CU using codes in table below

OpCode	Func	rf_write_en	rf_wb_addr_sel	alu_srcb_sel	mem_write_en	branch	rf_write_data_sel	pcsrc
000000	??????	1	1	0	0	0	1	3
000000	001000 (jr)	0						1
000000	001001 (jalr)		2				2	1
001???	??????	1	0	1	0	0	1	3
0001??	??????	0	?	0	0	Ins[26:26]	?	0
000010	??????	0	?	?	0	?	?	2
000011	??????	1	2	?	0	?	?	2
100011	??????	1	0	1	0	?	0	3

END!