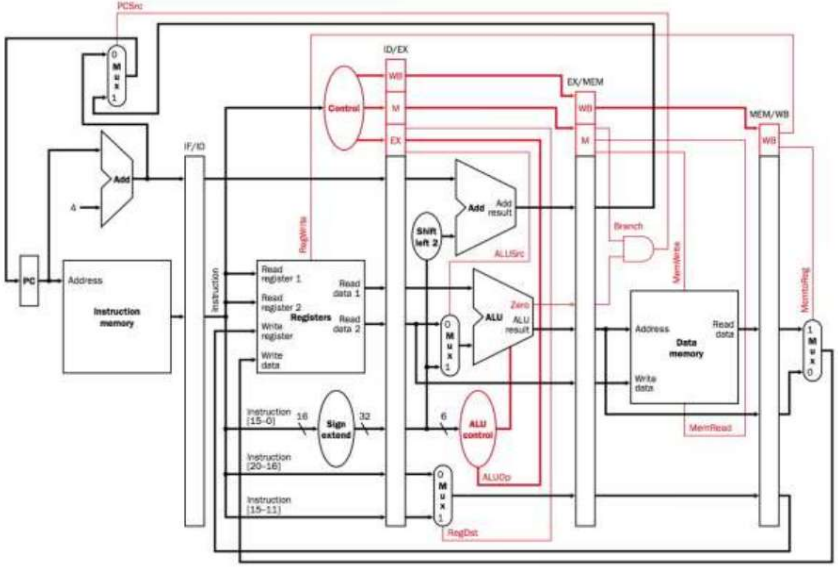
IN THE NAME OF GOD

Architecture Lab Description, Session #1

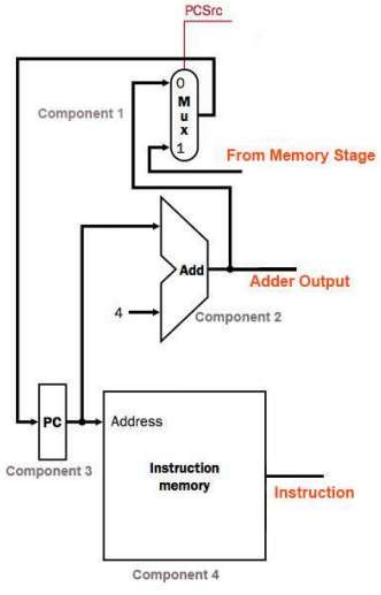
Session Abstract

- Introduction to course
- Implementing Instruction Fetch Pipe Stage
- Testing it

MIPS Datapath



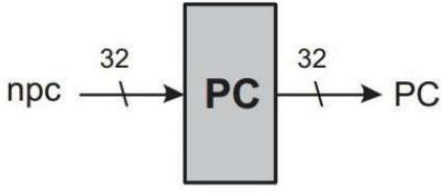
Instruction Fetch Pipeline



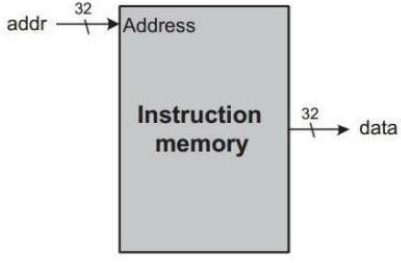
Fetch Pipe I/O

- Inputs:
  - PCSrc
  - Mux-1, From Memory Stage
- Outputs
  - Adder Output
  - Instruction

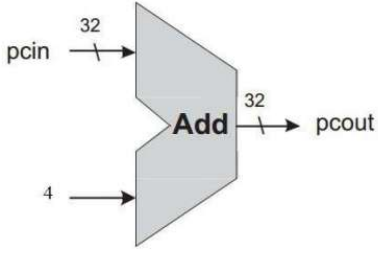
Module: PC



Module: Instruction Memory



Module: Increment By 4



Module: 2 to 1, 32 bit Multiplexer