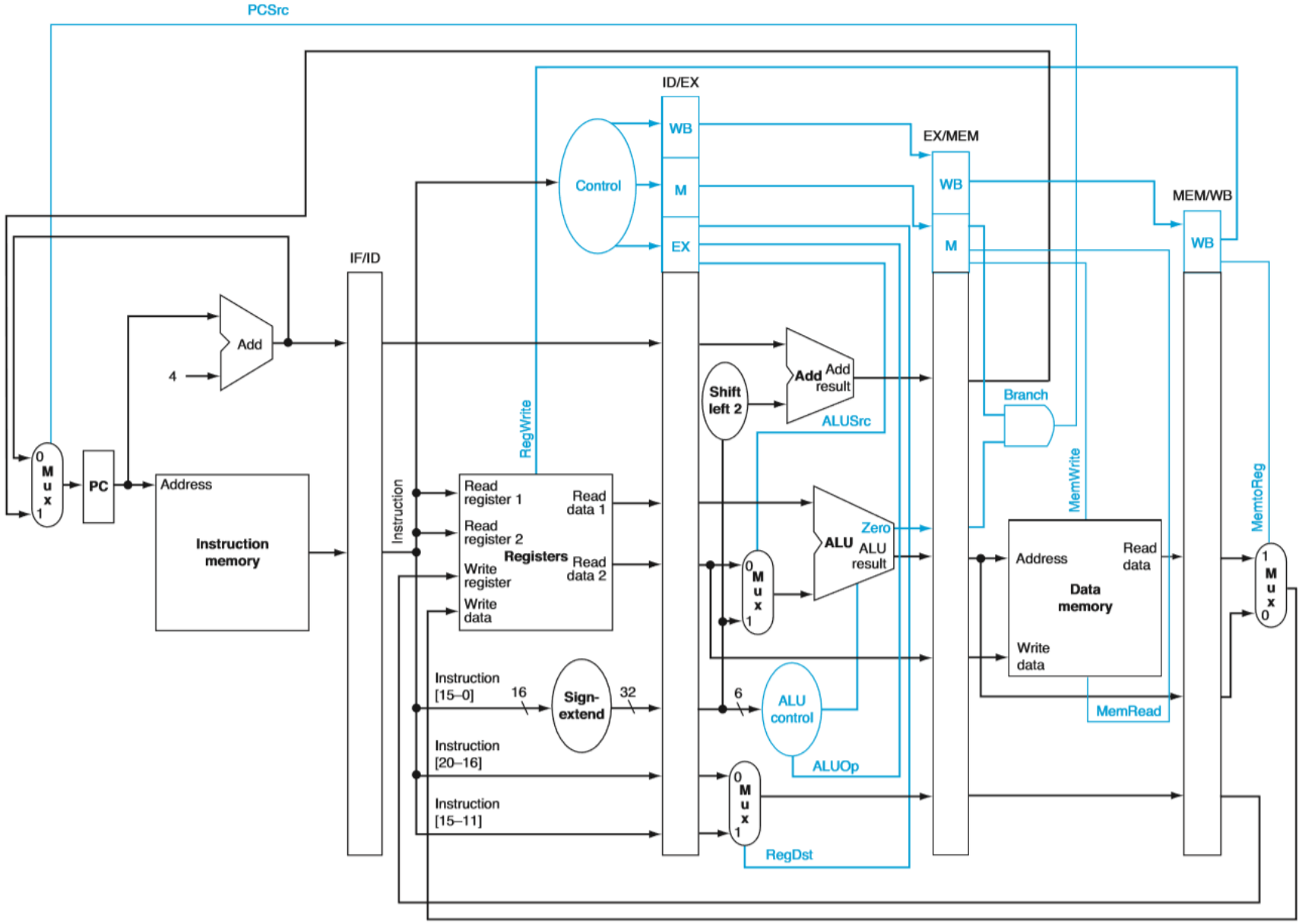
IN THE NAME OF GOD

Architecture Lab Description, Session #5

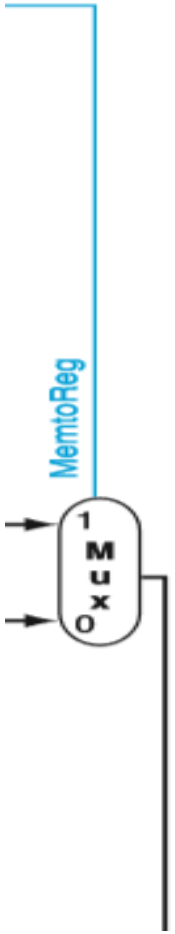
Session Abstract

- Implementing Writeback Pipe Stage and pipeline registers
- Creating test bench and testing it

MIPS DataPath



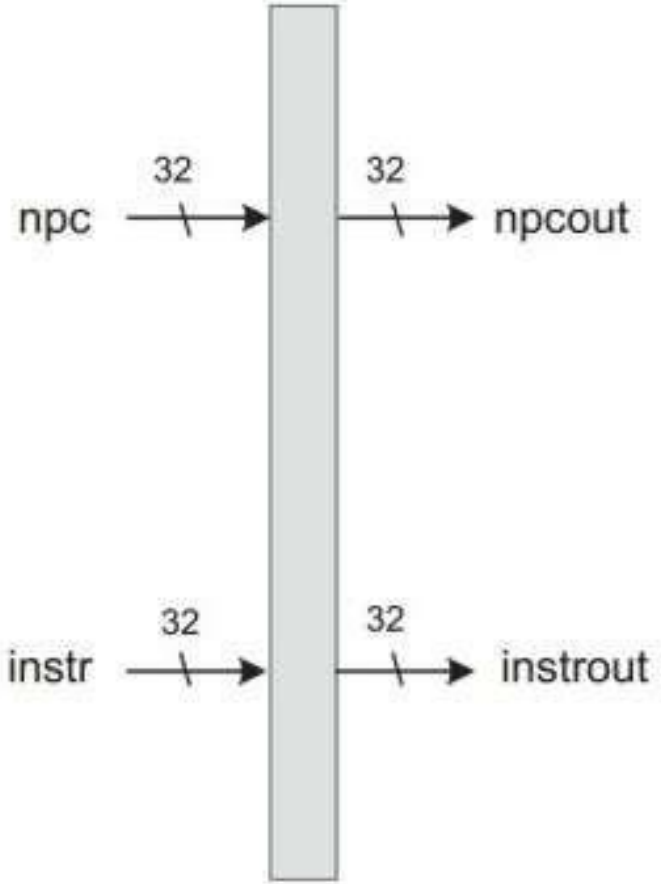
Instruction Writeback Pipe



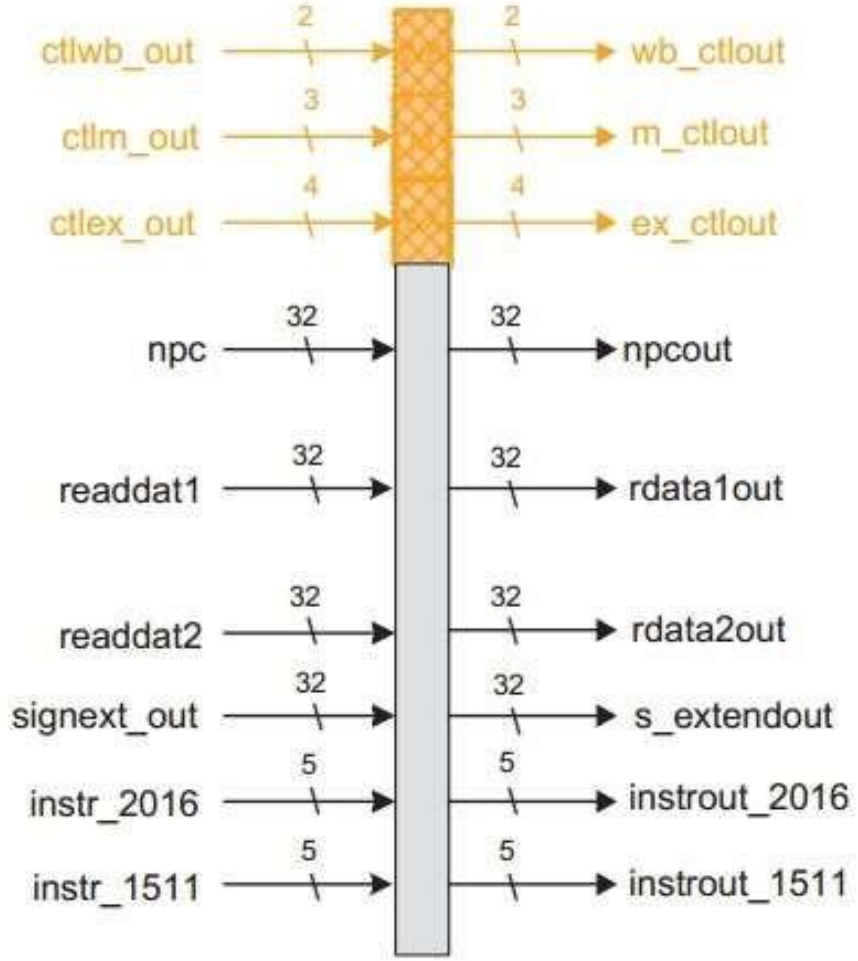
Writeback Pipe I/O

- Inputs:
  - Address/ ReadData(From last stage)
  - MemToReg(From CU)
- Outputs
  - Writedata(To register file)

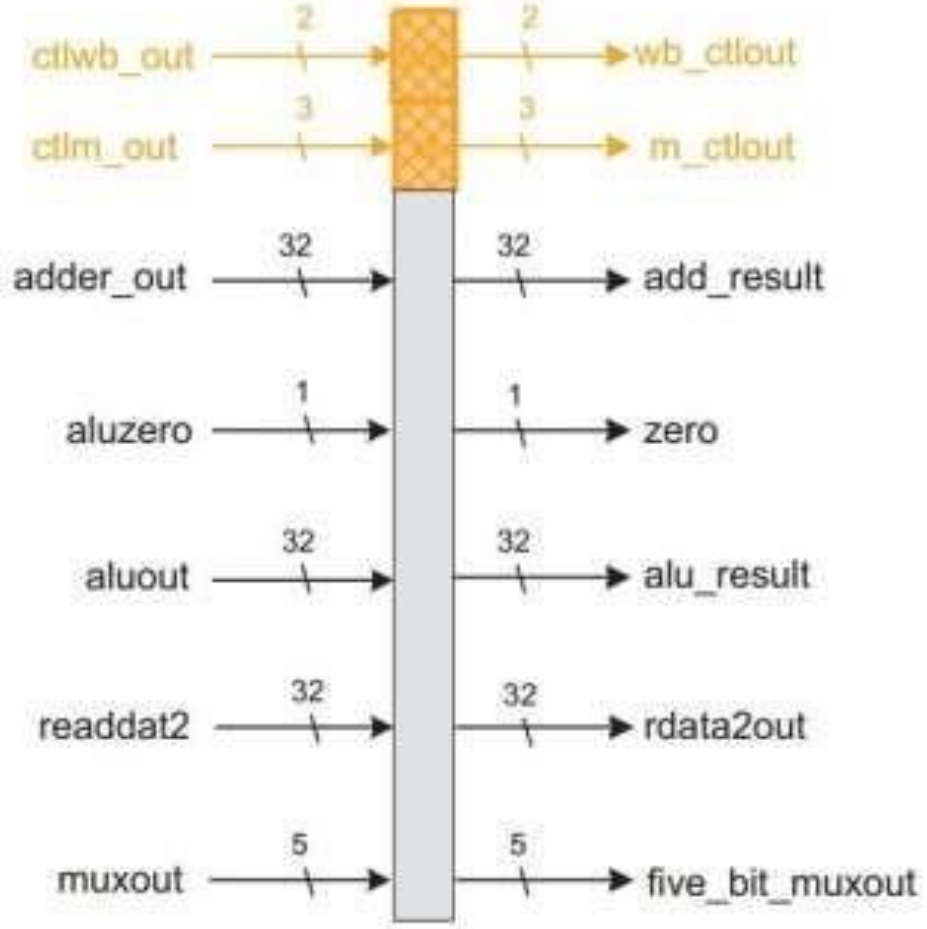
IF/ID pipeline register



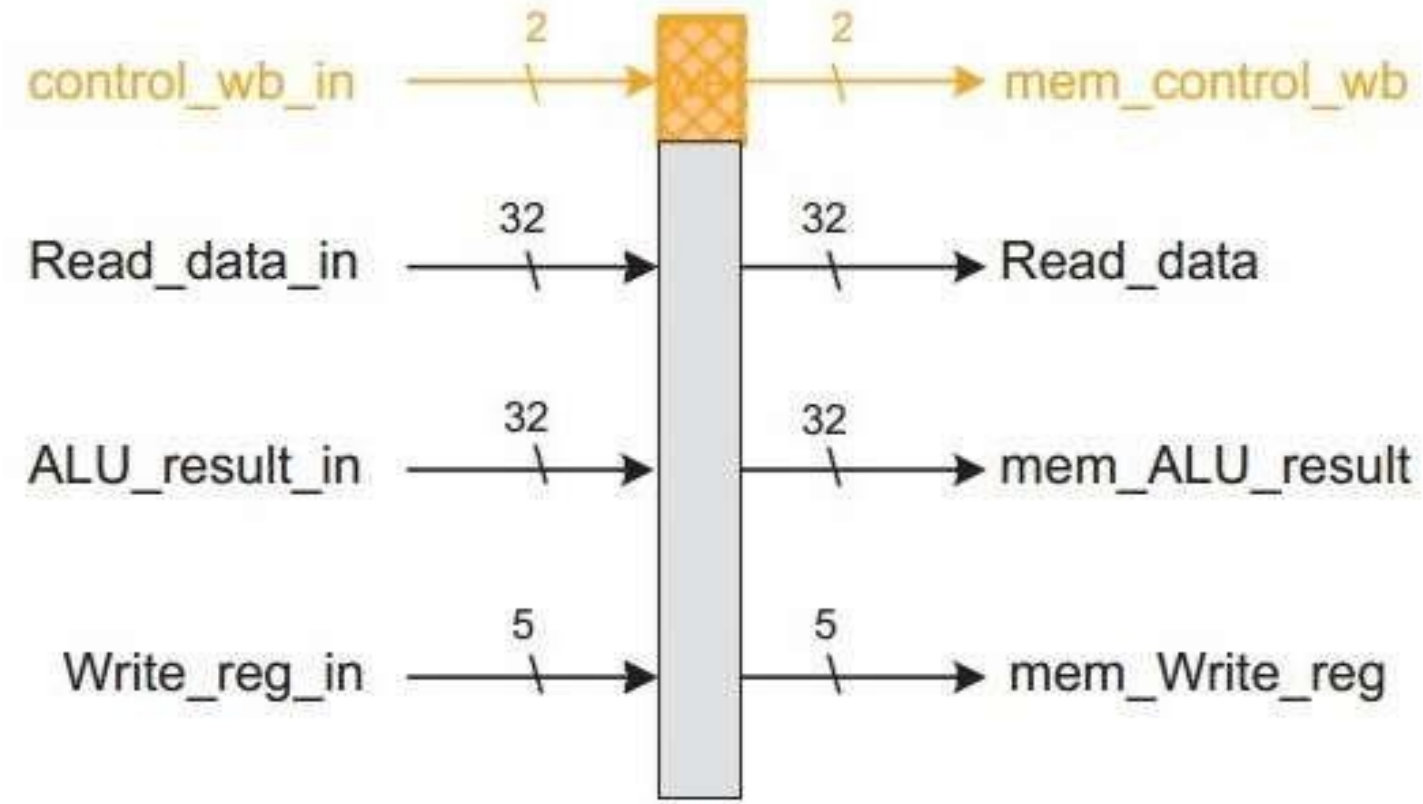
ID/EX pipeline register



EX/MEM pipeline register



MEM/WB pipeline register



END!